原盛科技股份有限公司
PrimeSensor Technology Inc.

PS5510
DATA SHEET

PRELIMINARY

1/2.5” 5MP CMOS IMAGE SENSOR

Mar. 2017

Version 0.2

PS5510 5MP CMOS IMAGE SENSOR

General Description

The **PS5510** is a highly integrated CMOS image sensor that output of **2592x1944 (5MP)** pixels with rolling shutter readout. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. **PS5510** outputs 10-bit RGB raw data through MIPI CSI-2 interface. It is available in **PLCC** and **CSP** package.

The **PS5510** can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **2592 x 1944 pixels with Bayer-RGB color filter array and micro-lens**
- **Output format:**
  - 10-bit RAW RGB
- **Output interface**
  - 4 lane MIPI output, up to 900Mbps
- **On-chip column A/D converter**
- **On-chip manual analog gain control**
- **Continuous variable frame time & exposure time**
- **I2C™ Interface**
- **Automatic black-level calibration**
- **Black sun cancellation**
- **Programmable fast-switch configuration**
- **Support Dual-Exposure DOL HDR output**
- **Support multi-sensor frame synchronization**
- **Support WOI and subsampling**
- **Support dummy line & pixel timing**
- **Support output Hsync at Vsync**
- **Support 1.7V~3.3V I/O**
- **On-chip PLL**
  (input_clock / PLL_m >= 1MHz)

Specifications

Parameter	Typical Value
Active array size	2608(H) x 1960(V)
Pixel size	2.25um (H) x 2.25um (V)
Shutter type	Electronic rolling shutter (ERS)
Optical format	1/2.5-inch
Lens chief ray angle	12.6 degree
ADC	10-bit
Sensitivity	2000 mV/Lux-sec
SNRmax	39 dB
Dynamic range	74 dB (Typical) 98dB (DOL HDR)
Scan mode	Progressive scan
Input clock	Max 64Hz
Pixel clock	Max 160 MHz
Max. frame rate	5MP: 2592x1944 @ 30fps 1080p: 1920x1080 @ 60fps
Supply voltage	Analog: 3.3 V Digital: 1.2 V I/O: 1.7V~3.3V
Power consumption	188mW
Operating temperature	-30 ºC ~85 ºC

Applications

- **Surveillance HD-CCTV Camera**
- **Surveillance IP Camera**
- **360 Panoramic Camera**
- **Sports DV Camera**
- **Car Video Recorder**
- **Video Door Phone**

Ordering Information

Part Number	Description
PS5510PP	56-Pin PLCC
PS5510LT	53-Ball CSP

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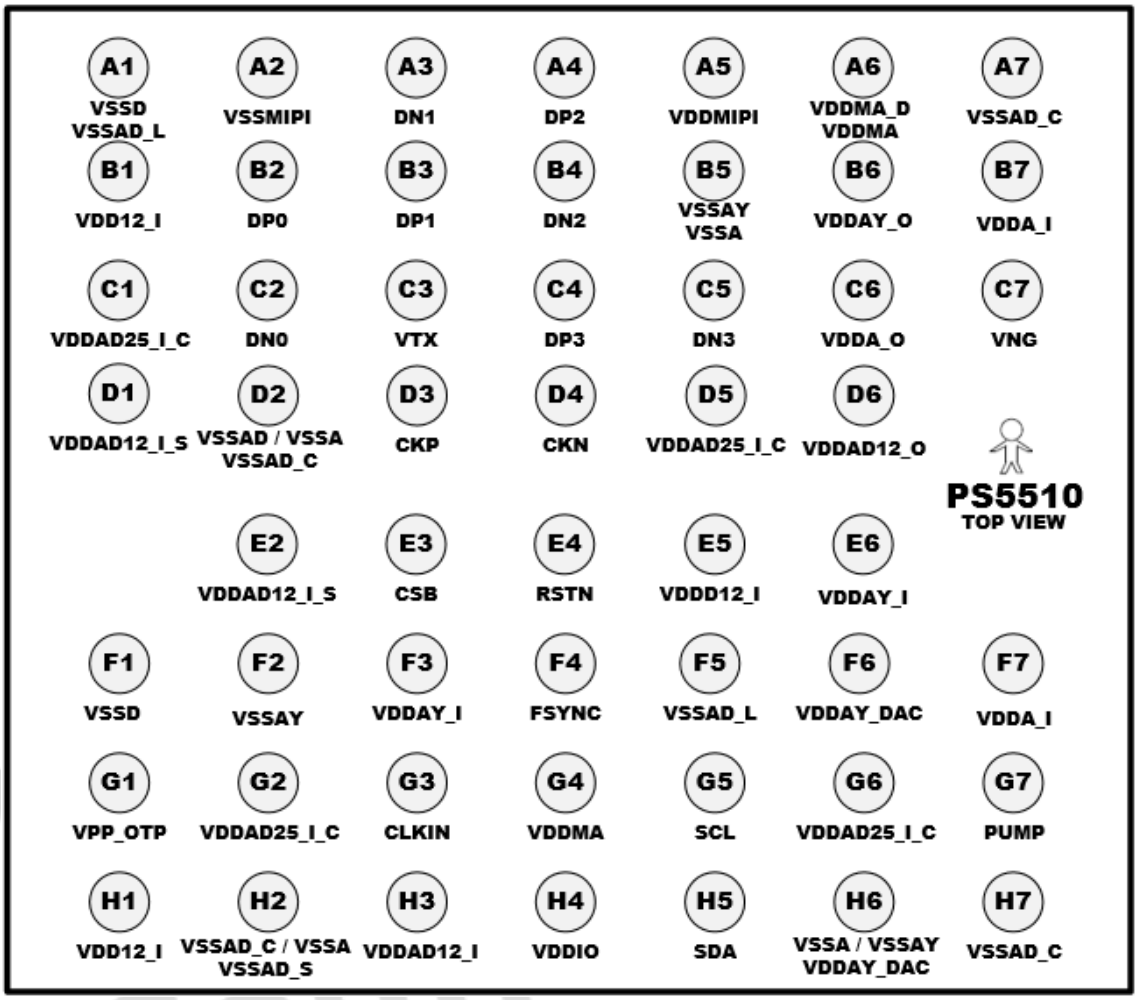
E-mail: fae.service@primesensor.com

1. Pin Assignment



Pin No.	Name	Type	Description
A1	**VSSD/VSSAD_L**	GND	Analog Ground
A2	**VSSMIPI**	GND	MIPI ground
A3	**DN1**	Output	MIPI digital data output_1 negative terminal
A4	**DP2**	Output	MIPI digital data output_2 positive terminal
A5	**VDDMIPI**	Power	MIPI VDD (1.2V)
A6	**VDDMA_D/VDDMA**	Power	Analog power : 3.3V
A7	**VSSAD_C**	GND	Analog Ground
B1	**VDD12_I**	Power	Digital power : 1.2V
B2	**DP0**	Output	MIPI digital data output_0 positive terminal
B3	**DP1**	Output	MIPI digital data output_1 positive terminal
B4	**DN2**	Output	MIPI digital data output_2 negative terminal
B5	**VSSAY/VSSA**	GND	Analog Ground
B6	**VDDAY_O**	Power	VDDAY LDO output voltage(2.7-3.0V)

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B7	**VDDA_I**	Power	Sensor power input
C1	**VDDAD25_I_C**	Power	Analog power input voltage (1.2V ~ 3V)
C2	**DN0**	Output	MIPI digital data output_0 negative terminal
C3	**VTX**	Power	MIPI internal TX power (0.4 V)
C4	**DP3**	Output	MIPI digital data output_3 positive terminal
C5	**DN3**	Output	MIPI digital data output_3 negative terminal
C6	**VDDA_O**	Power	VDDA LDO output voltage(2.7-3.0V)
C7	**VNG**	Ref.	Reference voltage
D1	**VDDAD12_I_S**	Power	Analog power input voltage (1.2V ~ 3V)
D2	**VSSAD_S/VSSAD_C/VSSA**	GND	Analog Ground
D3	**CKP**	Output	MIPI output clock positive terminal
D4	**CKN**	Output	MIPI output clock negative terminal
D5	**VDDAD25_I_C**	Power	Analog power input voltage (1.2V ~ 3V)
D6	**VDDAD12_O**	Power	Internal 1.2V LDO output voltage
E2	**VDDAD12_I_S**	Power	Analog power input voltage (1.2V ~ 3V)
E3	**CSB**	Input	Suspend control, "1" : suspend, "0" : normal function
E4	**RSTN**	Input	Reset signal, active low, internal pull high
E5	**VDDD12_I**	Power	Analog power input voltage(1.2V)
E6	**VDDAY_I**	Power	Sensor power input
F1	**VSSD**	GND	Digital ground
F2	**VSSAY**	GND	Analog ground
F3	**VDDAY_I**	Power	Sensor power input
F4	**FSYNC**	Input	Frame sync signal
F5	**VSSAD_L**	GND	Analog Ground
F6	**VDDAY_DAC**	Power	Sensor power input
F7	**VDDA_I**	Power	Analog power input voltage (2.7V ~ 3V)
G1	**VPP_OTP**	Power	External voltage for OTP device
G2	**VDDAD25_I_C**	Power	Analog power input voltage (1.2V ~ 3V)
G3	**CLKIN**	Input	Master clock input
G4	**VDDMA**	Power	Analog power : 3.3V
G5	**SCL**	Input	I2C clock, open drain type
G6	**VDDAD25_I_C**	Power	Analog power input voltage (1.2V ~ 3V)
G7	**PUMP**	Power	Positive pump output voltage
H1	**VDD12_I**	Power	Digital power : 1.2V
H2	**VSSAD_C/VSSA/VSSAD_S**	GND	Analog Ground
H3	**VDDAD12_I**	Power	Analog power input voltage(1.2V)
H4	**VDDIO**	Power	I/O power : 1.8V ~ 3.3V
H5	**SDA**	Input	I2C data, open drain type
H6	**VSSA/VSSAY/VSSAY_DAC**	GND	Analog ground
H7	**VSSAD_C**	GND	Analog ground

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2. Specifications

Absolute Maximum Ratings		
Operating Temperature		-30 ºC ~85 ºC
Ambient Storage Temperature		-40ºC ~ 125ºC
Supply Voltage (with respect to ground)	V_{DDA}	4.5V
	V_{DDD}	3.0V
	V_{DDIO}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to V_{DDIO} + 0.5V
Lead-free temperature, Surface-mount process		245ºC
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)					
Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDA}	DC supply voltage – Analog	3.0	3.3	3.6	V
V_{DDD}	DC supply voltage – Digital core	1.1	1.2	1.3	V
V_{DDIO}	DC supply voltage – I/O	1.7		3.3	V
I_{DDA}	Operating Current – Analog (2-lane MIPI)		38		mA
I_{DDD}	Operating Current – Digital (2-lane MIPI)		48		mA
I_{DDIO}	Operating Current – I/O (2-lane MIPI)		1		mA
Type : IN & I/O					
V_{IH}	Input Voltage HIGH	V_{DDIO} * 0.7			V
V_{IL}	Input Voltage LOW			V_{DDIO} * 0.3	V
Type : OUT & I/O					
V_{OH}	Output Voltage HIGH	V_{DDIO} * 0.9			V
V_{OL}	Output Voltage LOW			V_{DDIO} * 0.1	V

AC Operating Condition					
Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency			64	MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%

Sensor Characteristics		
Parameter	Typ.	Unit
Sensitivity	2000	mV/Lux-Sec
Signal to Noise Ratio MAX	38.5	dB
Dynamic Range	74	dB

†: Sensor function works in the ambient operating temperature range. However, the image quality may change at high temperaturecondition.

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3. I²C™ Bus

PS5510 supports I²C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1001000" and supports receiving / transmitting speed as maximum 400 kHz.

I²C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 3.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 3.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

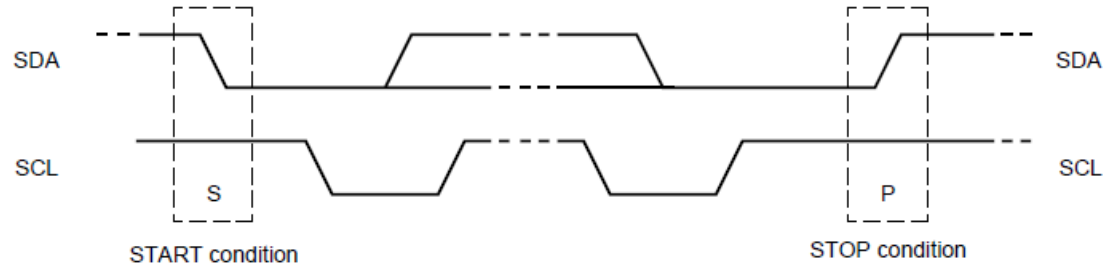

Fig.3.1 Start and Stop Condition

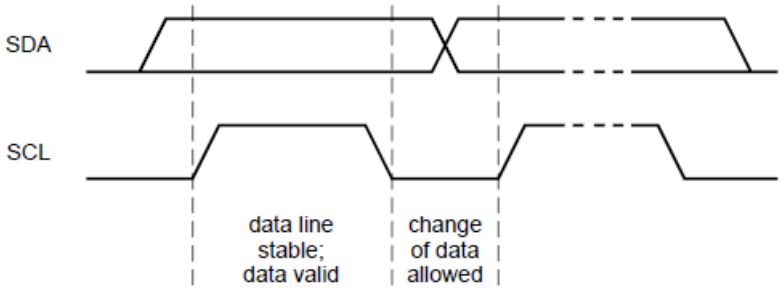

Fig.3.2 Valid Data

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Data Transfer Format

Master transmits data to salve (write cycle)

- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of **PS5510** internal control registers. (Please refer to **PS5510** register description)

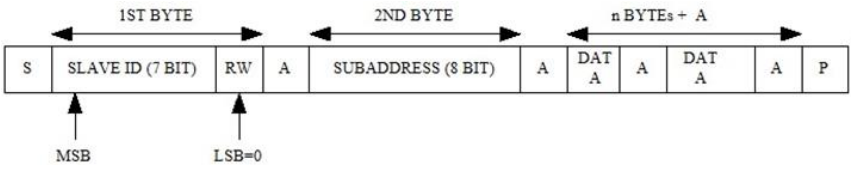

Fig.3.3 Master-transmitter transmits to slave-receiver

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (**PS5510**) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the **PS5510** acknowledgment, the master places the 8 bits data on SDA line and transmit to **PS5510** control register (address was assigned by 2nd byte). After **PS5510** issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the **PS5510** sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside **PS5510** can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.

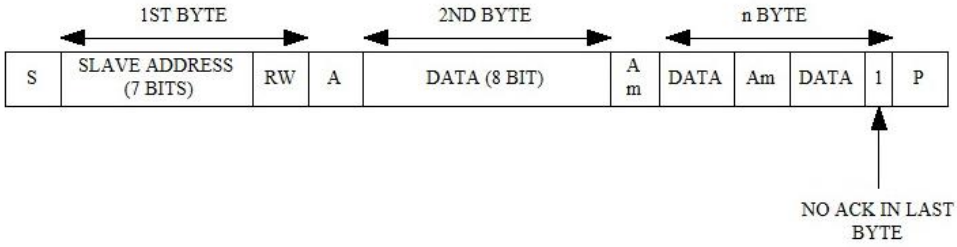

Fig.3.4 Slave-transmitter transmits to master-receiver

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by **PS5510**. The 8 bits data was read from **PS5510** internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the **PS5510** place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (**PS5510**) must releases SDA line to master to generate STOP condition.

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I²C™ Bus Timing

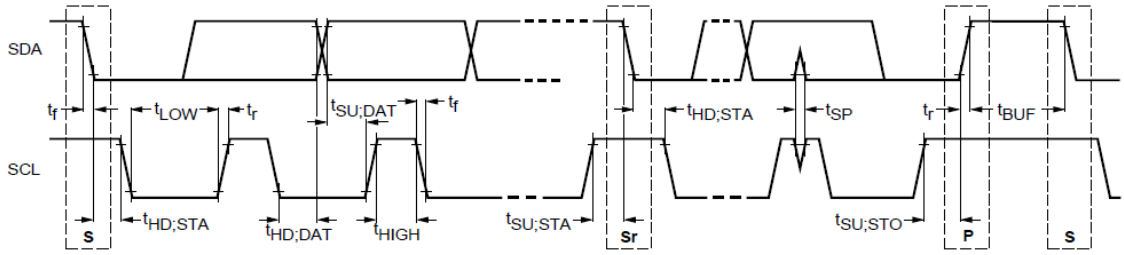

Fig.3.5 Definition of timing for F/S mode devices on the I2C-bus

I²C™ Bus Timing Specification						
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency.	f_{scl}	10	100	0	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	0.6	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	1.3	-	µs
High period of the SCL clock.	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	5.0	3.45	0	0.9	µs
Data set-up time.	$t_{SU;DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals.	t_r	-	1000	20+0.1Cb	300	ns (notel)
Fall time of both SDA and SCL signals.	t_f	-	300.	20+0.1Cb	300	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line.	C_b	-	400	-	400	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	0.2 VDD	-	V

Note: It depends on the “high” period time of SCL.

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4. Register Table

Bank	Address		Bit	Name	R/W	Description
	Hex	Dec				
0	00	00	[7:0]	PartID[15:8]	R	Sensor ID
0	01	01	[7:0]	PartID[7:0]	R	Sensor ID
0	02	02	[3:0]	VersionID[3:0]	R	Sensor ID
0	03	03	[3:0]	SubID[3:0]	R	Sensor ID
0	11	17	[7]	Cmd_GatedAllClk	R/W	Clock Gated Control (1: Gate Clock)
0	BE	190	[6]	Cmd_Pxclk_Inv	R/W	Invert Pxclk Out
			[5]	Cmd_Vsync_Inv	R/W	Invert Vsync Out
			[4]	Cmd_Hsync_Inv	R/W	Invert Hsync Out
1	04	04	[6:4]	R_PxclkO_dly[2:0]	R/W	Timing Delay for Pxclk
			[2:0]	R_HsyncO_dly[2:0]	R/W	Timing Delay for Hsync
1	05	05	[6:4]	R_VsyncO_dly[2:0]	R/W	Timing Delay for Vsync
			[3]	Cmd_8_TriState	R/W	TriState IO of PxData[1:0]
			[2]	Cmd_Sw_PwrDn	R/W	Power-Down Control
			[1]	Cmd_Sw_TriState	R/W	TriState IO of PxData, Hsync, Vsync, and Pxclk
1	09	09	[0]	UpdateFlag	W	Exposure & Gain Update Control (Write 0x01)
1	0A	10	[7:0]	Cmd_Lpf[15:8]	R/W	Line per frame = Cmd_Lpf + 1
1	0B	11	[7:0]	Cmd_Lpf[7:0]	R/W	Line per frame = Cmd_Lpf + 1
1	0C	12	[7:0]	Cmd_OffNy1[15:8]	R/W	Exposure Control
1	0D	13	[7:0]	Cmd_OffNy1[7:0]	R/W	Exposure Control
1	0E	14	[3:0]	Cmd_OffNe1[11:8]	R/W	Exposure Control
1	0F	15	[7:0]	Cmd_OffNe1[7:0]	R/W	Exposure Control
1	1B	27	[7]	Cmd_Hflip	R/W	Horizontal Flip
			[6:5]	Cmd_Askip_H[1:0]	R/W	Horizontal Skip
			[2:0]	Cmd_Hsize_e1[11:8]	R/W	Raw Image Horizontal Size
1	1C	28	[7:0]	Cmd_Hsize_e1[7:0]	R/W	Raw Image Horizontal Size
1	1D	29	[7]	Cmd_Vflip	R/W	Vertical Flip
			[6:5]	Cmd_Askip_V[1:0]	R/W	Vertical Skip
			[2:0]	Cmd_Vsize[10:8]	R/W	Raw Image Vertical Size
1	1E	30	[7:0]	Cmd_Vsize[7:0]	R/W	Raw Image Vertical Size

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1	1F	31	[2:0]	Cmd_Vstart[10:8]	R/W	Raw Image Vertical Offset
1	20	32	[7:0]	Cmd_VStart[7:0]	R/W	Raw Image Vertical Offset
1	27	39	[4:0]	Cmd_LineTime[12:8]	R/W	Line Time = Cmd_LineTime clock cycles
1	28	40	[7:0]	Cmd_LineTime[7:0]	R/W	Line Time = Cmd_LineTime clock cycles
1	78	120	[0]	Cmd_GDAC[8]	R/W	Gain Control
1	79	121	[7:0]	Cmd_GDAC[7:0]	R/W	Gain Control
1	90	144	[1]	Cmd_ADC_Sample_Rotate	R/W	ADC sample order control
			[0]	Cmd_Adc_sample_posedge	R/W	ADC sample timing control
1	92	146	[4:0]	R_ISP_TestMode[4:0]	R/W	Test Image Control
1	93	147	[7:0]	R_ISP_TestValueLo[7:0]	R/W	Test Image Control
1	94	148	[7:0]	R_ISP_TestValueHi[7:0]	R/W	Test Image Control
1	91	151	[0]	Cmd_Pga_D1frm	R/W	Pga Gain auto-delay one frame
1	A3	163	[4]	Cmd_WOI_VOffset_sign	R/W	Vertical offset of output image
			[2:0]	Cmd_WOI_VOffset[10:8]	R/W	Vertical offset of output image
1	A4	164	[7:0]	Cmd_WOI_VOffset[7:0]	R/W	Vertical offset of output image
1	A5	165	[2:0]	Cmd_WOI_VSize[10:8]	R/W	Vertical size of output image
1	A6	166	[7:0]	Cmd_WOI_VSize[7:0]	R/W	Vertical size of output image
1	A7	167	[4]	Cmd_WOI_HOffset_sign	R/W	Horizontal offset of output image
			[3:0]	Cmd_WOI_HOffset[11:8]	R/W	Horizontal offset of output image
1	A8	168	[7:0]	Cmd_WOI_HOffset[7:0]	R/W	Horizontal offset of output image
1	A9	169	[3:0]	Cmd_WOI_HSize[11:8]	R/W	Horizontal size of output image
1	AA	170	[7:0]	Cmd_WOI_HSize[7:0]	R/W	Horizontal size of output image
1	AB	171	[5:0]	Cmd_Np[5:0]	R/W	Frequency eliminate control
1	E3	227	[5]	T_SR_GPIO	R/W	IO slew control
			[1:0]	T_OPDRV_GPIO[1:0]	R/W	IO driving Strength
1	F1	241	[5:0]	T_spll_predivider[5:0]	R/W	PLL Control
1	F2	242	[5:0]	T_spll_postdivider [5:0]	R/W	PLL Control
1	F5	245	[1:0]	T_spll_modedivider [1:0]	R/W	PLL Control
2	46	70	[7]	Cmd_DigDac_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	47	71	[7:0]	Cmd_DigDac_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	48	72	[7]	Cmd_DigDac_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[2:0]	Cmd_DigDac_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel

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2	49	73	[7:0]	Cmd_DigDac_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	4A	74	[7]	Cmd_DigDac_Gr_Sign	R/W	Black Level Offset for Gr Channel
			[2:0]	Cmd_DigDac_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	4B	75	[7:0]	Cmd_DigDac_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	4C	76	[7]	Cmd_DigDac_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	4D	77	[7:0]	Cmd_DigDac_R_Offset[7:0]	R/W	Black Level Offset for R Channel

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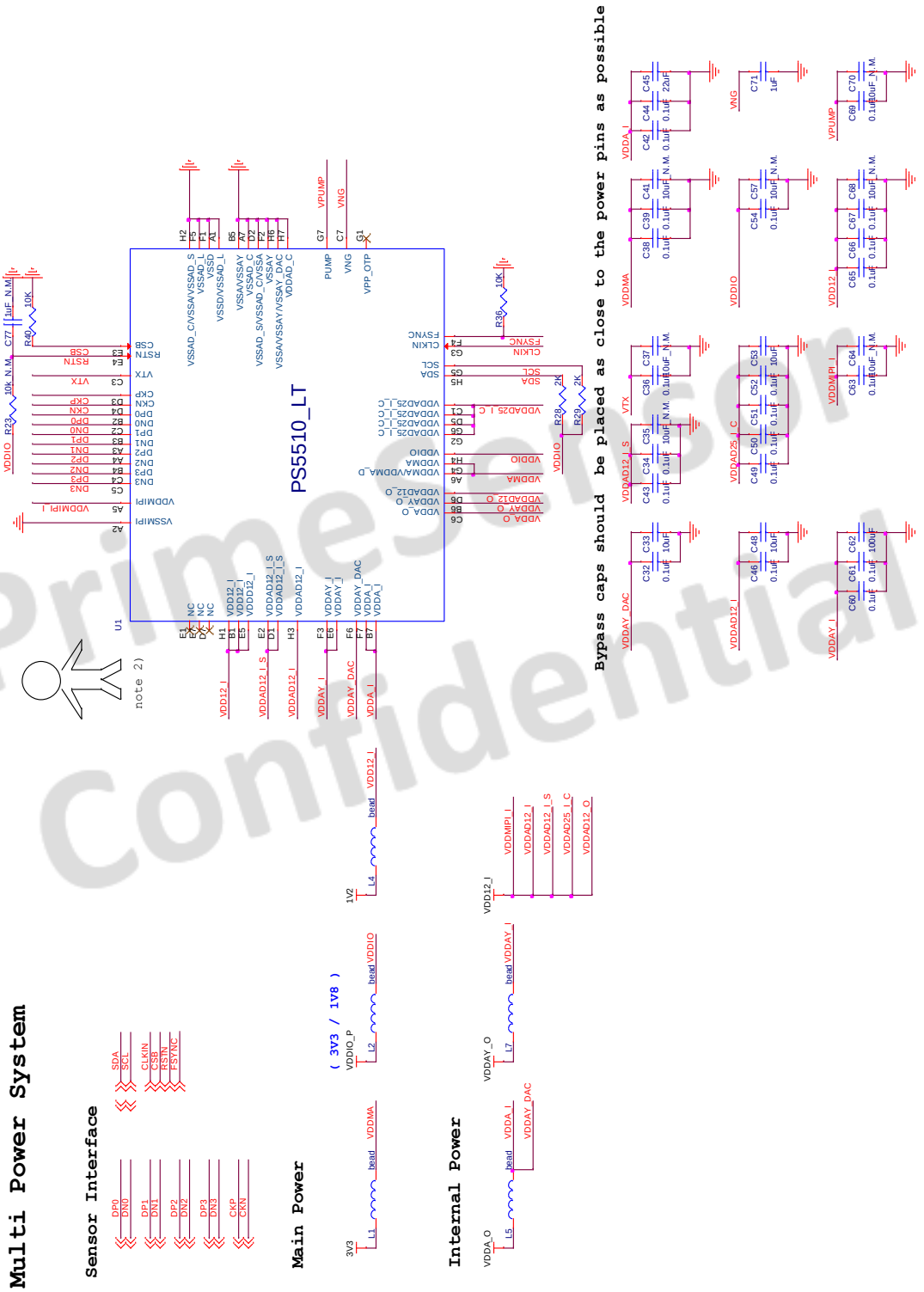
5. Reference Circuit Schematic

➢ **reference circuit for multi power system**



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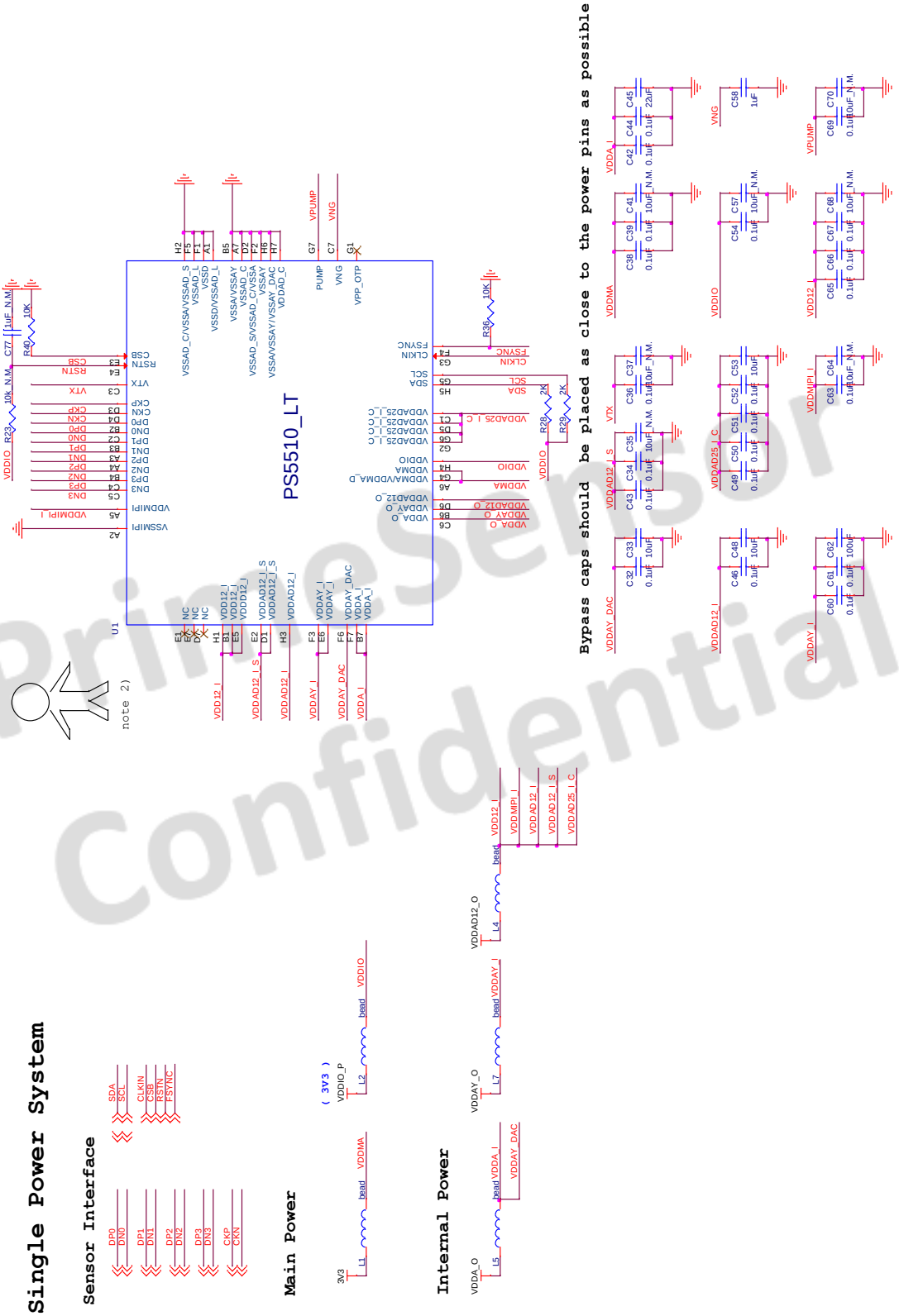
➢ reference circuit for single power system



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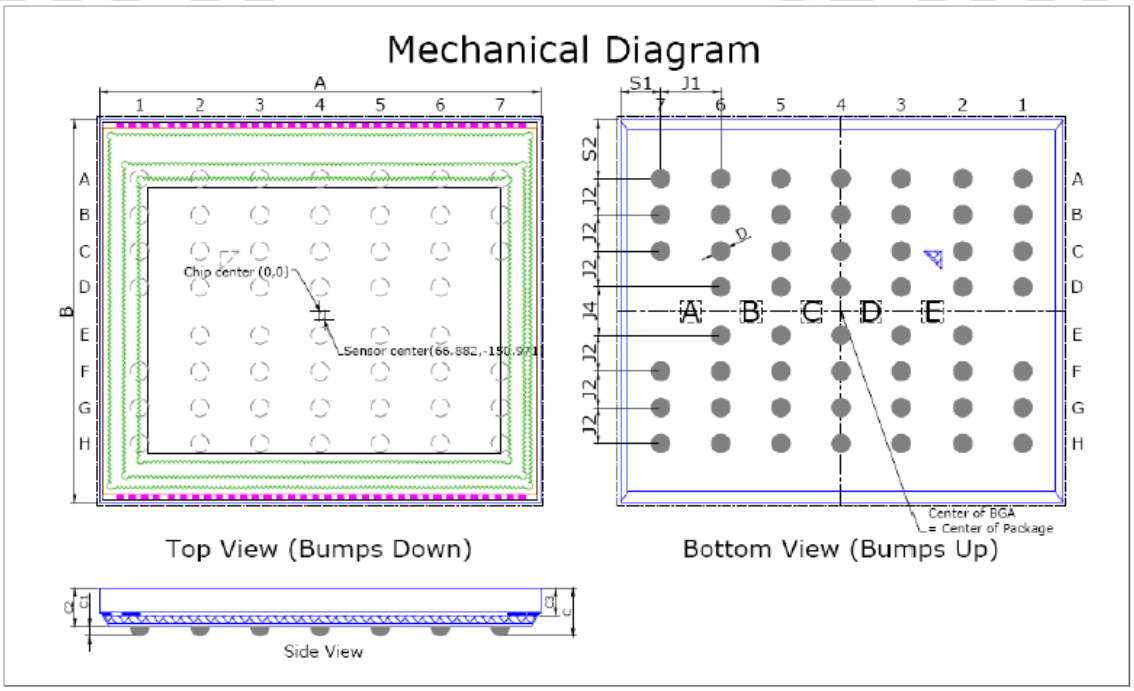
6. Package Information

- **Package Outline Dimension**

	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	7325	7300	7350
Package Body Dimension Y	B	6349	6324	6374
Package Height	C	790	730	850
Ball Height	C1	160	130	190
Package Body Thickness	C2	630	585	675
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	300	270	330
Total Pin Count	N	53		
Pin Count X axis	N1	7		
Pin Count Y axis	N2	8		
Pins Pitch X axis	J1	1000		
Pins Pitch Y axis	J2	600		
	J4	800		
Edge to Pin Center Distance along X	S1	662.5	632.5	692.5
Edge to Pin Center Distance along Y	S2	974.5	944.5	1004.5



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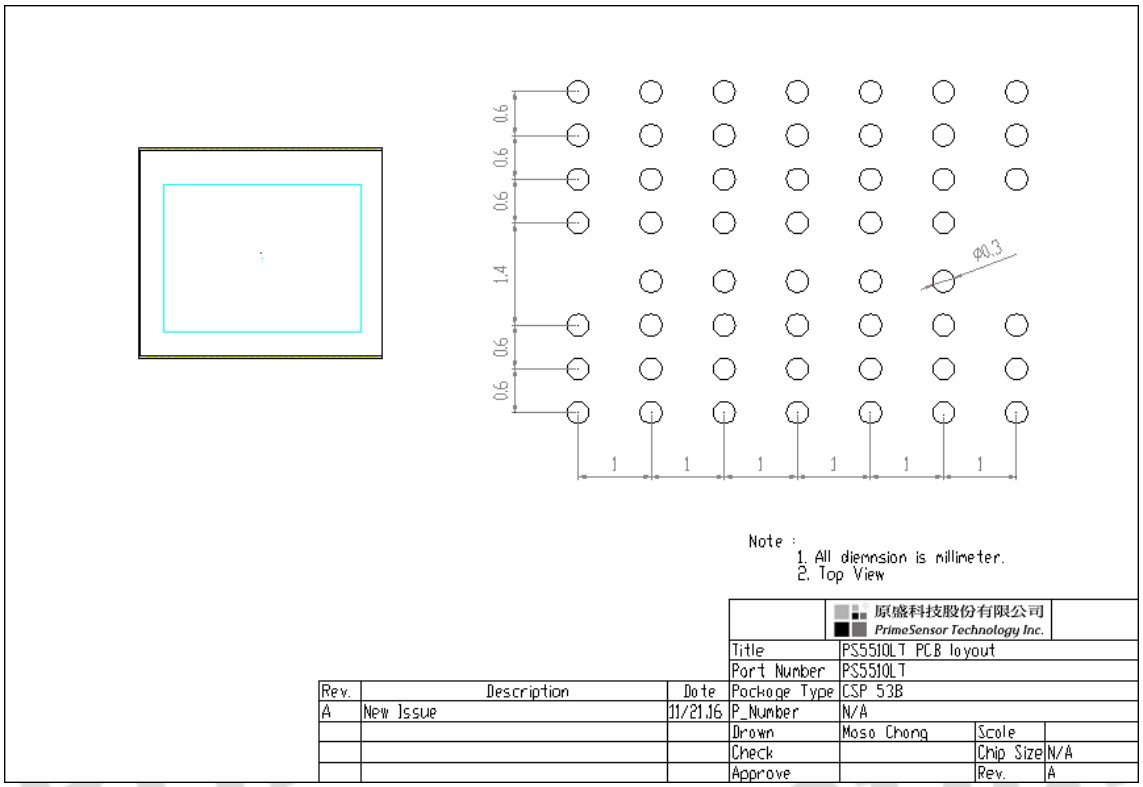
- **Recommended PCB Layout**



- If use FPC (Flex) board, need add stiffener onto the back-side to enhance the Flex strength.
- Recommended Stiffener type: FR4 or stainless steel or equivalent material.

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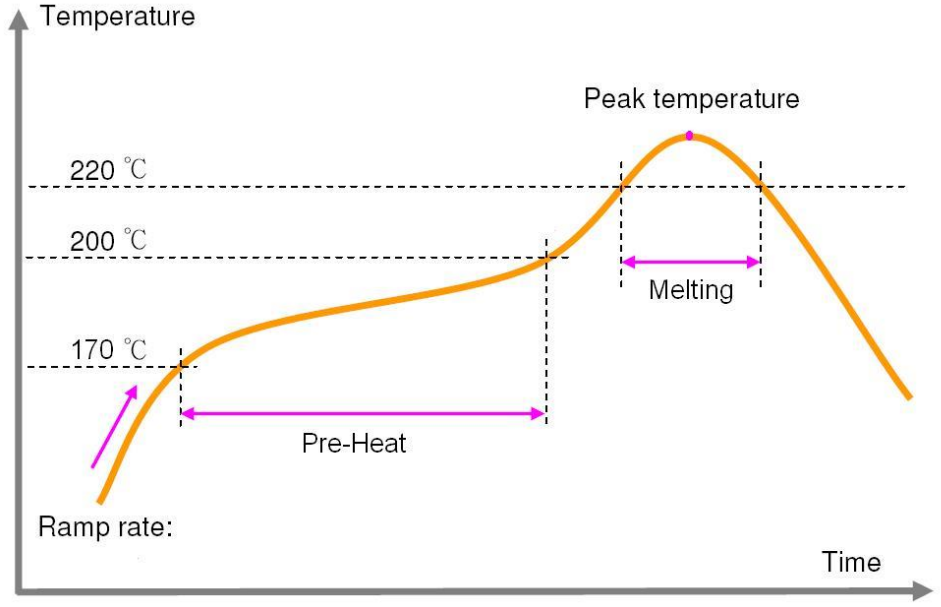
- **Recommended Guideline for PCB Assembly**

I. Recommended vender and type for Pb-free solder paste
   1 Almit LFM-48W TM-HP
   2 Senju M705-GRN360-K

II. IR Reflow Soldering Profile:

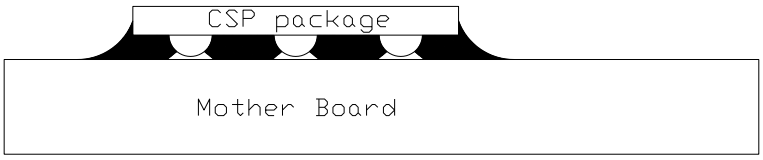
Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.



- **Reflow Profile**
  1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
  2. Preheat zone:
     2.1 Temp ramp from 170~ 200 degree C
     2.2 Exposure time: 90 +/- 30 sec
  3. Melting zone:
     3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
     3.2 Peak temperature: 245 degree C.

III. Others

- **Epoxy under-filled process is required post IC mounting process.**



- **Peek tweezers or plastic tweezers is required post IC manual handling for pick and place.**

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7. Revision History

Revision	Description	Date
V0.1	Preliminary data sheet release	Dec. 23, 2016
V0.2	Update reference schematics, sensor spec, PCB Layout	Mar. 13, 2017

PrimeSensor Technology Inc.
E-mail: fae.service@primesensor.com