原盛科技股份有限公司
PrimeSensor Technology Inc.

PS5220
DATA SHEET

PRELIMINARY

1/2.7” Full-HD 1080p CMOS IMAGE SENSOR

May 2016

Version 0.8

PS5220 Full-HD 1080p CMOS IMAGE SENSOR

General Description

The **PS5220** is a highly integrated CMOS image sensor that output of **1920x1080 (Full HD-1080p)** pixels with rolling shutter readout. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. **PS5220** outputs 10-bit RGB raw data through a parallel data bus. It is available in **CLCC** and **CSP** package.

The **PS5220** can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **1936 x 1096 pixels with Bayer-RGB color filter array and micro-lens**
- **Output format:**
  - 10-bit RAW RGB
- **Output interface**
  - 10bit parallel DVP output
- **On-chip column A/D converter**
- **On-chip manual analog gain control**
- **Continuous variable frame time & exposure time**
- **I2C™ Interface**
- **Automatic black-level calibration**
- **Black sun cancellation**
- **Programmable fast-switch configuration**
- **Support WOI and subsampling**
- **Support dummy line & pixel timing**
- **Support output Hsync at Vsync**
- **Support 1.7V~3.3V I/O**
- **On-chip PLL**
  (input_clock / PLL_m >= 1MHz)

Specifications

Parameter	Typical Value
Active array size	1936(H) x 1096(V)
Pixel size	3.0um (H) x 3.0um (V)
Shutter type	Electronic rolling shutter (ERS)
Optical format	1/2.7-inch
Lens chief ray angle	17 degree
ADC	10-bit
Sensitivity	3300 mV/Lux-sec
SNRmax	39 dB
Dynamic range	70 dB
Scan mode	Progressive scan
Input clock	Max 64MHz
Pixel clock	Max 81MHz
Max. frame rate	1080p: 1920x1080 @30fps 720p: 1280x720 @60fps VGA: 640x480 @120fps
Supply voltage	Analog: 3.3 V Digital: 1.2 V I/O: 1.7V~3.3V
Power consumption	85mW
Operating temperature	-30°C ~ 85°C

Applications

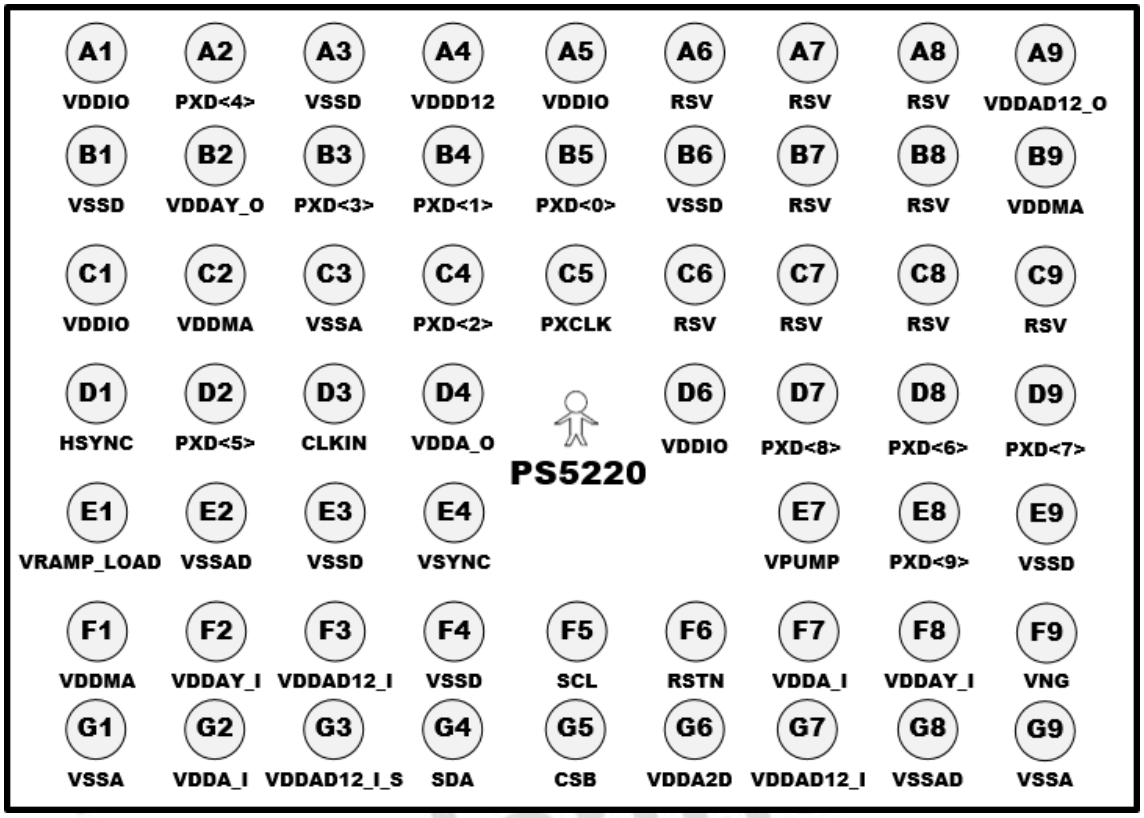
- **Surveillance HD-CCTV Camera**
- **Surveillance IP Camera**
- **Car Video Recorder**
- **Sports Camera**
- **Automotive Camera**
- **Video Door Phone**

Ordering Information

Part Number	Description
PS5220CA	48-Pin CLCC
PS5220LT	60-Ball CSP

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

1. Pin Assignment



Pin No.	Name	Type	Description
A1	**VDDIO**	Power	Input IO voltage
A2	**PXD<4>**	Output	pixel data output
A3	**VSSD**	GND	Digital ground
A4	**VDDD12**	Power	Input 1.2V Core power
A5	**VDDIO**	Power	Input IO voltage
A6	**RSV**	-	Reserved Pin
A7	**RSV**	-	Reserved Pin
A8	**RSV**	-	Reserved Pin
A9	**VDDAD12_O**	Power	Output Reference Power
B1	**VSSD**	GND	Digital ground
B2	**VDDAY_O**	Power	Output Reference Power
B3	**PXD<3>**	Output	pixel data output
B4	**PXD<1>**	Output	pixel data output
B5	**PXD<0>**	Output	pixel data output
B6	**VSSD**	GND	Digital ground
B7	**RSV**	-	Reserved Pin
B8	**RSV**	-	Reserved Pin
B9	**VDDMA**	Power	Input 3.3V Main Power

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

C1	**VDDIO**	Power	Input IO voltage
C2	**VDDMA**	Power	Input 3.3V Main Power
C3	**VSSA**	GND	Analog ground
C4	**PXD<2>**	Output	pixel data output
C5	**PXCLK**	Output	Pixel clock out
C6	**RSV**	-	Reserved Pin
C7	**RSV**	-	Reserved Pin
C8	**RSV**	-	Reserved Pin
C9	**RSV**	-	Reserved Pin
D1	**HSYNC**	Output	Asserted when DOUT line data is valid
D2	**PXD<5>**	Output	pixel data output
D3	**CLKIN**	Input	External input clock
D4	**VDDA_O**	Power	Output Reference Power
D6	**VDDIO**	Power	Input IO voltage
D7	**PXD<8>**	Output	pixel data output
D8	**PXD<6>**	Output	pixel data output
D9	**PXD<7>**	Output	pixel data output
E1	**VRAMP_LOAD**	Power	Input Reference Power
E2	**VSSAD**	GND	Analog ground
E3	**VSSD**	GND	Digital ground
E4	**VSYNC**	Output	Asserted when DOUT frame data is valid
E7	**VPUMP**	Power	Reference Power
E8	**PXD<9>**	Output	pixel data output
E9	**VSSD**	GND	Digital ground
F1	**VDDMA**	Power	Input 3.3V Main Power
F2	**VDDAY_I**	Power	Input Reference Power
F3	**VDDAD12_I**	Power	Input 1.2V Core power
F4	**VSSD**	GND	Digital ground
F5	**SCL**	Input	I2C clock
F6	**RSTN**	Input/PU	Reset signal, active low, internal pull high
F7	**VDDA_I**	Power	Input Reference Power
F8	**VDDAY_I**	Power	Input Reference Power
F9	**VNG**	Power	Output Reference Power
G1	**VSSA**	GND	Analog ground
G2	**VDDA_I**	Power	Input Reference Power
G3	**VDDAD12_I_S**	Power	Input 1.2V Core power
G4	**SDA**	Input/Output/OD	I2C data, open drain type
G5	**CSB**	Input	Chip select, Active Low
G6	**VDDA2D**	Power	Input Reference Power
G7	**VDDAD12_I**	Power	Input 1.2V Core power
G8	**VSSAD**	GND	Analog ground
G9	**VSSA**	GND	Analog ground

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

2. Specifications

Absolute Maximum Ratings		
Operating Temperature (sensor junction temperature)		-30°C ~ 85°C
Ambient Storage Temperature		-40°C ~ 125°C
Supply Voltage (with respect to ground)	V_{DDA}	4.5V
	V_{DDD}	3.0V
	V_{DDIO}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to V_{DDIO} + 0.5V
Lead-free temperature, Surface-mount process		245°C
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)					
Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDA}	DC supply voltage – Analog	3.14	3.3	3.46	V
V_{DDD}	DC supply voltage – Digital core	1.1	1.15	1.2	V
V_{DDIO}	DC supply voltage – I/O	1.7	1.8	3.3	V
I_{DDA}	Operating Current – Analog		18		mA
I_{DDD}	Operating Current – Digital		22		mA
Type : IN & I/O					
V_{IH}	Input Voltage HIGH	V_{DDIO} * 0.7			V
V_{IL}	Input Voltage LOW			V_{DDIO} * 0.3	V
Type : OUT & I/O					
V_{OH}	Output Voltage HIGH	V_{DDIO} * 0.9			V
V_{OL}	Output Voltage LOW			V_{DDIO} * 0.1	V

AC Operating Condition					
Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency			64	MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%

Sensor Characteristics		
Parameter	Typ.	Unit
Sensitivity	3300	mV/Lux-Sec
Signal to Noise Ratio MAX	39	dB
Dynamic Range	70	dB

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

3. I²C™ Bus

PS5220 supports I²C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1001000" and supports receiving / transmitting speed as maximum 400 kHz.

I²C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 3.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 3.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

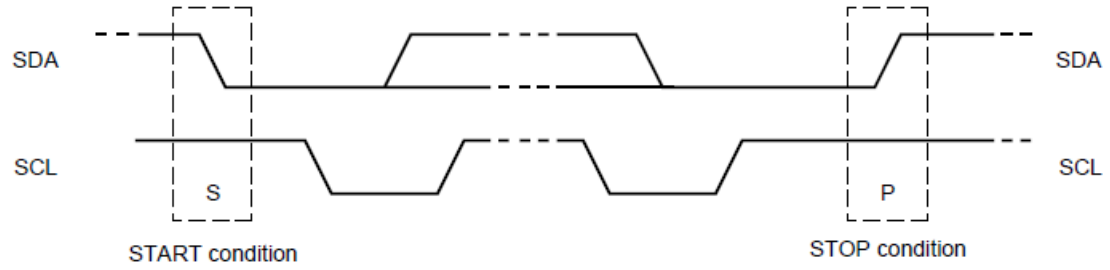


Fig.3.1 Start and Stop Condition

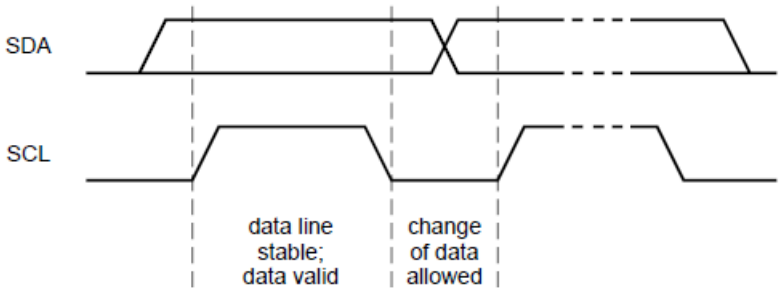


Fig.3.2 Valid Data

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

Data Transfer Format

Master transmits data to salve (write cycle)

- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of **PS5220** internal control registers. (Please refer to **PS5220** register description)

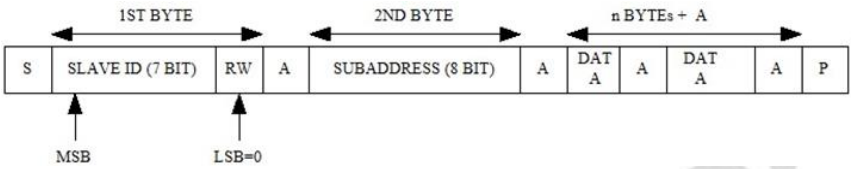


Fig.3.3 Master-transmitter transmits to slave-receiver

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (**PS5220**) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the **PS5220** acknowledgment, the master places the 8 bits data on SDA line and transmit to **PS5220** control register (address was assigned by 2nd byte). After **PS5220** issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the **PS5220** sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside **PS5220** can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.

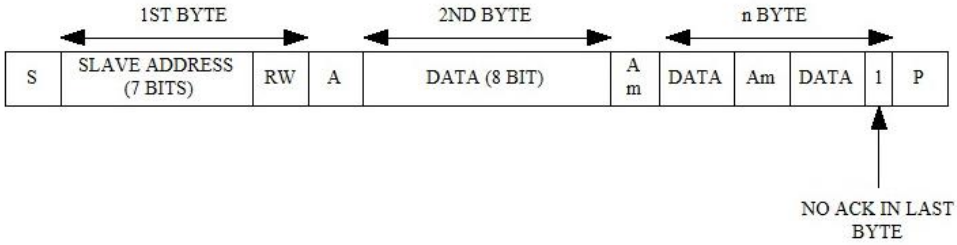


Fig.3.4 Slave-transmitter transmits to master-receiver

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by **PS5220**. The 8 bits data was read from **PS5220** internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the **PS5220** place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (**PS5220**) must releases SDA line to master to generate STOP condition.

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

I²C™ Bus Timing

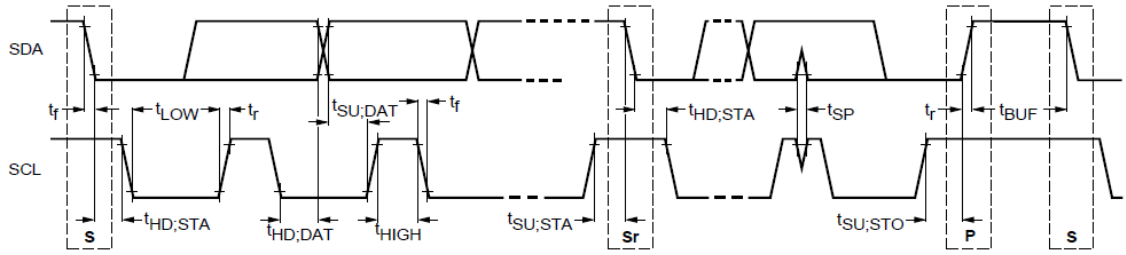


Fig.3.5 Definition of timing for F/S mode devices on the I2C-bus

I²C™ Bus Timing Specification				
Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	µs
High period of the SCL clock.	t_{HIGH}	0.75	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	µs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	µs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note: It depends on the “high” period time of SCL.

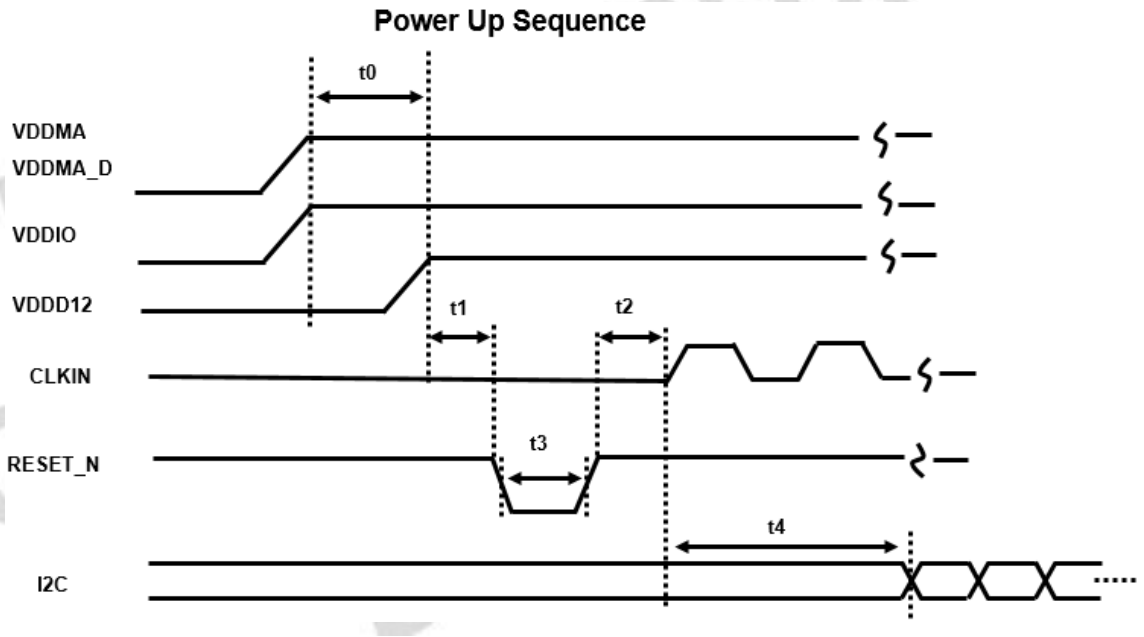
PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

4. Power Sequence

Power-Up Sequence

The recommended power-up sequence for the PS5220 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn on VDDMA, VDDMA_D and VDDIO power supply simultaneously.
2. After 100µs (t0), turn on VDDD12 power supply.
3. After 100µs (t1), RESET_N must go low.
4. RESET_N active low for at least 1ms (t3).
5. After 100µs (t2), enable CLKIN.
6. Wait at least 1ms (t4), I2C starts to write commands.



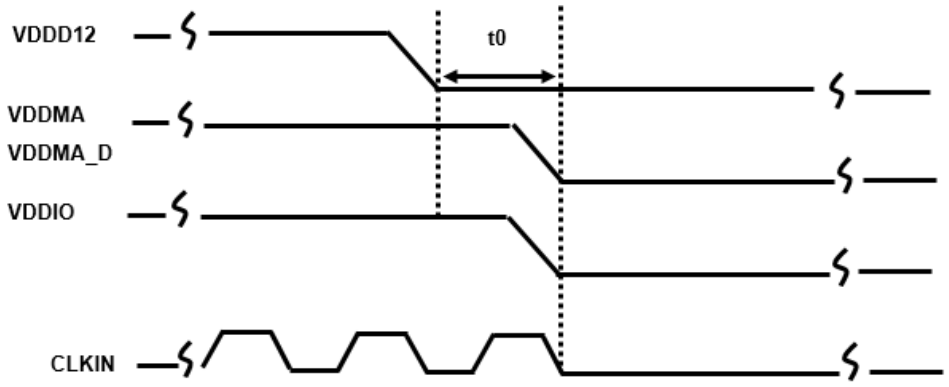
Power-Down Sequence

The recommended power-down sequence for the PS5220 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn off VDDD12 power supply.
2. After 100µs (t0), turn off VDDMA, VDDMA_D and VDDIO power supply simultaneously.

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

Power Down Sequence



CSB Suspend Sequence

The recommended CSB Suspend sequence for the PS5220 is shown as the following figure. The available power supplies must have the separation specified below.

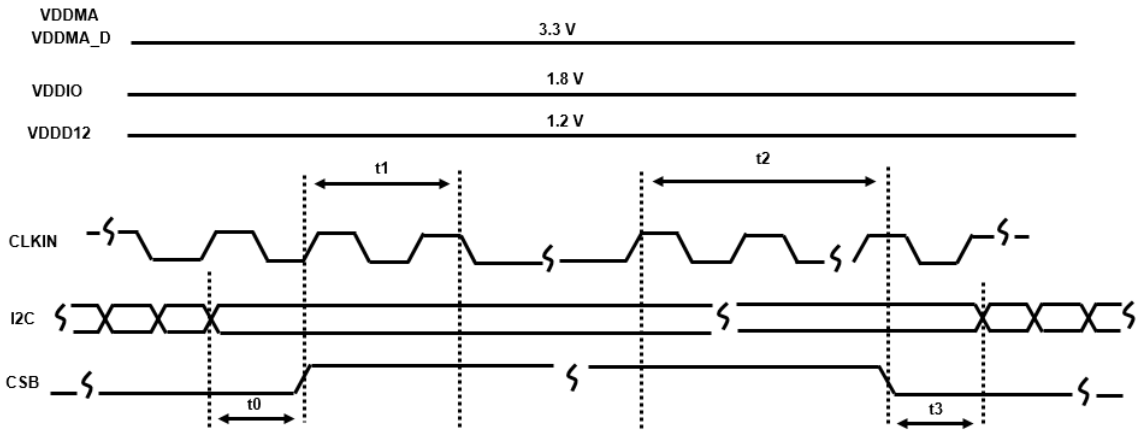
ON → OFF :

1. I2C must write commands to turn off internal clock for PS5220 .
2. After 100μs (t0), CSB must go high
3. After 100μs (t1), turn off CLKIN.

OFF → ON :

1. Turn on CLKIN.
2. After 100μs (t2), CSB must go low.
3. Wait at least 1ms (t3) for internal clock stable.
4. I2C starts to write commands.

CSB Suspend Sequence



PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

5. Register Table

Bank	Address		Bit	Name	R/W	Description
	Hex	Dec				
0	00	00	[7:0]	PartID[15:8]	R	Sensor ID
0	01	01	[7:0]	PartID[7:0]	R	Sensor ID
0	02	02	[3:0]	VersionID[3:0]	R	Sensor ID
0	03	03	[3:0]	SubID[3:0]	R	Sensor ID
0	11	17	[7]	Cmd_GatedAllClk	R/W	Clock Gated Control (1: Gate Clock)
0	BE	190	[6]	Cmd_Pxclk_Inv	R/W	Invert Pxclk Out
			[5]	Cmd_Vsync_Inv	R/W	Invert Vsync Out
			[4]	Cmd_Hsync_Inv	R/W	Invert Hsync Out
1	04	04	[6:4]	R_PxclkO_dly[2:0]	R/W	Timing Delay for Pxclk
			[2:0]	R_HsyncO_dly[2:0]	R/W	Timing Delay for Hsync
1	05	05	[6:4]	R_VsyncO_dly[2:0]	R/W	Timing Delay for Vsync
			[3]	Cmd_8_TriState	R/W	TriState IO of PxData[1:0]
			[2]	Cmd_Sw_PwrDn	R/W	Power-Down Control
			[1]	Cmd_Sw_TriState	R/W	TriState IO of PxData, Hsync, Vsync, and Pxclk
1	09	09	[0]	UpdateFlag	R/W	Exposure & Gain Update Control (Write 0x01)
1	0A	10	[7:0]	Cmd_Lpf[15:8]	R/W	Line per frame = Cmd_Lpf + 1
1	0B	11	[7:0]	Cmd_Lpf[7:0]	R/W	Line per frame = Cmd_Lpf + 1
1	0C	12	[7:0]	Cmd_OffNy1[15:8]	R/W	Exposure Control
1	0D	13	[7:0]	Cmd_OffNy1[7:0]	R/W	Exposure Control
1	0E	14	[3:0]	Cmd_OffNe1[11:8]	R/W	Exposure Control
1	0F	15	[7:0]	Cmd_OffNe1[7:0]	R/W	Exposure Control
1	1B	27	[7]	Cmd_Hflip	R/W	Horizontal Flip
			[6:5]	Cmd_Askip_H[1:0]	R/W	Horizontal Skip
			[2:0]	Cmd_Hsize_e1[10:8]	R/W	Raw Image Horizontal Size
1	1C	28	[7:0]	Cmd_Hsize_e1[7:0]	R/W	Raw Image Horizontal Size
1	1D	29	[7]	Cmd_Vflip	R/W	Vertical Flip
			[6:5]	Cmd_Askip_V[1:0]	R/W	Vertical Skip
			[2:0]	Cmd_Vsize[10:8]	R/W	Raw Image Vertical Size
1	1E	30	[7:0]	Cmd_Vsize[7:0]	R/W	Raw Image Vertical Size

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

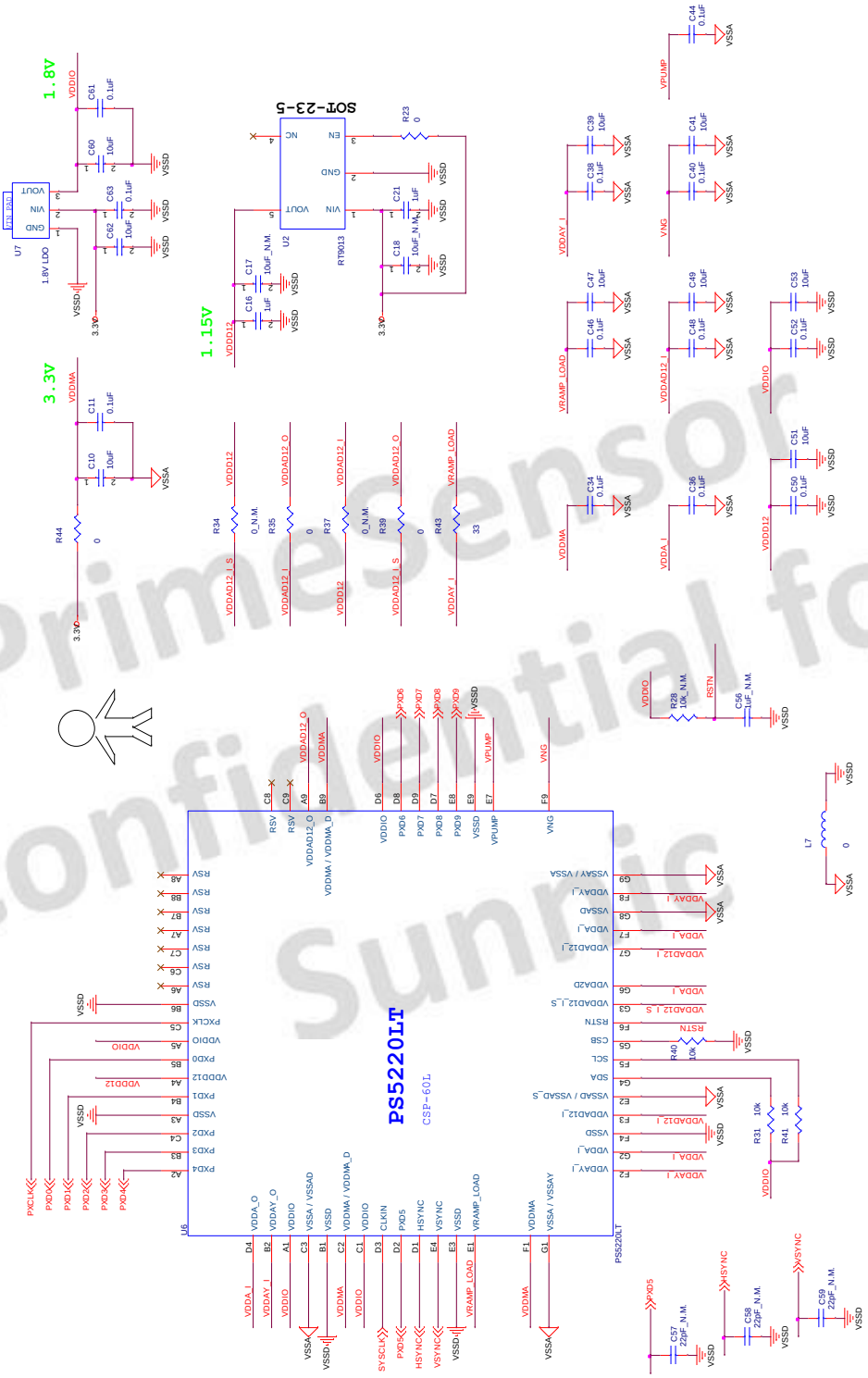
1	1F	31	[2:0]	Cmd_Vstart[10:8]	R/W	Raw Image Vertical Offset
1	20	32	[7:0]	Cmd_VStart[7:0]	R/W	Raw Image Vertical Offset
1	27	39	[4:0]	Cmd_LineTime[12:8]	R/W	Line Time = Cmd_LineTime clock cycles
1	28	40	[7:0]	Cmd_LineTime[7:0]	R/W	Line Time = Cmd_LineTime clock cycles
1	78	120	[4:0]	Cmd_GDAC[12:8]	R/W	Gain Control
1	79	121	[7:0]	Cmd_GDAC[7:0]	R/W	Gain Control
1	90	144	[1]	Cmd_ADC_Sample_Rotate	R/W	ADC sample order control
			[0]	Cmd_Adc_sample_posedge	R/W	ADC sample timing control
1	92	146	[4:0]	R_ISP_TestMode[4:0]	R/W	Test Image Control
1	93	147	[7:0]	R_ISP_TestValueLo[7:0]	R/W	Test Image Control
1	94	148	[7:0]	R_ISP_TestValueHi[7:0]	R/W	Test Image Control
1	91	151	[0]	Cmd_Pga_D1frm	R/W	Pga Gain auto-delay one frame
1	A3	163	[4]	Cmd_WOI_VOffset_sign	R/W	Vertical offset of output image
			[2:0]	Cmd_WOI_VOffset[10:8]	R/W	Vertical offset of output image
1	A4	164	[7:0]	Cmd_WOI_VOffset[7:0]	R/W	Vertical offset of output image
1	A5	165	[2:0]	Cmd_WOI_VSize[10:8]	R/W	Vertical size of output image
1	A6	166	[7:0]	Cmd_WOI_VSize[7:0]	R/W	Vertical size of output image
1	A7	167	[4]	Cmd_WOI_HOffset_sign	R/W	Horizontal offset of output image
			[2:0]	Cmd_WOI_HOffset[10:8]	R/W	Horizontal offset of output image
1	A8	168	[7:0]	Cmd_WOI_HOffset[7:0]	R/W	Horizontal offset of output image
1	A9	169	[2:0]	Cmd_WOI_HSize[10:8]	R/W	Horizontal size of output image
1	AA	170	[7:0]	Cmd_WOI_HSize[7:0]	R/W	Horizontal size of output image
1	AB	171	[5:0]	Cmd_Np[5:0]	R/W	Frequency eliminate control
1	E3	227	[5]	T_SR	R/W	IO slew control
			[1:0]	T_OPDRV[1:0]	R/W	IO driving Strength
1	E7	231	[7:6]	T_slew[1:0]	R/W	IO slew control
1	F1	241	[5:0]	T_spll_predivider[5:0]	R/W	PLL Control
1	F2	242	[5:0]	T_spll_postdivider [5:0]	R/W	PLL Control
1	F5	245	[1:0]	T_spll_modedivider [1:0]	R/W	PLL Control
2	46	70	[7]	Cmd_DigDac_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	47	71	[7:0]	Cmd_DigDac_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	48	72	[7]	Cmd_DigDac_Gb_Sign	R/W	Black Level Offset for Gb Channel

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

			[2:0]	Cmd_DigDac_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel
2	49	73	[7:0]	Cmd_DigDac_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	4A	74	[7]	Cmd_DigDac_Gr_Sign	R/W	Black Level Offset for Gr Channel
			[2:0]	Cmd_DigDac_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	4B	75	[7:0]	Cmd_DigDac_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	4C	76	[7]	Cmd_DigDac_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	4D	77	[7:0]	Cmd_DigDac_R_Offset[7:0]	R/W	Black Level Offset for R Channel

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

6. Reference Circuit Schematic



PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

7. Package Information

- **Package Outline Dimension**

	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	7284	7259	7309
Package Body Dimension Y	B	5338	5313	5363
Package Height	C	810	750	870
Ball Height	C1	180	150	210
Package Body Thickness	C2	630	585	675
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	350	320	380
Total Pin Count	N	60		
Pin Count X axis	N1	9		
Pin Count Y axis	N2	7		
Pins Pitch X axis	J1	750		
Pins Pitch Y axis	J2	600		
	J4	750		
Edge to Pin Center Distance along X	S1	642	612	672
Edge to Pin Center Distance along Y	S2	569	539	599

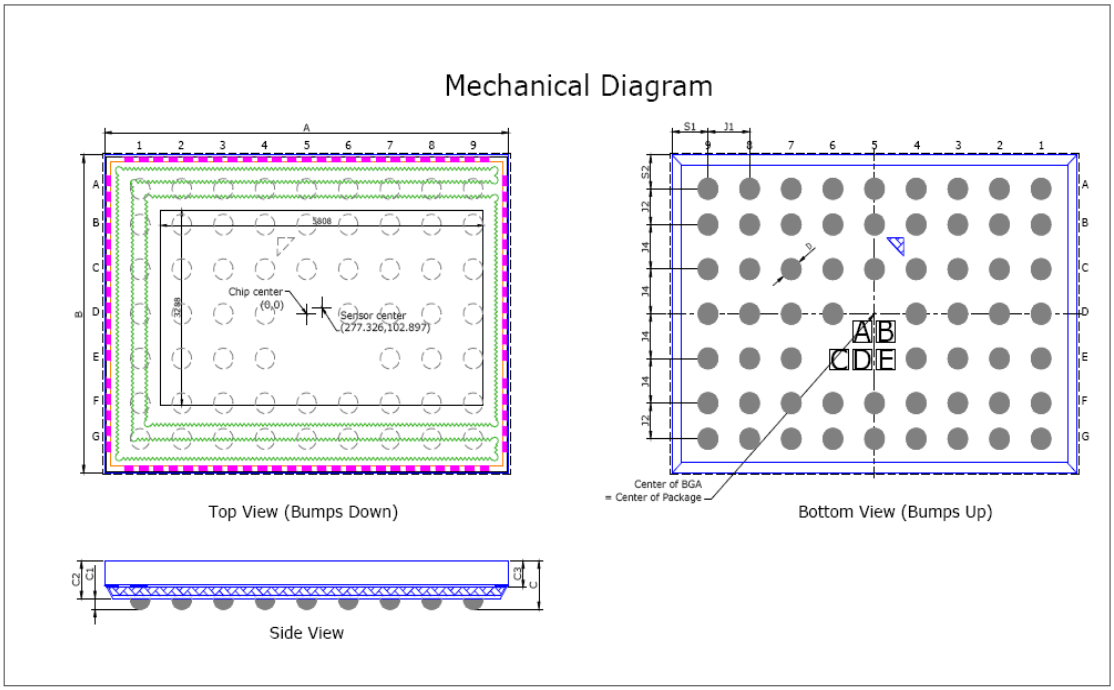
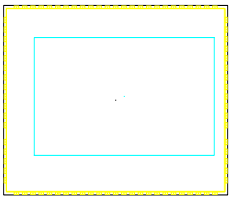
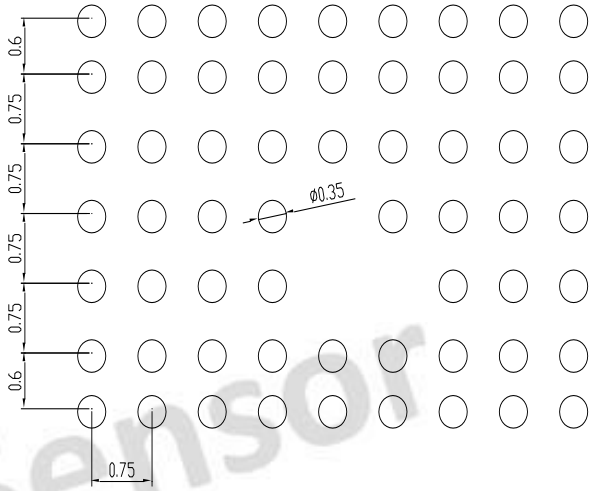


Figure. 1

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

- **Recommended PCB Layout**





Note :
1. All diemnsion is millimeter.
2. Top View

			原盛科技股份有限公司 PrimeSensor Technology Inc.		
			Title	PAS5220LT PCB layout	
			Part Number	PAS5220LT	
Rev.	Description	Date	Package Type	CSP 60B	
A	New Issue	07/08,14	P_Number	N/A	
B	Add VDDAD12_I_S Ball	12/15,14	Drawn	Masa Chang	Scale
C	Add VDDIO Ball	05/28,15	Check		Chip Size N/A
			Approve		Rev. B

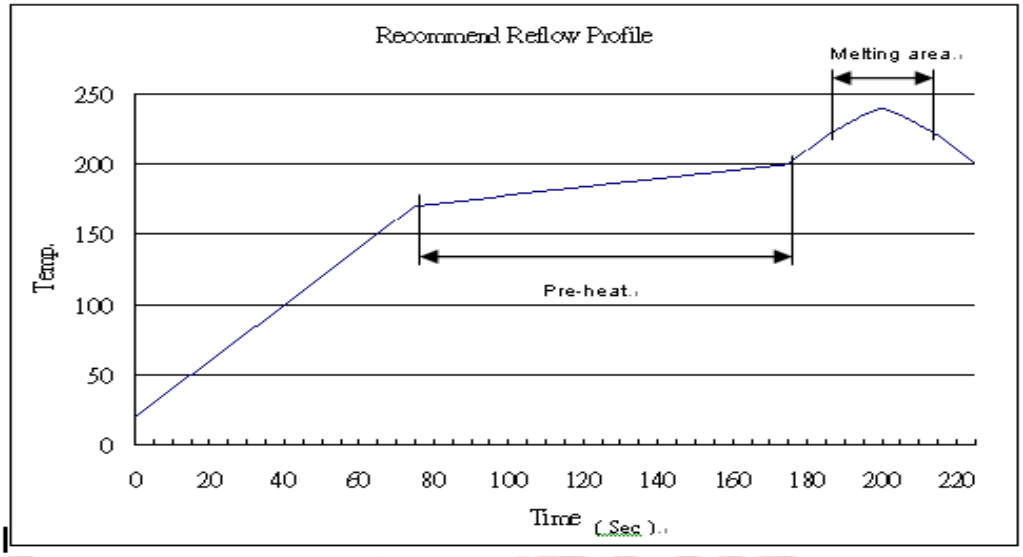
PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

- **Recommended Guideline for PCB Assembly**

I. Recommended vender and type for Pb-free solder paste
   1 Almit LFM-48W TM-HP
   2 Senju M705-GRN360-K

II. IR Reflow Soldering Profile:

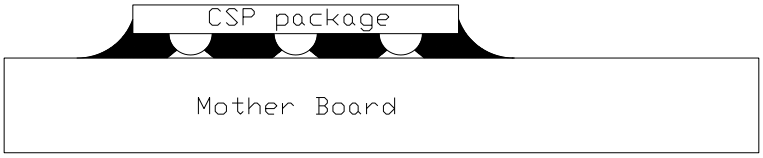
Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.



- **Reflow Profile**
  1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
  2. Preheat zone:
     2.1 Temp ramp from 170~ 200 degree C
     2.2 Exposure time: 90 +/- 30 sec
  3. Melting zone:
     3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
     3.2 Peak temperature: 245 degree C.

III. Others

- **Epoxy under-filled process is required post IC mounting process.**



- **Peek tweezers or plastic tweezers is required post IC manual handling for pick and place.**

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw

8. Revision History

Revision	Description	Date
V0.1	Preliminary data sheet release	Jan. 21, 2015
V0.2	Reference circuit schematic, register table update, package information	Jan. 30, 2015
V0.3	Update register table, spec.	Feb. 25, 2015
V0.4	Update CSP package information	May 26, 2015
V0.5	Update B1 pin assignment Update register table	Dec. 23, 2015
V0.6	Reference circuit schematic and digital core voltage	Feb. 25, 2016
V0.7	Add power sequence, update pin descriptions	Apr. 12, 2016
V0.8	Update sensor operating temperature specification	May 11, 2016

PrimeSensor Technology Inc.
E-mail: fae_service@primesensor.com.tw