

PS5280

DATA SHEET

PRELIMINARY

1/2" Full-HD 1080p HDR CMOS IMAGE SENSOR

Dec. 2017

Version 0.2

PS5280 Full-HD 1080p HDR CMOS IMAGE SENSOR

General Description

The **PS5280** is a low power, highly integrated CMOS image sensor that output of **1920x1080 (Full HD-1080p)** pixels with rolling shutter readout. It embedded the new FinePixel™ and HDR sensor technology to perform the excellent image quality and motion-blur-free high dynamic range output. **PS5280** outputs 12-bit compressed RGB raw data through a parallel digital video port or via serial MIPI interface through one-lane or dual-lane or quad-lane transmission. It is available in **PLCC** and **CSP** package.

The **PS5280** can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip black level correction and high temperature image quality control.

Features

- 1936 x 1096 pixels with Bayer-RGB color filter array and micro-lens
- Output format:
 - 12bit HDR Compressed RAW RGB
 - 12bit/10bit RAW RGB
- Output interface
 - 12bit parallel DVP output
 - quad lanes serial MIPI CSI2 output (up to 800Mbps per lane)
- On-chip column A/D converter
- On-chip manual analog gain control
- Continuous variable frame time & exposure time
- I2C™ Interface
- Automatic black-level calibration
- Black sun cancellation
- Support WOI and subsampling
- Support dummy line & pixel timing
- Support output Hsync at Vsync
- Support sensor frame synchronization
- Support motion detection mode
- On-chip PLL
(input_clock / PLL_m >= 1MHz)

Specifications

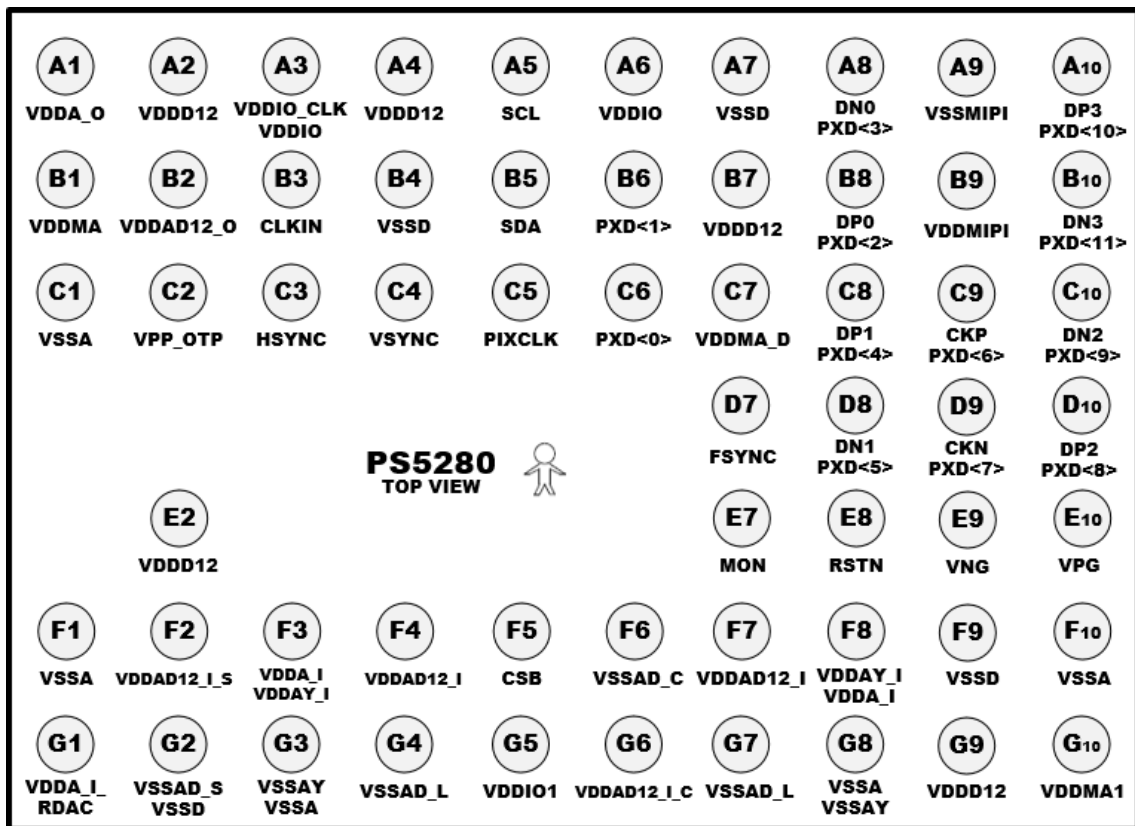
Parameter	Typical Value
Active array size	1936(H) x 1096(V)
Pixel size	4.0um (H) x 4.0um (V)
Shutter type	Electronic rolling shutter (ERS)
Optical format	1/2-inch
Lens chief ray angle	16 degree
ADC	12-bit
Sensitivity	10650 mV/Lux-sec
SNRmax	43.5 dB
Dynamic range	85 dB
Scan mode	Progressive scan
Input clock	Max 50MHz
Pixel clock	Max 148.5MHz
Max. frame rate	1080p: 1920x1080 @ 60fps 1080p: 1920x1080 HDR @ 30fps
Supply voltage	Analog: 3.3 V Digital: 1.2 V I/O: 1.8V / 3.3V
Power consumption	65 mW @ 1080p30 88 mW @ 1080p HDR 1080p30 (DVP with 1.8V I/O)
Operating temperature	-30°C ~ 85°C

Applications

- Surveillance HD-CCTV Camera
- Surveillance IP Camera
- Car Video Recorder
- Automotive Camera
- Video Door Phone
- Outdoor Camera w/o IR-LED

Ordering Information

Part Number	Description
PS5280PR	48-Pin PLCC, 11.43mmx11.43mm
PS5280LT	59-ball CSP

1. Pin Assignment


Pin No.	Name	Type	Description
A1	VDDA_O	Power	VDDA LDO output voltage(2.7-3.0V)
A2	VDDD12	Power	Digital power : 1.2V
A3	VDDIO	Power	I/O power : 1.8V ~ 3.3V
A4	VDDD12	Power	Digital power : 1.2V
A5	SCL	I/O	I2C clock, open drain type
A6	VDDIO	Power	I/O power : 1.8V ~ 3.3V
A7	VSSD	GND	Digital ground
A8	DN0_PXD<3>	Output	Pixel data output ; MIPI digital data output_3 negative terminal
A9	VSSMIPI	GND	Digital ground
A10	DP3_PXD<10>	Output	Pixel data output ; MIPI digital data output_3 positive terminal
B1	VDDMA	Power	Analog power : 3.3V
B2	VDDAD12_O	Power	Internal 1.2V LDO output voltage
B3	CLKIN	Input	Master clock input
B4	VSSD	GND	Digital ground
B5	SDA	I/O	I2C data, open drain type
B6	PXD<1>	Output	Pixel data output
B7	VDDD12	Power	Digital power : 1.2V

All rights strictly reserved any portion in this paper shall not be reproduced, copied or transformed to any other forms without permission.

B8	DP0_PXD<2>	Output	Pixel data output ; MIPI digital data output_0 positive terminal
B9	VDDMIPI	Power	MIPI VDD (1.2V)
B10	DN3_PXD<11>	Output	Pixel data output ; MIPI digital data output_3 negative terminal
C1	VSSA	GND	Analog Ground
C2	VPP_OTP	Power	External voltage for OTP device
C3	HSYNC	Output	Asserted when line data is valid
C4	VSYNC	Output	Asserted when frame data is valid
C5	PIXCLK	Output	Pixel clock output
C6	PXD<0>	Output	Pixel data output
C7	VDDMA_D	Power	Analog power : 3.3V
C8	DP1_PXD<4>	Output	Pixel data output ; MIPI digital data output_1 positive terminal
C9	CKP_PXD<6>	Output	Pixel data output ; MIPI output clock positive terminal
C10	DN2_PXD<9>	Output	Pixel data output ; MIPI digital data output_2 negative terminal
D7	FSYNC	Input	Frame sync signal
D8	DN1_PXD<5>	Output	Pixel data output ; MIPI digital data output_1 negative terminal
D9	CKN_PXD<7>	Output	Pixel data output ; MIPI output clock negative terminal
D10	DP2_PXD<8>	Output	Pixel data output ; MIPI digital data output_2 positive terminal
E2	VDDD12	Power	Digital power : 1.2V
E7	MON	Output	detection of motion signal
E8	RSTN	Input	Reset signal, active low, internal pull high
E9	VNG	Power	Reference voltage
E10	VPG	Power	Positive pump output voltage
F1	VSSA	Power	Analog Ground
F2	VDDAD12_I_S	Power	Analog power input voltage(1.2V)
F3	VDDA_I /VDDAY_I	Power	Analog power input voltage (2.7V ~ 3V)
F4	VDDAD12_I	Power	Analog power input voltage(1.2V)
F5	CSB	Input	Suspend control, "1" : suspend, "0" : normal function
F6	VSSAD_C	GND	Analog Ground
F7	VDDAD12_I	Power	Analog power input voltage(1.2V)
F8	VDDAY_I /VDDA_I	Power	Analog power input voltage (2.7V ~ 3V)
F9	VSSD	GND	Digital ground
F10	VSSA	GND	Analog Ground
G1	VDDAY_I_RDAC	Power	Analog power input voltage (2.7V ~ 3V)
G2	VSSAD_S /VSSD	GND	Analog Ground and Digital ground
G3	VSSAY /VSSA	GND	Analog Ground
G4	VSSAD_L	GND	Analog Ground
G5	VDDIO1	Power	I/O power : 1.8V ~ 3.3V
G6	VDDAD12_I_C	Power	Analog power input voltage(1.2V)

G7	VSSAD_L	GND	Analog Ground
G8	VSSA /VSSAY	GND	Analog Ground
G9	VDDD12	Power	Digital power : 1.2V
G10	VDDMA1	Power	Analog power : 3.3V

PrimeSensor
Confidential for
GlobalizeX

2. Specifications

Absolute Maximum Ratings					
Operating Temperature (sensor junction temperature)		-30°C ~ 85°C			
Ambient Storage Temperature		-40°C ~ 125°C			
Supply Voltage (with respect to ground)	V _{DDA}	4.5V			
	V _{DDD}	3.0V			
	V _{DDIO}	4.5V			
All Input / Output Voltage (with respect to ground)		-0.3V to V _{DDIO} + 0.5V			
Lead-free temperature, Surface-mount process		245°C			
ESD rating, Human Body model		2000V			
DC Electrical Characteristics (Ta = -30°C ~ 85°C)					
Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V _{DDA}	DC supply voltage – Analog	3.14	3.3	3.47	V
V _{DDD}	DC supply voltage – Digital core	1.1	1.2	1.3	V
V _{DDIO}	DC supply voltage – I/O	1.7	1.8	3.47	V
Type : IN & I/O					
V _{IH}	Input Voltage HIGH	V _{DDIO} * 0.7			V
V _{IL}	Input Voltage LOW			V _{DDIO} * 0.3	V
Type : OUT & I/O					
V _{OH}	Output Voltage HIGH	V _{DDIO} * 0.9			V
V _{OL}	Output Voltage LOW			V _{DDIO} * 0.1	V
AC Operating Condition					
Symbol	Parameter	Min.	Typ.	Max.	Unit
f _{sysclk}	System clock frequency		TBD		MHz
t _{sysclk_dc}	System clock duty cycle	45		55	%
Sensor Characteristics					
Parameter		Typ.		Unit	
Sensitivity		TBD		mV/Lux-Sec	
Maximum Signal to Noise Ratio		TBD		dB	
Dynamic Range		TBD		dB	

†: Sensor function works in the ambient operating temperature range. However, the image quality may change at high temperature condition.

†: The power consumption is measured with 4X analog gain.

3. I²C™ Bus

PS5280 supports I²C bus transfer protocol and acts as slave device. The 7-bits unique slave address is “1001000” and supports receiving / transmitting speed as maximum 400 kHz.

I²C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiate a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 3.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 3.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

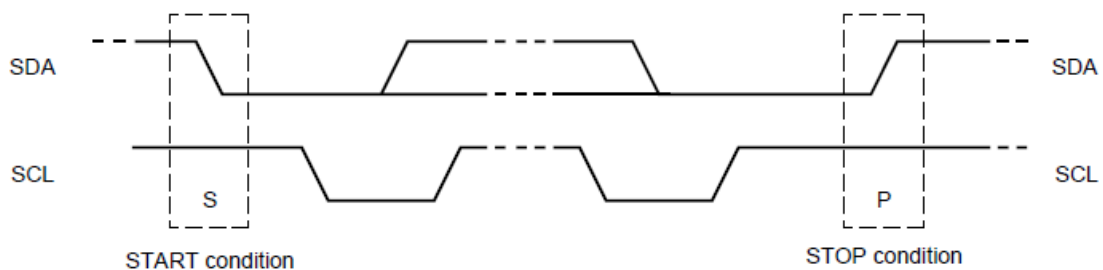


Fig.3.1 Start and Stop Condition

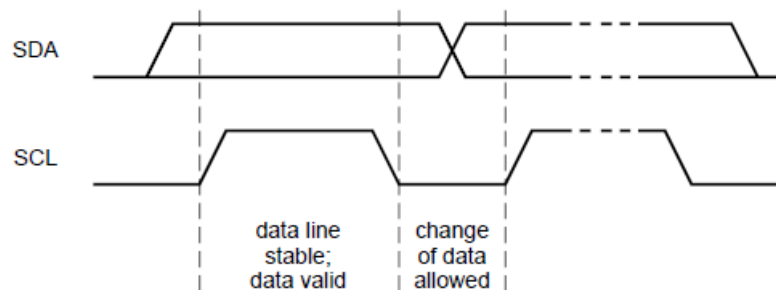


Fig.3.2 Valid Data

Data Transfer Format

Master transmits data to slave (write cycle)

- S : Start.
- A : Acknowledge by slave.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle.
RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of **PS5280** internal control registers. (Please refer to **PS5280** register description)

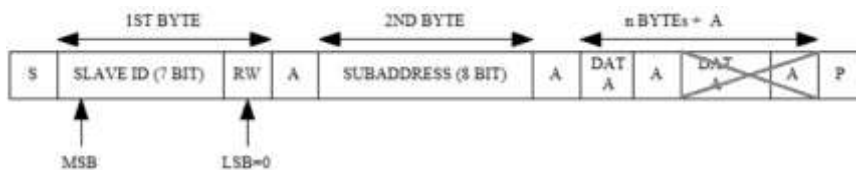


Fig.3.3 Master-transmitter transmits to slave-receiver

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (**PS5280**) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the **PS5280** acknowledgment, the master places the 8 bits data on SDA line and transmit to **PS5280** control register (address was assigned by 2nd byte). After **PS5280** issues acknowledgment, the master can generate a stop condition to end of this write cycle. Every control registers value inside **PS5280** can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.

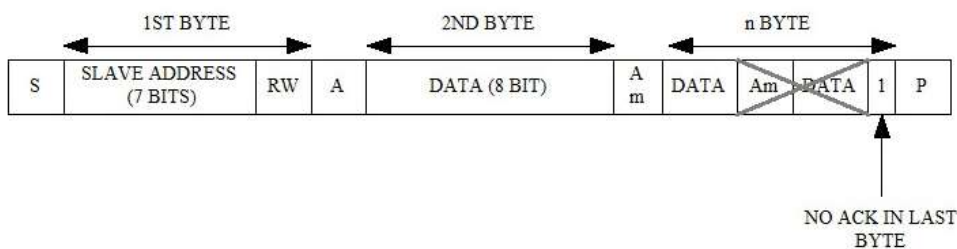


Fig.3.4 Slave-transmitter transmits to master-receiver

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by **PS5280**. The 8 bits data was read from **PS5280** internal control register that address was assigned by previous write cycle. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (**PS5280**) must releases SDA line to master to generate STOP condition.

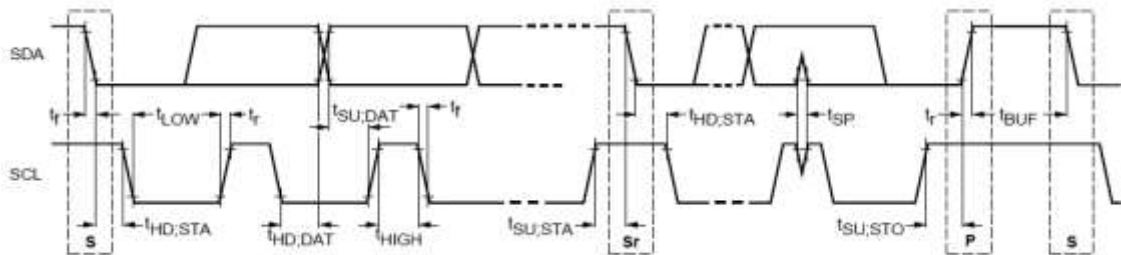
I²C™ Bus Timing


Fig.3.5 Definition of timing for F/S mode devices on the I2C-bus

I ² C™ Bus Timing Specification						
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency.	f_{scl}	10	100	0	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD,STA}$	4.0	-	0.6	-	μ s
Low period of the SCL clock.	t_{LOW}	4.7	-	1.3	-	μ s
High period of the SCL clock.	t_{HIGH}	4.0	-	0.6	-	μ s
Set-up time for a repeated START condition.	$t_{SU,STA}$	4.7	-	0.6	-	μ s
Data hold time. For I2C-bus device.	$t_{HD,DAT}$	5.0	3.45	0	0.9	μ s
Data set-up time.	$t_{SU,DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals.	t_r	-	1000	$20+0.1 C_b$	300	ns (note 1)
Fall time of both SDA and SCL signals.	t_f	-	300	$20+0.1 C_b$	300	ns (note 1)
Set-up time for STOP condition.	$t_{SU,STO}$	4.0	-	0.6	-	μ s
Bus free time between a STOP and START.	t_{BUF}	4.7	-	1.3	-	μ s
Capacitive load for each bus line.	C_b	-	400	-	400	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	-	0.1 VDD	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	-	0.2 VDD	V

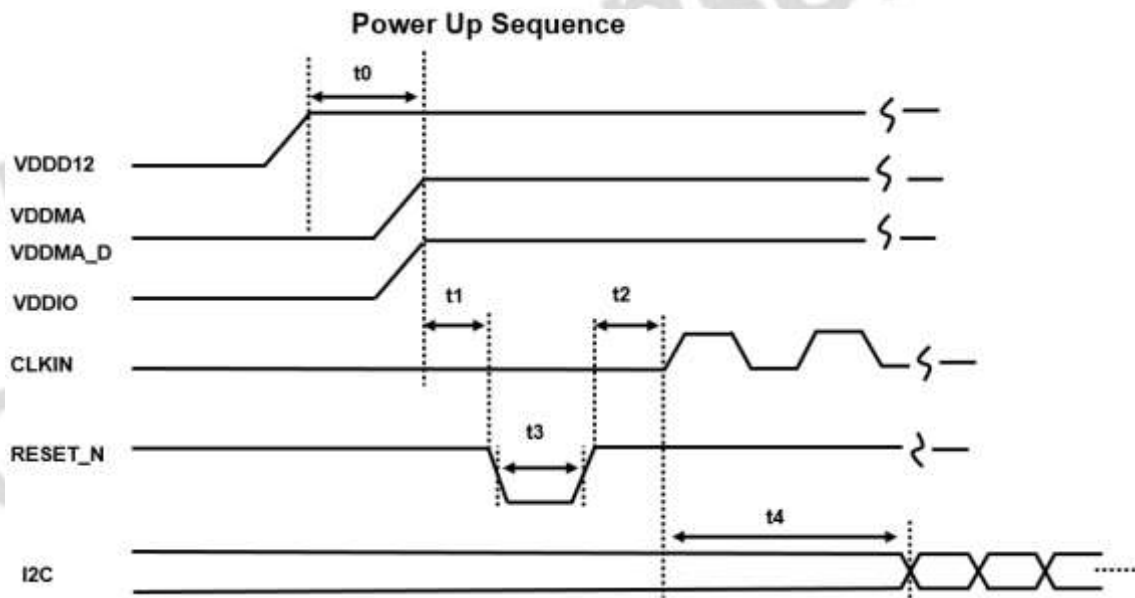
Note: It depends on the "high" period time of SCL.

4. Power Sequence

Power-Up Sequence

The recommended power-up sequence for the PS5280 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn on VDDD12 power supply.
2. After 100 μ s (t_0), VDDMA, VDDMA_D and VDDIO power supply simultaneously.
3. After 100 μ s (t_1), RESET_N must go low.
4. RESET_N active low for at least 1ms (t_3).
5. After 100 μ s (t_2), enable CLKIN.
6. Wait at least 1ms (t_4), I2C starts to write commands.

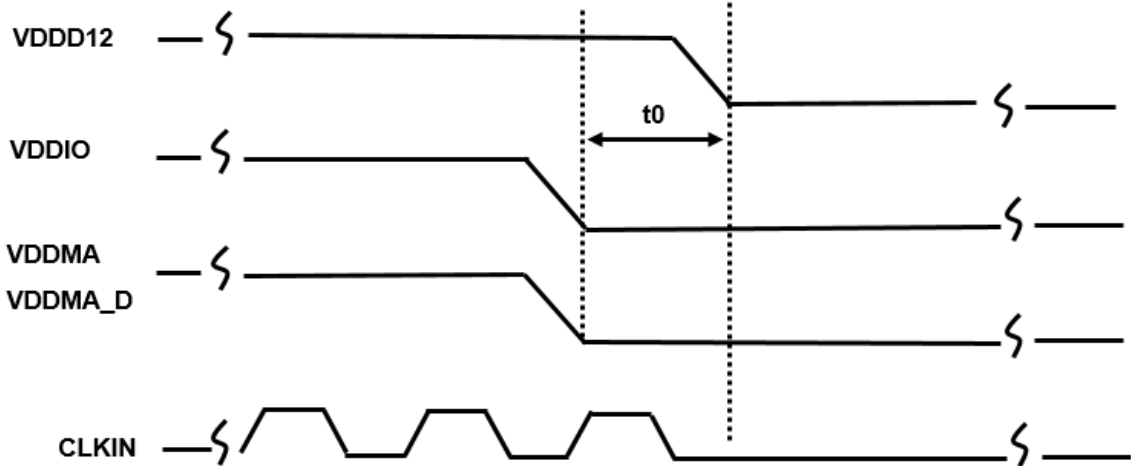


Power-Down Sequence

The recommended power-down sequence for the PS5280 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn off VDDMA, VDDMA_D and VDDIO power supply simultaneously.
2. After 100 μ s (t_0), turn off VDDD12 power supply.

Power Down Sequence



CSB Suspend Sequence

The recommended CSB Suspend sequence for the PS5280 is shown as the following figure. The available power supplies must have the separation specified below.

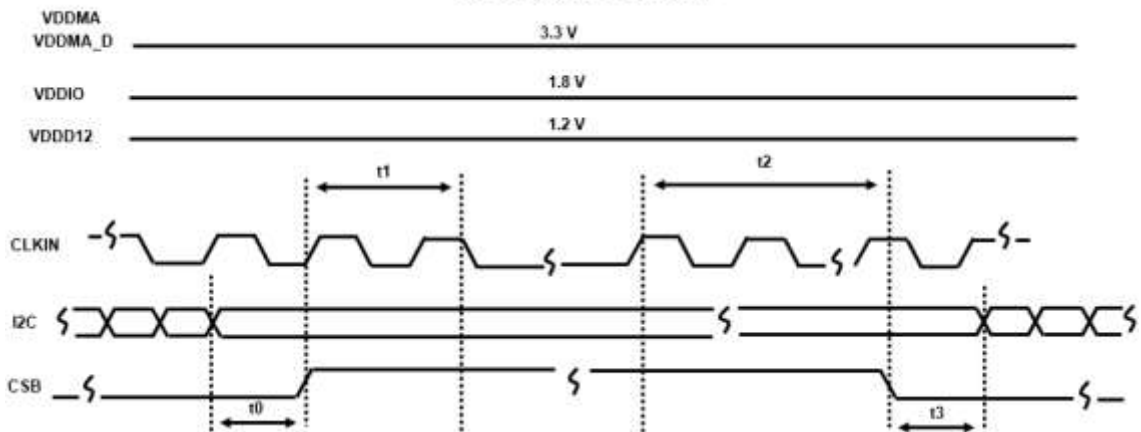
ON → OFF :

1. I2C must write commands to turn off internal clock for PS5280 .
2. After $100\mu\text{s}$ (t_0), CSB must go high
3. After $100\mu\text{s}$ (t_1), turn off CLKIN.

OFF → ON :

1. Turn on CLKIN.
2. After $100\mu\text{s}$ (t_2), CSB must go low.
3. Wait at least 1ms (t_3) for internal clock stable.
4. I2C starts to write commands.

CSB Suspend Sequence



5. Register Table

Bank	Address		Bit	Name	R/W	Description
	Hex	Dec				
0	00	00	[7:0]	PartID[15:8]	R	Sensor ID
0	01	01	[7:0]	PartID[7:0]	R	Sensor ID
0	02	02	[3:0]	VersionID[3:0]	R	Sensor ID
0	03	03	[3:0]	SubID[3:0]	R	Sensor ID
0	11	17	[7]	Cmd_GatedAllClk	R/W	Clock Gated Control (1: Gate Clock)
0	BE	190	[6]	Cmd_Pxclk_Inv	R/W	Invert Pxclk Out
			[5]	Cmd_Vsync_Inv	R/W	Invert Vsync Out
			[4]	Cmd_Hsync_Inv	R/W	Invert Hsync Out
1	04	04	[6:4]	R_PxclkO_dly[2:0]	R/W	Timing Delay for Pxclk
			[2:0]	R_HsyncO_dly[2:0]	R/W	Timing Delay for Hsync
1	05	05	[6:4]	R_VsyncO_dly[2:0]	R/W	Timing Delay for Vsync
			[3]	Cmd_8_TriState	R/W	TriState IO of PxData[1:0]
			[2]	Cmd_Sw_PwrDn	R/W	Power-Down Control
			[1]	Cmd_Sw_TriState	R/W	TriState IO of PxData, Hsync, Vsync, and Pxclk
1	09	09	[0]	UpdateFlag	R/W	Exposure & Gain Update Control (Write 0x01)
1	0A	10	[7:0]	Lpf1[15:8]	R/W	Line per frame = Lpf1 + 1
1	0B	11	[7:0]	Lpf1[7:0]	R/W	Line per frame = Lpf1 + 1
1	0C	12	[7:0]	Cmd_OffNy1[15:8]	R/W	Exposure Control
1	0D	13	[7:0]	Cmd_OffNy1[7:0]	R/W	Exposure Control
1	0E	14	[4:0]	Cmd_OffNe1[12:8]	R/W	Exposure Control
1	0F	15	[7:0]	Cmd_OffNe1[7:0]	R/W	Exposure Control
1	18	24	[0]	Cmd_SGHD	R/W	High/Low Sensitivity Selection : 0: High Sensitivity Mode 1: Low Sensitivity Mode
1	1B	27	[7]	Cmd_Hflip	R/W	Horizontal Flip
			[6:5]	Cmd_Askip_H[1:0]	R/W	Horizontal Skip
			[2:0]	Cmd_Hsize_e1[10:8]	R/W	Raw Image Horizontal Size
1	1C	28	[7:0]	Cmd_Hsize_e1[7:0]	R/W	Raw Image Horizontal Size
1	1D	29	[7]	Cmd_Vflip	R/W	Vertical Flip
			[6:5]	Cmd_Askip_V[1:0]	R/W	Vertical Skip

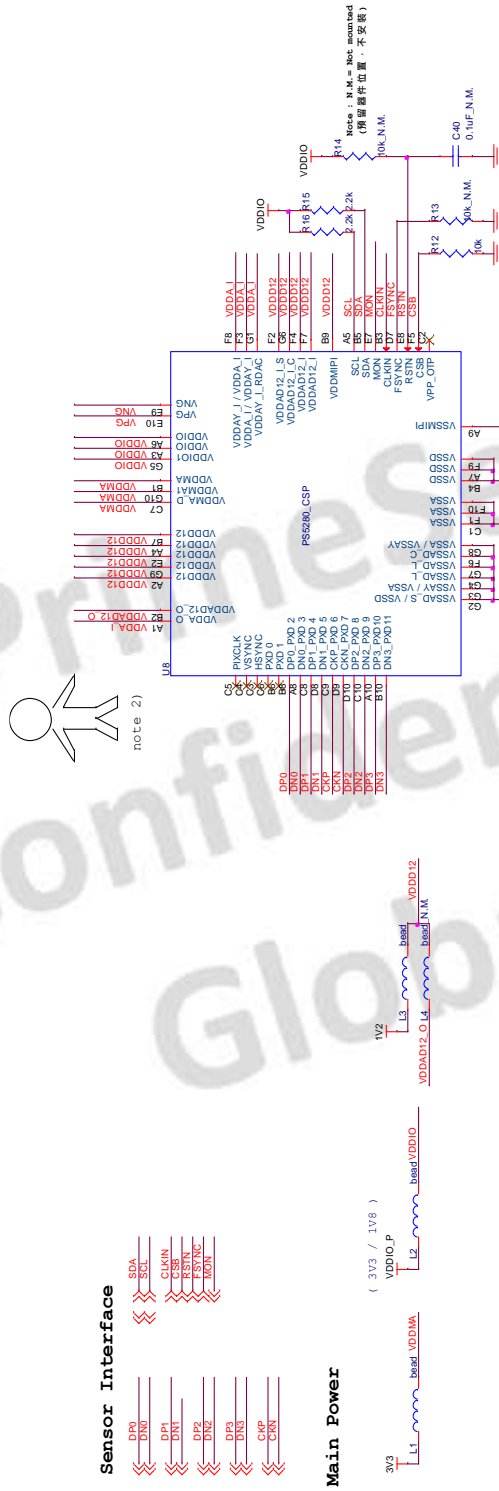
			[2:0]	Cmd_Vsize[10:8]	R/W	Raw Image Vertical Size
1	1E	30	[7:0]	Cmd_Vsize[7:0]	R/W	Raw Image Vertical Size
1	1F	31	[2:0]	Cmd_Vstart[10:8]	R/W	Raw Image Vertical Offset
1	20	32	[7:0]	Cmd_VStart[7:0]	R/W	Raw Image Vertical Offset
1	27	39	[4:0]	LineTime1[12:8]	R/W	Line Time = LineTime1 * 0.5 clock cycles
1	28	40	[7:0]	LineTime1[7:0]	R/W	Line Time = LineTime1 * 0.5 clock cycles
1	83	131	[7:0]	Cmd_gain_idx[7:0]	R/W	Sensor Analog Gain index
1	8F	143	[2]	Cmd_ImgSyn_Mode	R/W	HDR Image Mode : 0: anglog nonHDR-mode 1: analog HDR-mode
			[0]	Cmd_ImgSyn_EnH	R/W	HDR Image Synthesis Enable
1	90	144	[0]	Cmd_Adc_sample_posedge	R/W	ADC sample timing control
1	92	146	[4:0]	R_ISP_TestMode[4:0]	R/W	Test Image Control
1	93	147	[7:0]	R_ISP_TestValueLo[7:0]	R/W	Test Image Control
1	94	148	[7:0]	R_ISP_TestValueHi[7:0]	R/W	Test Image Control
1	97	151	[0]	Cmd_Pga_D1frm	R/W	Pga Gain auto-delay one frame
1	A3	163	[4]	Cmd_WOI_VOffset_sign	R/W	Vertical offset of output image
			[2:0]	Cmd_WOI_VOffset[10:8]	R/W	Vertical offset of output image
1	A4	164	[7:0]	Cmd_WOI_VOffset[7:0]	R/W	Vertical offset of output image
1	A5	165	[2:0]	Cmd_WOI_VSize[10:8]	R/W	Vertical size of output image
1	A6	166	[7:0]	Cmd_WOI_VSize[7:0]	R/W	Vertical size of output image
1	A7	167	[4]	Cmd_WOI_HOffset_sign	R/W	Horizontal offset of output image
			[2:0]	Cmd_WOI_HOffset[10:8]	R/W	Horizontal offset of output image
1	A8	168	[7:0]	Cmd_WOI_HOffset[7:0]	R/W	Horizontal offset of output image
1	A9	169	[2:0]	Cmd_WOI_HSize[10:8]	R/W	Horizontal size of output image
1	AA	170	[7:0]	Cmd_WOI_HSize[7:0]	R/W	Horizontal size of output image
1	AB	171	[3:0]	Cmd_Np[3:0]	R/W	Frequency eliminate control
1	E3	227	[5]	T_SR_GPIO	R/W	IO slew control
			[1:0]	T_OPDRV[1:0]	R/W	IO driving Strength
1	F1	241	[5:0]	T_spll_predivider[5:0]	R/W	PLL Control
1	F2	242	[5:0]	T_spll_postdivider [5:0]	R/W	PLL Control
1	F5	245	[1:0]	T_spll_modedivider [1:0]	R/W	PLL Control
2	10	16	[1]	R_FrameSyncWait	R/W	0: Continuous output after one pulse trigger signal. 1: One frame output after one pulse trigger signal.

			[0]	R_FrameSyncMode	R/W	0: Normal Mode. 1: Frame Sync Mode.
2	46	70	[7]	Cmd_DigDac_B_Sign	R/W	Black Level Offset for B Channel
			[4:0]	Cmd_DigDac_B_Offset[12:8]	R/W	Black Level Offset for B Channel
2	47	71	[7:0]	Cmd_DigDac_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	48	72	[7]	Cmd_DigDac_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[4:0]	Cmd_DigDac_Gb_Offset[12:8]	R/W	Black Level Offset for Gb Channel
2	49	73	[7:0]	Cmd_DigDac_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	4A	74	[7]	Cmd_DigDac_Gr_Sign	R/W	Black Level Offset for Gr Channel
			[4:0]	Cmd_DigDac_Gr_Offset[12:8]	R/W	Black Level Offset for Gr Channel
2	4B	75	[7:0]	Cmd_DigDac_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	4C	76	[7]	Cmd_DigDac_R_Sign	R/W	Black Level Offset for R Channel
			[4:0]	Cmd_DigDac_R_Offset[12:8]	R/W	Black Level Offset for R Channel
2	4D	77	[7:0]	Cmd_DigDac_R_Offset[7:0]	R/W	Black Level Offset for R Channel

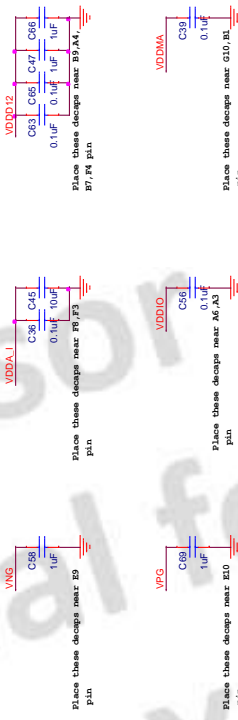
PrimeSensor
Confidential for
GlobalizeX

6. Reference Circuit Schematic

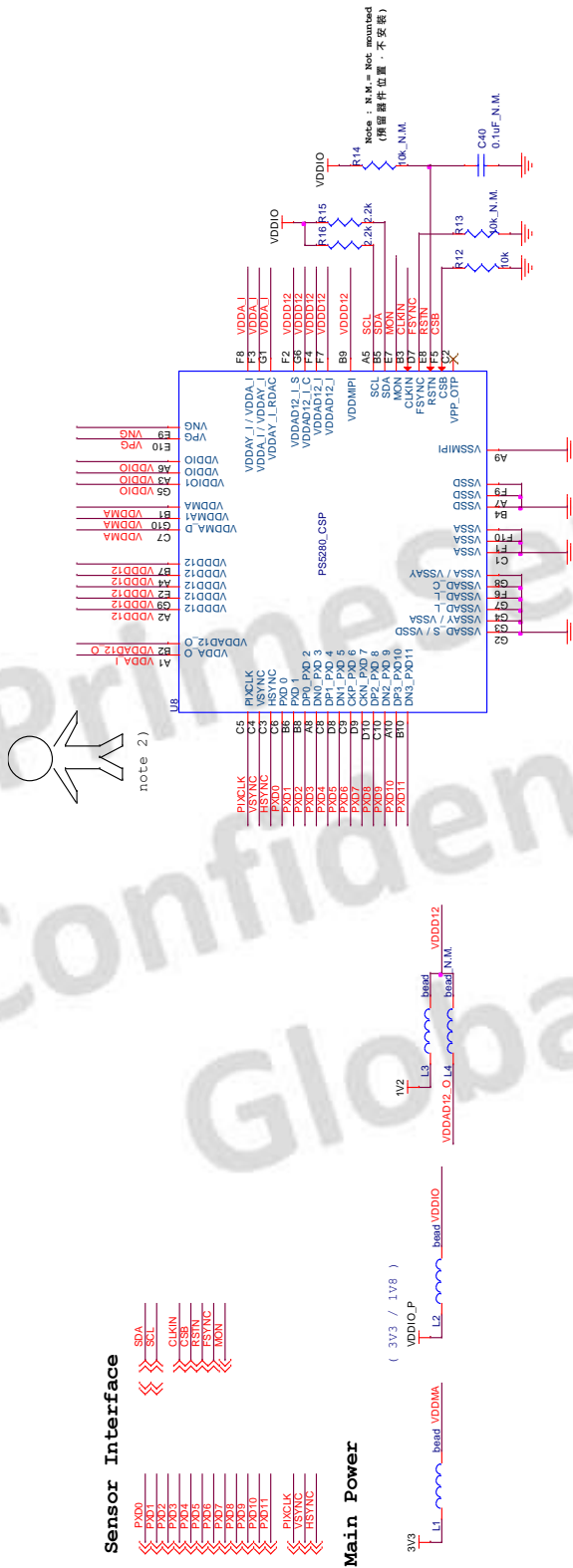
MIPI Interface:



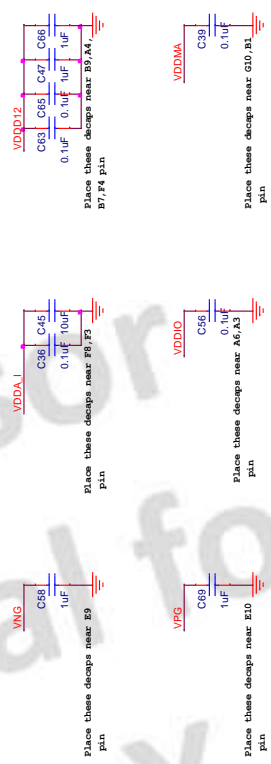
Bypass caps should be placed as close to the power pins as possible



Parallel Interface:



Bypass caps should be placed as close to the power pins as possible



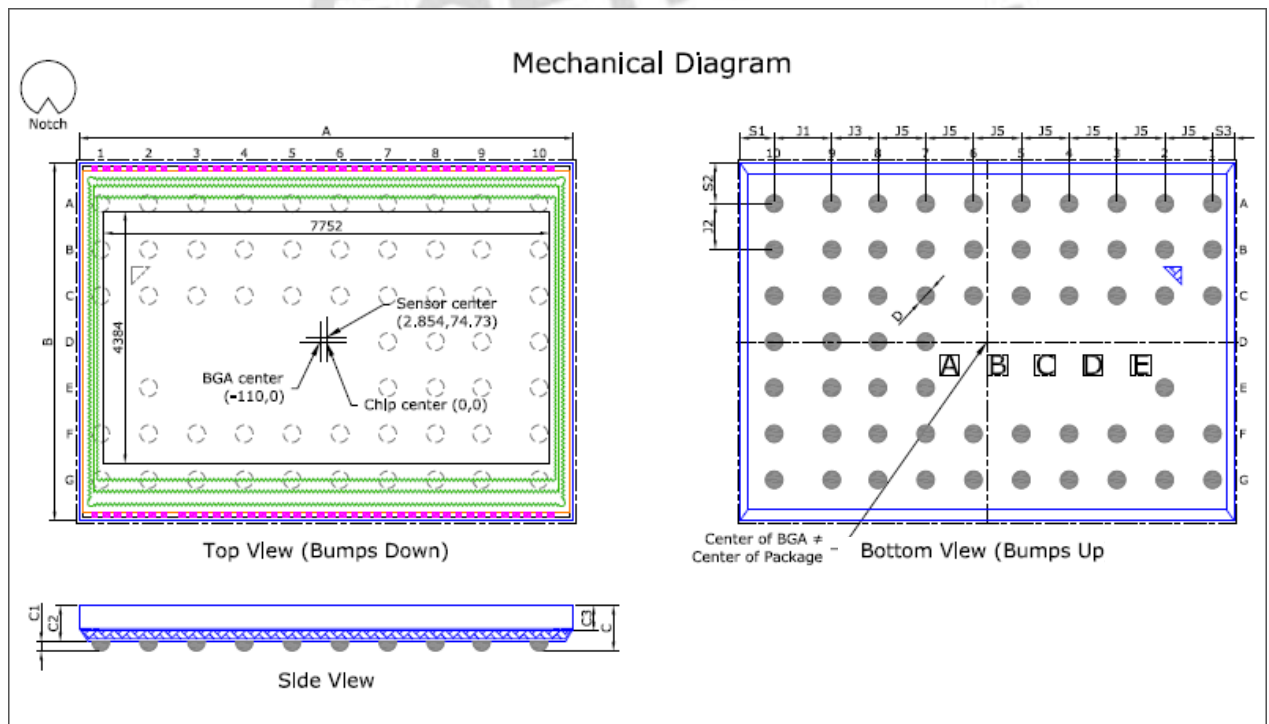
Confidential for GlobalizeX

7. Package Information

- Package Outline Dimension

	Symbol	Nominal	Min.	Max.
			μm	
Package Body Dimension X	A	8586	8561	8611
Package Body Dimension Y	B	6226	6201	6251
Package Height	C	790	730	850
Ball Height	C1	160	130	190
Package Body Thickness	C2	630	585	675
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	300	270	330
Total Pin Count	N	59		
Pin Count X axis	N1	10		
Pin Count Y axis	N2	7		
Pins Pitch X axis	J1	1000		
	J3	800		
	J5	830		
Pins Pitch Y axis	J2	800		
Edge to Pin Center Distance along X	S1	598	568	628
	S3	378	348	408
Edge to Pin Center Distance along Y	S2	713	683	743

- * 1. The thickness of Bond-1 glass is 400 μm (Green glass x 1pcs).
- * 2. The material of solder printing is SAC305.



- Recommended PCB Layout

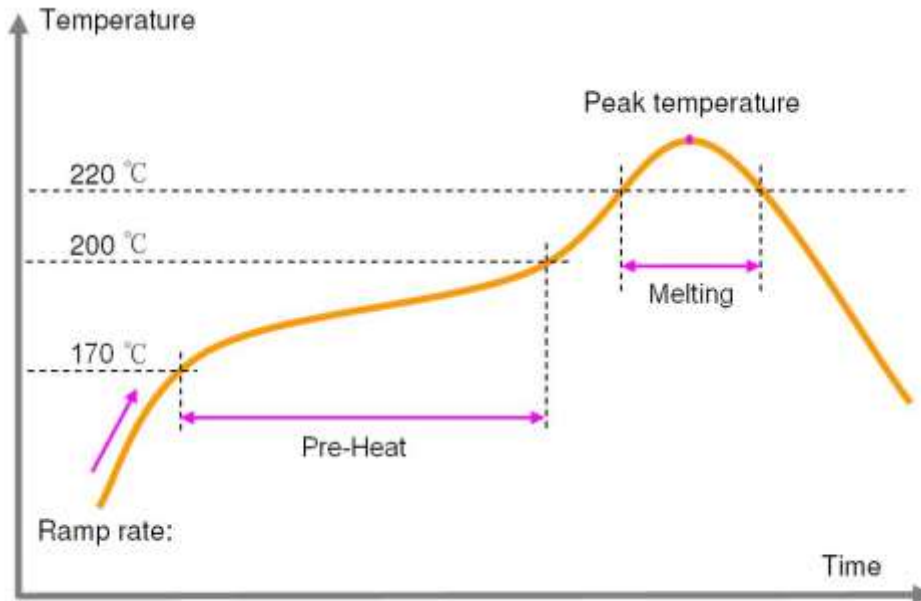
PrimeSensor
Confidential for
GlobalizeX

- **Recommended Guideline for PCB Assembly**

- I. Recommended vender and type for Pb-free solder paste
 - 1 Almit LFM-48W TM-HP
 - 2 Senju M705-GRN360-K

- II. IR Reflow Soldering Profile:

Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.

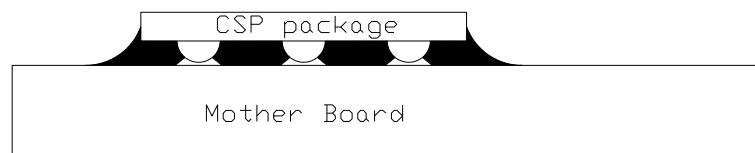


- **Reflow Profile**

1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
2. Preheat zone:
 - 2.1 Temp ramp from 170~ 200 degree C
 - 2.2 Exposure time: 90 +/- 30 sec
3. Melting zone:
 - 3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
 - 3.2 Peak temperature: 245 degree C.

- III. Others

- **Epoxy under-filled process is required post IC mounting process.**



- **Peek tweezers or plastic tweezers is required post IC manual handling for pick and place.**



8. Revision History

Revision	Description	Date
V0.1	Preliminary data sheet release	Dec. 09, 2017
V0.2	Update specifications and reference circuit schematics	Dec. 26, 2017

PrimeSensor
Confidential for
GlobalizeX