原盛科技股份有限公司
PrimeSensor Technology Inc.

PS5270
DATA SHEET

PRELIMINARY

1/2.4” 2.38MP CMOS IMAGE SENSOR

Aug. 2017

Version 0.3

PS5270 2.38M PANORAMIC CMOS IMAGE SENSOR

General Description

The **PS5270** is a highly integrated CMOS image sensor that output of **1544x1544 (2.38MP 1:1)** pixels with rolling shutter readout. It embedded the new FinePixel™ sensor technology and superior HDR processing to capture the excellent image quality. **PS5270** outputs 14-bit RGB raw data through DVP and MIPI CSI-2 interface. It is well suited for panoramic camera application

The **PS5270** can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **1544 x 1544 pixels with Bayer-RGB color filter array and micro-lens**
- **Output format:**
  - 14-bit RAW RGB
- **Output interface**
  - 14bit parallel DVP output
  - Dual-lane MIPI-CSI2 output (up to 800Mbps per lane)
- **On-chip column A/D converter**
- **On-chip manual analog gain control**
- **Continuous variable frame time & exposure time**
- **I2C™ Interface**
- **High dynamic range (Support On/Off fast switch)**
- **Support frame synchronization**
- **Automatic black-level calibration**
- **Black sun cancellation**
- **Programmable fast-switch configuration**
- **Support WOI and subsampling**
- **Support dummy line & pixel timing**
- **Support output Hsync at Vsync**
- **Support 1.7V~3.3V I/O**
- **On-chip PLL (input_clock / PLL_m >= 1MHz)**

Specifications

Parameter	Typical Value
Active array size	1544(H) x 1544(V)
Pixel size	3.4um (H) x 3.4um (V)
Shutter type	Electronic rolling shutter (ERS)
Optical format	1408x1408 @1/2.7-inch 1536x1536 @1/2.4-inch
Lens chief ray angle	22 degree
ADC	14-bit
Sensitivity	6500 mV/Lux-sec
SNRmax	42.5 dB
Dynamic range	81 dB
Scan mode	Progressive scan
Input clock	Max 64MHz
Pixel clock	Max 81MHz
Max. frame rate	1536x1536 @30fps 1280x1280 @30fps 1024x1024 @45fps
Supply voltage	Analog: 3.3 V Digital: 1.2 V I/O: 1.7V~3.3V
Power consumption	138mW
Operating temperature	-40ºC ~ 85ºC

Applications

- **180/360/720 Panoramic Camera**
- **Surveillance IP Camera**
- **Surveillance HD-CCTV Camera**
- **Automotive applications**
- **Video Door Phone**

Ordering Information

Part Number	Description
PS5270LT	61-Ball CSP

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1. Pin Assignment

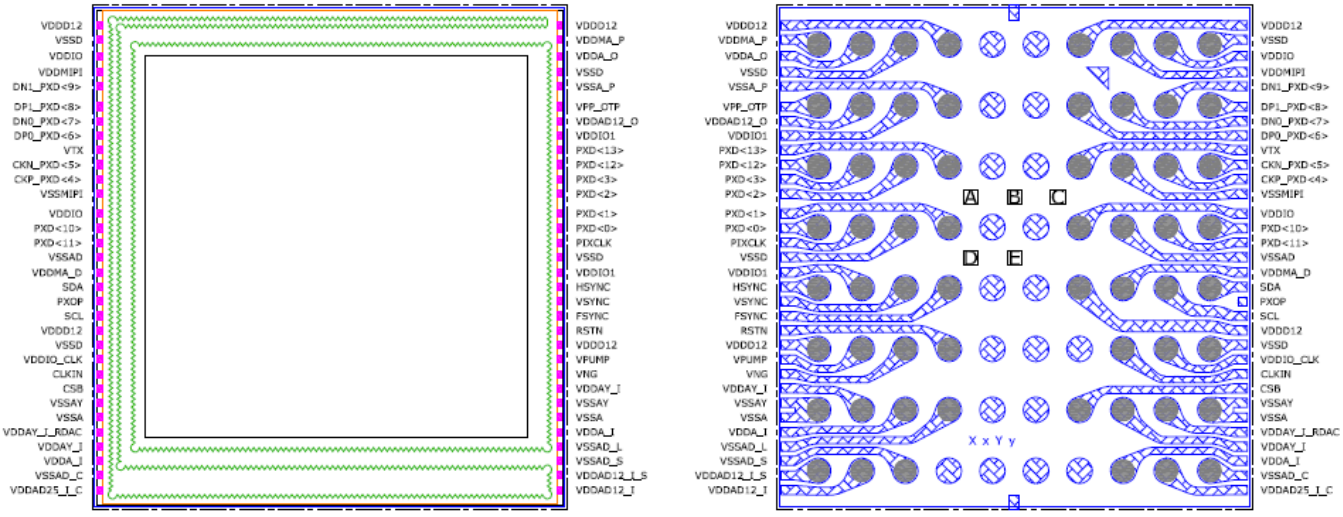
(See Fig. 1 Top view)

	1	2	3	4	5	6	7	8
A	VSSD	VDDIO	VDDMIPI	VDDD12	VDDD12	VSSD	VDDA_O	VDDMA_P
B	DP1_PXD<8>	DN1_PXD<9>	DN0_PXD<7>	DP0_PXD<6>	VSSA_P	VDDIO1	VDDAF12_O	VPP_OTP
C	CKN_PXD<5>	CKP_PXD<4>	VSSMIPI	VTX	PXD<13>	PXD<2>	PXD<3>	PXD<12>
D	PXD<10>	PXD<11>	VSSAD	VDDIO	PXD<1>	VSSD	PIXCLK	PXD<0>
E	SDA	SCL	VDDMA_D	VDDD12	FSYNC	VSYNC	VDDIO1	HSYNC
F	VSSD	VDDIO_CLK	CLKIN		RSTN	VNG	VPUMP	VDDD12
G	VSSAY/VSSA	VDDAY_I_RDAC	VDDAY_I	CSB	VSSAD_L	VDDA_I	VDDAY_I	VSSAY/VSSA
H	VSSAD_C	VDDAD25_I_C	VDDA_I			VSSAD_S	VDDAD12_I	VDDAD12_I_S

Pad Extension Formation

Lead & BGA Formation

Notch



Top View (Bumps Down)

Bottom View (Bumps Up)

Package Size : 6477 × 6886 um
Mark code : (Dimension : 200x200um)
ABCD - Date code
E - Wafer ID

Fig. 1 BGA Ball Matrix

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Pin No.	Name	Type	Description
A1	**VSSD**	GND	Digital ground
A2	**VDDIO**	Power	I/O power : 1.8V ~ 3.3V
A3	**VDDMIPI**	Power	Input 1.2V MIPI power
A4	**VDDD12**	Power	1.2V Core power
A5	**VDDD12**	Power	1.2V Core power
A6	**VSSD**	GND	Digital ground
A7	**VDDA_O**	Power	VDDA LDO output voltage(2.7-3.0V)
A8	**VDDMA_P**	Power	Input 3.3V Main Power
B1	**DP1 PXD<8>**	Output	Pixel data output ; MIPI digital data output_1 positive terminal
B2	**DN1 PXD<9>**	Output	Pixel data output ; MIPI digital data output_1 negative terminal
B3	**DN0 PXD<7>**	Output	Pixel data output ; MIPI digital data output_0 negative terminal
B4	**DP0 PXD<6>**	Output	Pixel data output ; MIPI digital data output_0 positive terminal
B5	**VSSA_P**	GND	Analog Ground
B6	**VDDIO**	Power	I/O power : 1.8V ~ 3.3V
B7	**VDDAD12_O**	Power	Internal 1.2V LDO output voltage
B8	**VPP_OTP**	Power	External voltage for OTP device
C1	**CKN PXD<5>**	Output	Pixel data output ; MIPI output clock negative terminal
C2	**CKP PXD<4>**	Output	Pixel data output ; MIPI output clock positive terminal
C3	**VSSMIPI**	GND	MIPI ground
C4	**VTX**	Power	MIPI internal TX power (0.4 V)
C5	**PXD<13>**	Output	Pixel data output
C6	**PXD<2>**	Output	Pixel data output
C7	**PXD<3>**	Output	Pixel data output
C8	**PXD<12>**	Output	Pixel data output
D1	**PXD<10>**	Output	Pixel data output
D2	**PXD<11>**	Output	Pixel data output
D3	**VSSAD**	GND	Analog Ground
D4	**VDDIO**	Power	I/O power : 1.8V ~ 3.3V
D5	**PXD<1>**	Output	Pixel data output
D6	**VSSD**	GND	Digital ground
D7	**PIXCLK**	Output	Pixel clock output
D8	**PXD<0>**	Output	Pixel data output
E1	**SDA**	I/O	I2C data, open drain type
E2	**SCL**	I/O	I2C clock, open drain type
E3	**VDDMA_D**	Power	Analog power : 3.3V
E4	**VDDD12**	Power	Digital power : 1.2V
E5	**FSYNC**	Output	Frame sync signal
E6	**VSYNC**	Output	Asserted when DOUT frame data is valid

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E7	**VDDIO**	Power	I/O power : 1.8V ~ 3.3V
E8	**HSYNC**	Output	Asserted when DOUT line data is valid
F1	**VSSD**	GND	Digital ground
F2	**VDDIO_CLK**	Power	I/O power : 1.8V ~ 3.3V
F3	**CLKIN**	Input	Master clock input
F5	**RSTN**	Input	Reset signal, active low, internal pull high
F6	**VNG**	Ref.	Reference voltage
F7	**VPUMP**	Power	Positive pump output voltage
F8	**VDDD12**	Power	Digital power : 1.2V
G1	**VSSA**	GND	Analog ground
G2	**VDDAY_I_ RDAC**	Power	Sensor power input
G3	**VDDAY_I**	Power	Sensor power input
G4	**CSB**	Input	Suspend control, "1" : suspend, "0" : normal function
G5	**VSSAD**	GND	Analog Ground
G6	**VDDA_I**	Power	Analog power input voltage (2.7V ~ 3V)
G7	**VDDAY_I**	Power	Sensor power input
G8	**VSSA**	GND	Analog ground
H1	**VSSAD**	GND	Analog Ground
H2	**VDDAD25_I**	Power	Analog power input voltage (1.2V ~ 3V)
H3	**VDDA_I**	Power	Analog power input voltage (2.7V ~ 3V)
H6	**VSSAD**	GND	Analog ground
H7	**VDDAD12_I**	Power	Analog power input voltage(1.2V)
H8	**VDDAD12_I_S**	Power	1.2V Core power

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2. Specification

Absolute Maximum Ratings		
Operating Temperature		-30ºC ~ 85ºC
Ambient Storage Temperature		-40ºC ~ 125ºC
Supply Voltage (with respect to ground)	V_{DDA}	4.5V
	V_{DDD}	3.0V
	V_{DDIO}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to V_{DDIO} + 0.5V
Lead-free temperature, Surface-mount process		245ºC
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)					
Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDA}	DC supply voltage – Analog	3.14	3.3	3.46	V
V_{DDD}	DC supply voltage – Digital core	1.1	1.2	1.3	V
V_{DDIO}	DC supply voltage – I/O	1.7	1.8	3.3	V
I_{DDA}	Operating Current – Analog (DVP) (Gain=4X)		19.74		mA
	Operating Current – Analog (MIPI) (Gain=4X)		20.16		mA
I_{DDD}	Operating Current – Digital (DVP) (Gain=4X)		47.61		mA
	Operating Current – Digital (MIPI) (Gain=4X)		58.76		mA
I_{DDIO}	Operating Current –IO 1.8V (DVP)		9.09		mA
Type : IN & I/O					
V_{IH}	Input Voltage HIGH	V_{DDIO} * 0.7			V
V_{IL}	Input Voltage LOW			V_{DDIO} * 0.3	V
Type : OUT & I/O					
V_{OH}	Output Voltage HIGH	V_{DDIO} * 0.9			V
V_{OL}	Output Voltage LOW			V_{DDIO} * 0.1	V

AC Operating Condition					
Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency			64	MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%

Sensor Characteristics		
Parameter	Typ.	Unit
Sensitivity	6500	mV/Lux-Sec
Signal to Noise Ratio MAX	42.5	dB
Dynamic Range	81	dB

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3. I²C™ Bus

PS5270 supports I²C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1001000" and supports receiving / transmitting speed as maximum 400 kHz.

I²C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 3.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 3.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

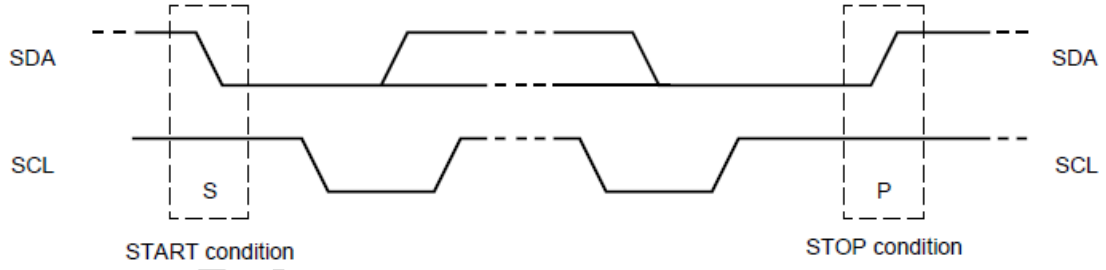

Fig.3.1 Start and Stop Condition

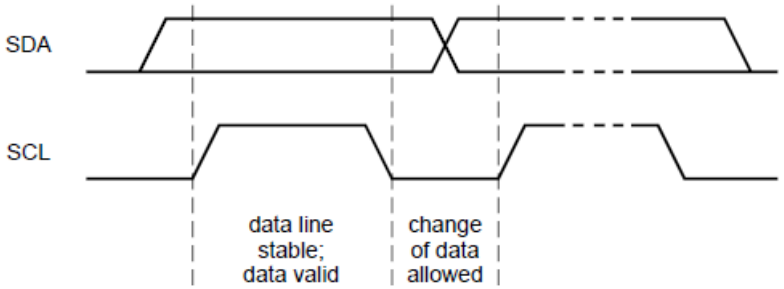

Fig.3.2 Valid Data

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Data Transfer Format

Master transmits data to salve (write cycle)

- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of **PS5270** internal control registers. (Please refer to **PS5270** register description)

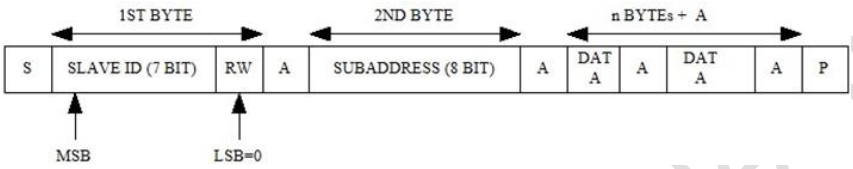

Fig.3.3 Master-transmitter transmits to slave-receiver

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (**PS5270**) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the **PS5270** acknowledgment, the master places the 8 bits data on SDA line and transmit to **PS5270** control register (address was assigned by 2nd byte). After **PS5270** issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the **PS5270** sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside **PS5270** can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.

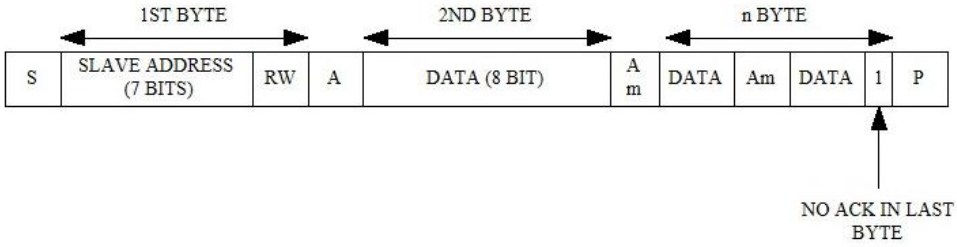

Fig.3.4 Slave-transmitter transmits to master-receiver

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by **PS5270**. The 8 bits data was read from **PS5270** internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the **PS5270** place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (**PS5270**) must releases SDA line to master to generate STOP condition.

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I²C™ Bus Timing

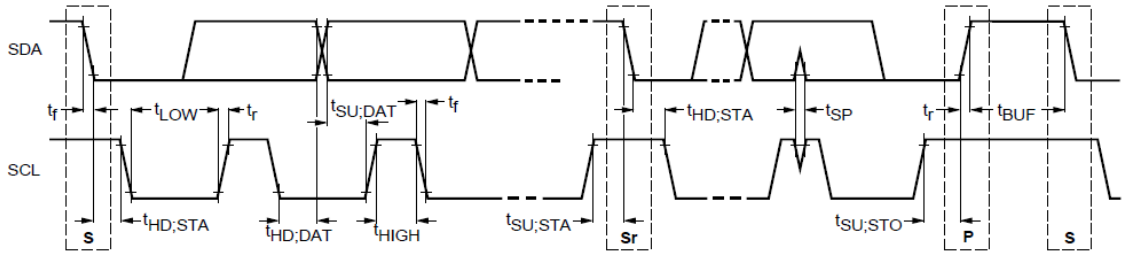

Fig.3.5 Definition of timing for F/S mode devices on the I2C-bus

I²C™ Bus Timing Specification						
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency.	f_{scl}	10	100		400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-			µs
Low period of the SCL clock.	t_{LOW}	4.7	-			µs
High period of the SCL clock.	t_{HIGH}	0.75	-			µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-			µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45			µs
Data set-up time.	$t_{SU;DAT}$	250	-			ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.			ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.			ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-			µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-			µs
Capacitive load for each bus line.	C_b	1	15			pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-			V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-			V

Note: It depends on the “high” period time of SCL.

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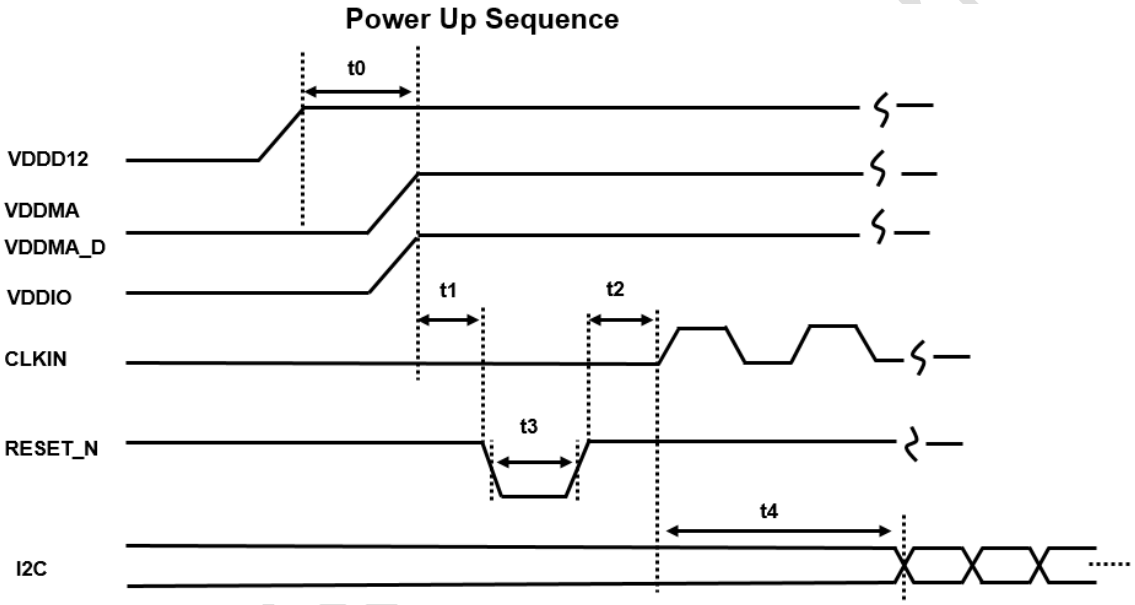
4. Power Sequence

Power-Up Sequence

The recommended power-up sequence for the PS5270 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn on VDDD12 power supply.
2. After 100µs (t0), VDDMA, VDDMA_D and VDDIO power supply simultaneously.
3. After 100µs (t1), RESET_N must go low.
4. RESET_N active low for at least 1ms (t3).
5. After 100µs (t2), enable CLKIN.
6. Wait at least 1ms (t4), I2C starts to write commands.



Power-Down Sequence

The recommended power-down sequence for the PS5270 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn off VDDD12 power supply.
2. After 100µs (t0), turn off VDDMA, VDDMA_D and VDDIO power supply simultaneously.

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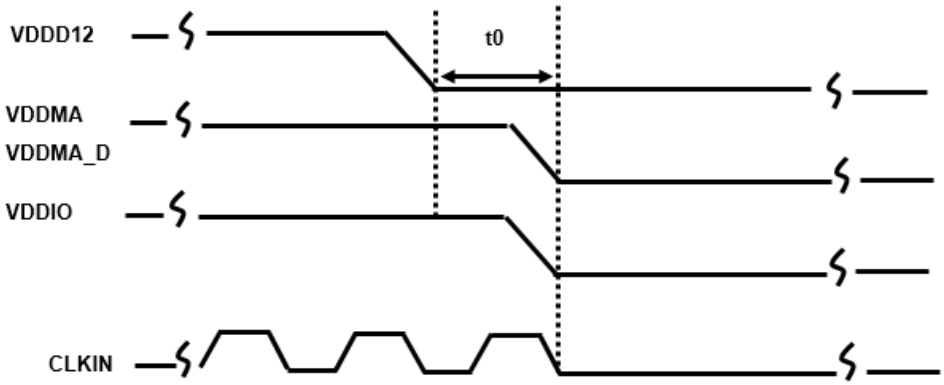
Power Down Sequence



CSB Suspend Sequence

The recommended CSB Suspend sequence for the PS5270 is shown as the following figure. The available power supplies must have the separation specified below.

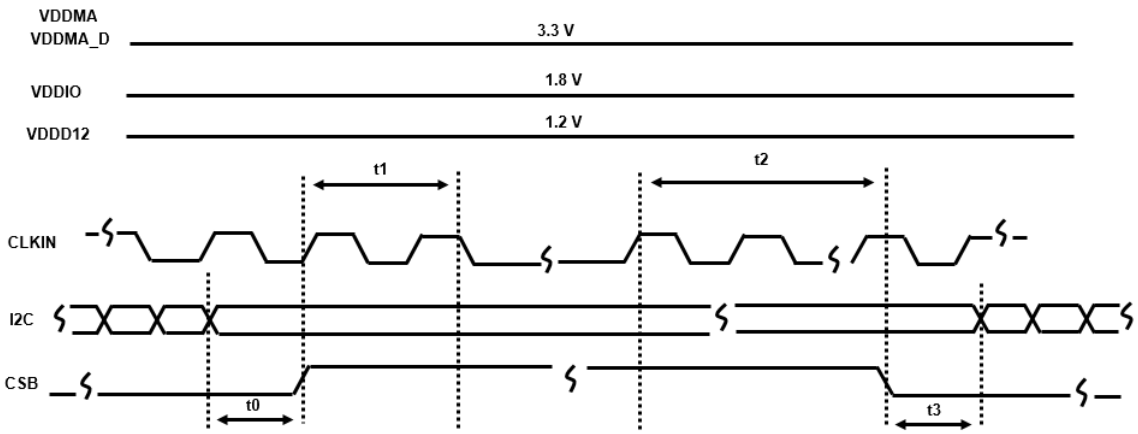
ON → OFF :

1. I2C must write commands to turn off internal clock for PS5270 .
2. After 100μs (t0), CSB must go high
3. After 100μs (t1), turn off CLKIN.

OFF → ON :

1. Turn on CLKIN.
2. After 100μs (t2), CSB must go low.
3. Wait at least 1ms (t3) for internal clock stable.
4. I2C starts to write commands.

CSB Suspend Sequence



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5. Register Table

Bank	Address		Bit	Name	R/W	Description
	Hex	Dec				
0	00	00	[7:0]	PartID[15:8]	R	Sensor ID
0	01	01	[7:0]	PartID[7:0]	R	Sensor ID
0	02	02	[3:0]	VersionID[3:0]	R	Sensor ID
0	03	03	[3:0]	SubID[3:0]	R	Sensor ID
0	11	17	[7]	Cmd_GatedAllClk	R/W	Clock Gated Control (1: Gate Clock)
0	BE	190	[6]	Cmd_Pxclk_Inv	R/W	Invert Pxclk Out
			[5]	Cmd_Vsync_Inv	R/W	Invert Vsync Out
			[4]	Cmd_Hsync_Inv	R/W	Invert Hsync Out
1	04	04	[6:4]	R_PxclkO_dly[2:0]	R/W	Timing Delay for Pxclk
			[2:0]	R_HsyncO_dly[2:0]	R/W	Timing Delay for Hsync
1	05	05	[6:4]	R_VsyncO_dly[2:0]	R/W	Timing Delay for Vsync
			[3]	Cmd_8_TriState	R/W	TriState IO of PxData[1:0]
			[2]	Cmd_Sw_PwrDn	R/W	Power-Down Control
			[1]	Cmd_Sw_TriState	R/W	TriState IO of PxData, Hsync, Vsync, and Pxclk
1	09	09	[0]	UpdateFlag	R/W	Exposure & Gain Update Control (Write 0x01)
1	0A	10	[7:0]	Cmd_Lpf[15:8]	R/W	Line per frame = Cmd_Lpf + 1
1	0B	11	[7:0]	Cmd_Lpf[7:0]	R/W	Line per frame = Cmd_Lpf + 1
1	0C	12	[7:0]	Cmd_OffNy1[15:8]	R/W	Exposure Control
1	0D	13	[7:0]	Cmd_OffNy1[7:0]	R/W	Exposure Control
1	0E	14	[3:0]	Cmd_OffNe1[11:8]	R/W	Exposure Control
1	0F	15	[7:0]	Cmd_OffNe1[7:0]	R/W	Exposure Control
1	1B	27	[7]	Cmd_Hflip	R/W	Horizontal Flip
			[6:5]	Cmd_Askip_H[1:0]	R/W	Horizontal Skip
			[2:0]	Cmd_Hsize_e1[10:8]	R/W	Raw Image Horizontal Size
1	1C	28	[7:0]	Cmd_Hsize_e1[7:0]	R/W	Raw Image Horizontal Size
1	1D	29	[7]	Cmd_Vflip	R/W	Vertical Flip
			[6:5]	Cmd_Askip_V[1:0]	R/W	Vertical Skip
			[2:0]	Cmd_Vsize[10:8]	R/W	Raw Image Vertical Size
1	1E	30	[7:0]	Cmd_Vsize[7:0]	R/W	Raw Image Vertical Size
1	1F	31	[2:0]	Cmd_Vstart[10:8]	R/W	Raw Image Vertical Offset

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1	20	32	[7:0]	Cmd_VStart[7:0]	R/W	Raw Image Vertical Offset
1	27	39	[4:0]	Cmd_LineTime[12:8]	R/W	Line Time = Cmd_LineTime clock cycles
1	28	40	[7:0]	Cmd_LineTime[7:0]	R/W	Line Time = Cmd_LineTime clock cycles
1	83	131	[7:0]	Cmd_gain_idx[7:0]	R/W	Gain index
1	90	144	[1]	Cmd_ADC_Sample_Rotate	R/W	ADC sample order control
			[0]	Cmd_Adc_sample_posedge	R/W	ADC sample timing control
1	92	146	[4:0]	R_ISP_TestMode[4:0]	R/W	Test Image Control
1	93	147	[7:0]	R_ISP_TestValueLo[7:0]	R/W	Test Image Control
1	94	148	[7:0]	R_ISP_TestValueHi[7:0]	R/W	Test Image Control
1	91	151	[0]	Cmd_Pga_D1frm	R/W	Pga Gain auto-delay one frame
1	A3	163	[4]	Cmd_WOI_VOffset_sign	R/W	Vertical offset of output image
			[2:0]	Cmd_WOI_VOffset[10:8]	R/W	Vertical offset of output image
1	A4	164	[7:0]	Cmd_WOI_VOffset[7:0]	R/W	Vertical offset of output image
1	A5	165	[2:0]	Cmd_WOI_VSize[10:8]	R/W	Vertical size of output image
1	A6	166	[7:0]	Cmd_WOI_VSize[7:0]	R/W	Vertical size of output image
1	A7	167	[4]	Cmd_WOI_HOffset_sign	R/W	Horizontal offset of output image
			[2:0]	Cmd_WOI_HOffset[10:8]	R/W	Horizontal offset of output image
1	A8	168	[7:0]	Cmd_WOI_HOffset[7:0]	R/W	Horizontal offset of output image
1	A9	169	[2:0]	Cmd_WOI_HSize[10:8]	R/W	Horizontal size of output image
1	AA	170	[7:0]	Cmd_WOI_HSize[7:0]	R/W	Horizontal size of output image
1	AB	171	[5:0]	Cmd_Np[5:0]	R/W	TG Frequency control
1	E3	227	[5]	T_SR_GPIO	R/W	IO slew control
			[1:0]	T_OPDRV_GPIO[1:0]	R/W	IO driving Strength
1	F1	241	[5:0]	T_spll_predivider[5:0]	R/W	PLL Control
1	F2	242	[5:0]	T_spll_postdivider [5:0]	R/W	PLL Control
1	F5	245	[1:0]	T_spll_modedivider [1:0]	R/W	PLL Control
2	46	70	[7]	Cmd_DigDac_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	47	71	[7:0]	Cmd_DigDac_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	48	72	[7]	Cmd_DigDac_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[2:0]	Cmd_DigDac_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel
2	49	73	[7:0]	Cmd_DigDac_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	4A	74	[7]	Cmd_DigDac_Gr_Sign	R/W	Black Level Offset for Gr Channel

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			[2:0]	Cmd_DigDac_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	4B	75	[7:0]	Cmd_DigDac_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	4C	76	[7]	Cmd_DigDac_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	4D	77	[7:0]	Cmd_DigDac_R_Offset[7:0]	R/W	Black Level Offset for R Channel

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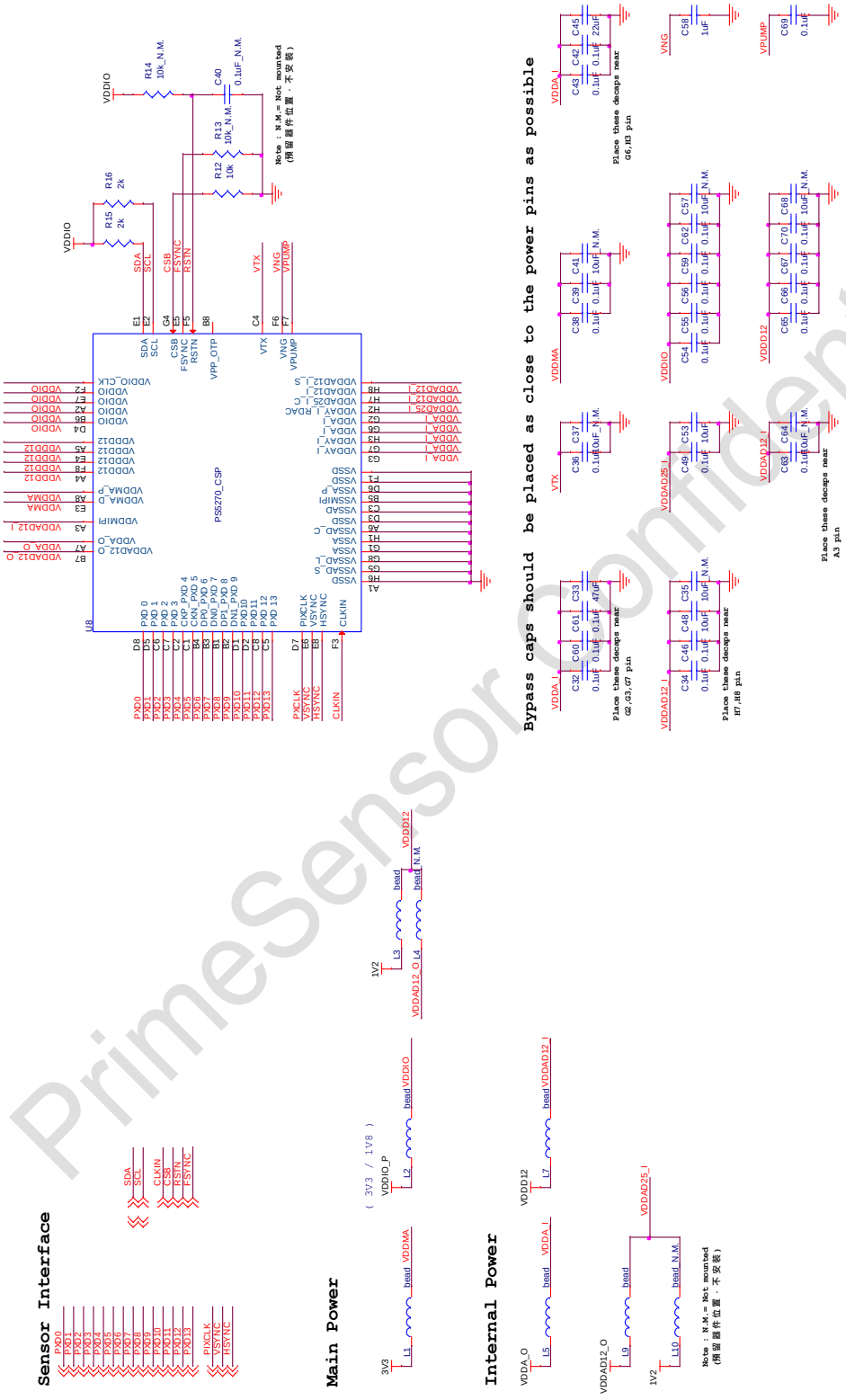
6. Reference Circuit Schematic

➢ Parallel Interface



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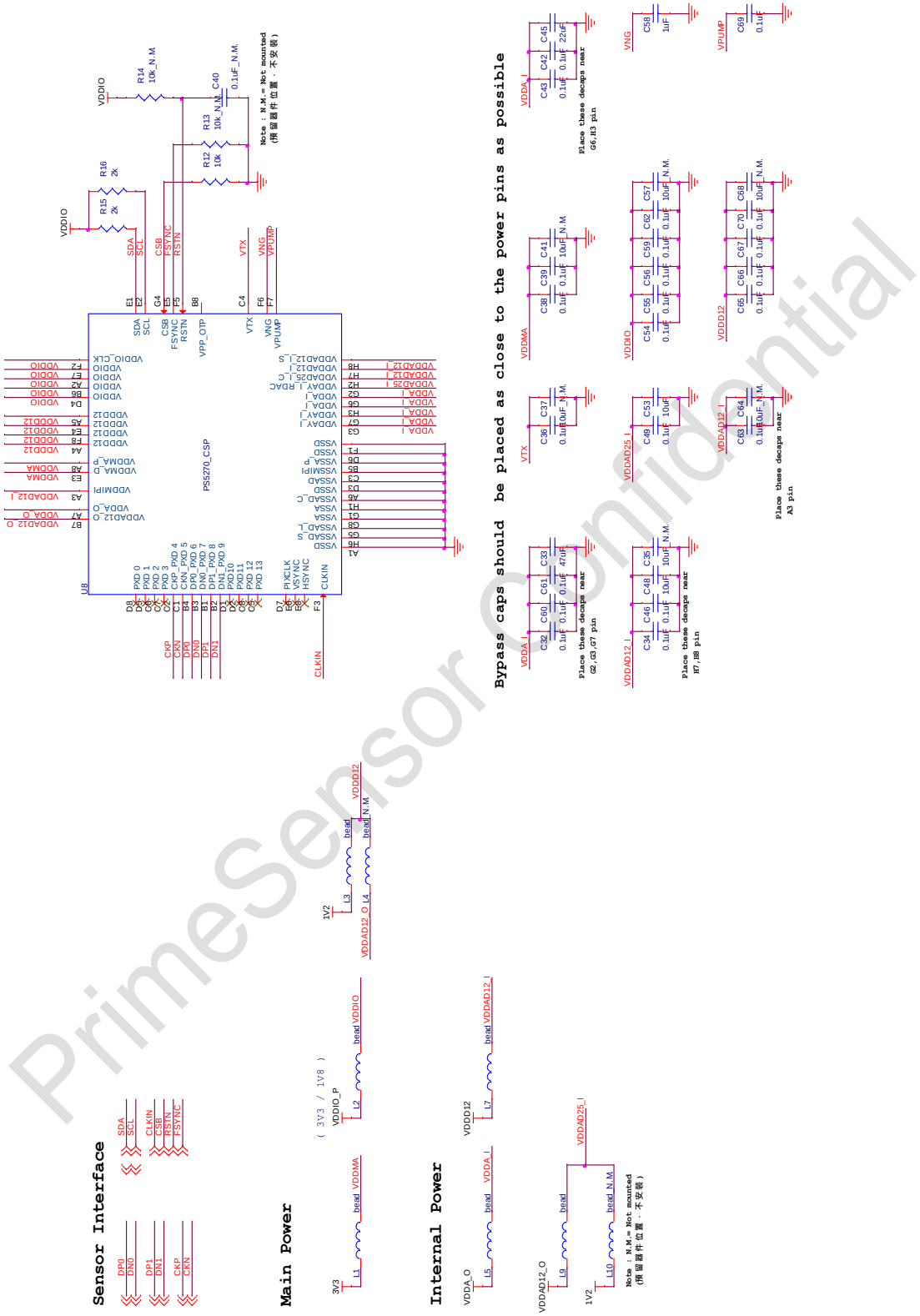
➢ MIPI Interface



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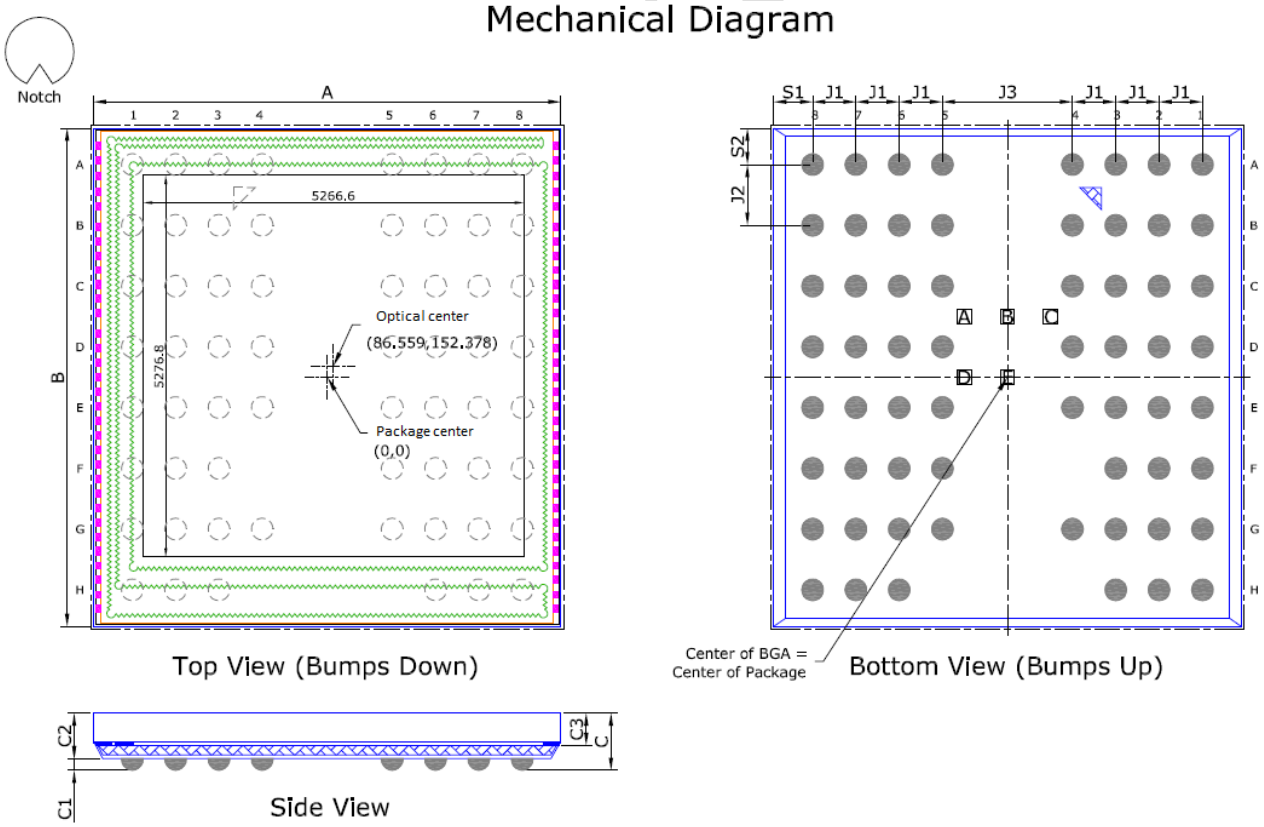
7. Package Information

- **Package Outline Dimension**

	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	**A**	6447	6422	6472
Package Body Dimension Y	**B**	6886	6861	6911
Package Height	**C**	790	730	850
Ball Height	**C1**	160	130	190
Package Body Thickness	**C2**	630	585	675
Thickness of Glass surface to wafer	**C3**	445	425	465
Ball Diameter	**D**	300	270	330
Total Pin Count	**N**	61		
Pin Count X axis	**N1**	8		
Pin Count Y axis	**N2**	8		
Pins Pitch X axis	**J1**	600		
	J3	1800		
Pins Pitch Y axis	**J2**	840		
Edge to Pin Center Distance along X	**S1**	538.5	508.5	568.5
Edge to Pin Center Distance along Y	**S2**	503	473	533

Mechanical Diagram



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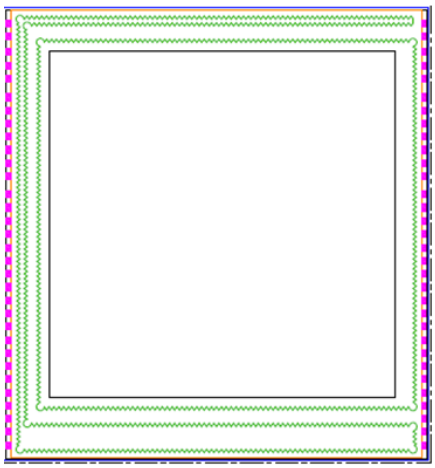
- **Recommended PCB Layout**

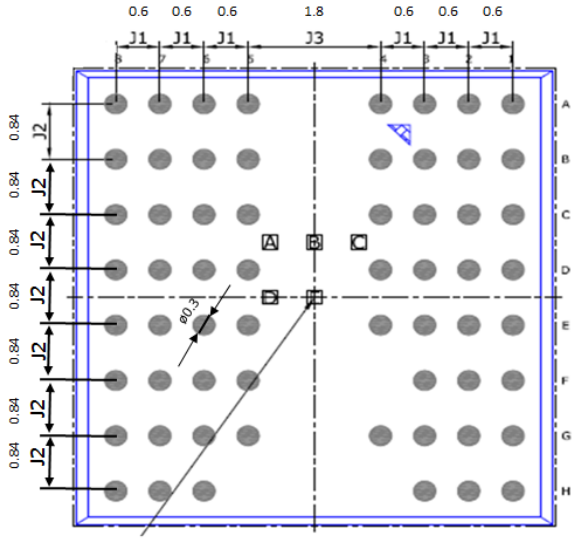
Recommended Stiffener type for FPC(Flex) back-site (at Sensor package area)

If use FPC (Flex) board, need add stiffener onto the back-side to enhance the Flex strength.

Recommended Stiffener type: FR4 or stainless steel or equivalent material

.





Note:
1. All diemension is millimeter
2. Top View

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Title	PS5270LT PCB Layout
Part Number	PS5270LT
Package Type	CSP 61B
P number	N/A
Drawn	Masa Chang
Check	
Approve	
Scale	
Chip Size	N/A
Rev.	A

Rev.	Description	Date
A	New Issue	7/17/17

- **Recommended Guideline for PCB Assembly**

I. Recommended vender and type for Pb-free solder paste
   1 Almit LFM-48W TM-HP
   2 Senju M705-GRN360-K

II. IR Reflow Soldering Profile:

Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.

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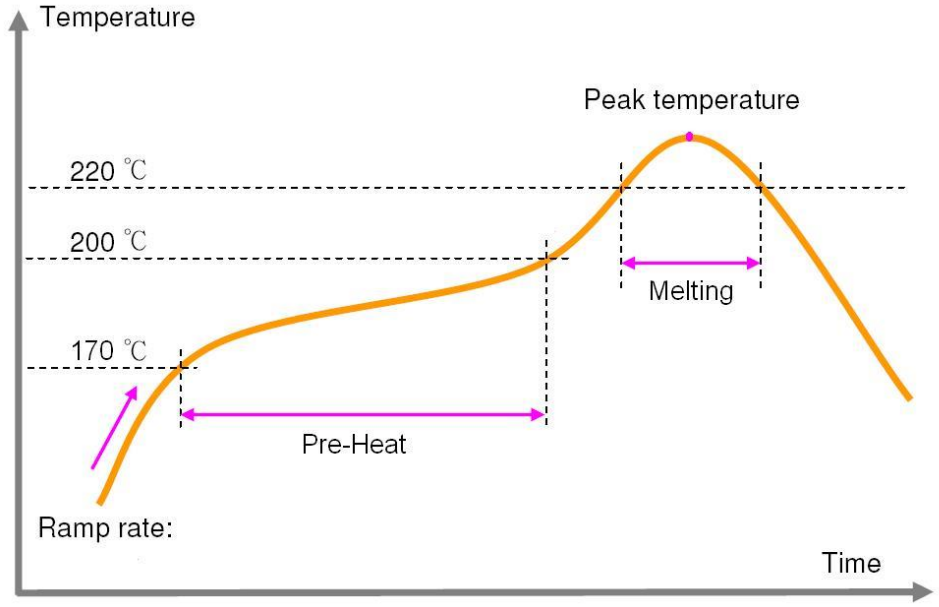
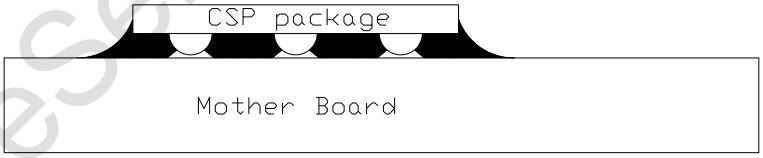


- **Reflow Profile**
  1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
  2. Preheat zone:
     - 2.1 Temp ramp from 170~ 200 degree C
     - 2.2 Exposure time: 90 +/- 30 sec
  3. Melting zone:
     - 3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
     - 3.2 Peak temperature: 245 degree C.

III. Others

- **Epoxy under-filled process is required post IC mounting process.**



- **Peek tweezers or plastic tweezers is required post IC manual handling for pick and place.**

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8. Revision History

Revision	Description	Date
V0.1	Preliminary data sheet release	Jul. 20, 2017
V0.2	Sensitivity update	Aug.18, 2017
V0.3	Add specification and power consumption	Aug.28, 2017

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E-mail: fae.service@primesensor.com.tw