4Gb M-die NAND Flash

Single-Level-Cell (1bit/Cell)

datasheet

Revision History

Revision No.	History	Draft Date	Remark
1.0	Final version release	Feb. 2019	Final

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1.0 INTRODUCTION

1.1 General Description

S8F4G08UAM is a 4G-bit NAND Flash Memory with spare 256M-bit. The device is offered in 3.3V V_{CC}. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 350μs per one page and an erase operation can be performed in typical 4ms per one block. Data in the data register can be read out at 20ns cycle time per Byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The write operations can be locked using $\overline{WP}$ input pin.
This device supports ONFI 1.0 specification.
The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.
The devices is available to support below three security features:

- OTP (one time programmable) area which is a restricted access area where sensitive data/code can be store permanently.
- Serial number(unique identifier) which allows the devices to be uniquely identified.
- Non-volatile protection to lock sensible data permanently.

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, not described in the datasheet.

1.2 Features

- Voltage Supply
  - V_{CC} : 3.3V (2.7V ~ 3.6V)

- NAND Interface
  - Command/Address/Data Multiplexed I/O Port
  - X8 I/O Bus
  - ONFI 1.0 Command Set

- Organization
  - Memory Cell Array : (512M + 32M)Byte x 8bit
  - Block Size : (256K + 16K)Bytes
  - Page Size : (4K + 256)Byte
  - Data Register : (4K + 256)Byte

- Automatic Program and Erase
  - Page Program : (4K + 256)Byte
  - Block Erase : (256K + 16K)Byte

- Page Read Operation
  - Single Plane Read : 55μs(Typ.) 350μs(Max.)
  - Serial Access 3.3V : 20ns(Min.)

- Fast Write Cycle Time
  - Page Program time : 350μs(Typ.)
  - Block Erase Time : 4ms(Typ.)

- Copy Back Program
  - Fast data copy without external buffering

- Security
  - OTP area
  - Serial number (unique ID)
  - Non-volatile protection

- Electronic Signature
  - 1st cycle: Manufacturer Code
  - 2nd cycle: Device Code
  - 3rd cycle: Internal chip number, Cell Type
  - 4th cycle: Page size, Block size, Organization, Spare size
  - 5th cycle : Multi-plane information

- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions

- Data Retention
  - 60K Program / Erase Cycles with internal ECC on

- Chip Enable don't care option
  - Simple interface with microcontrollers Data Retention

- Package :
  - 48 pin TSOP (12 x 20mm)
  - 48 Ball FBGA (6.5 x 8.0mm)
  - 63 Ball FBGA (9.0 x 11.0mm)
  - Lead and Halogen Free

1.3 Product List

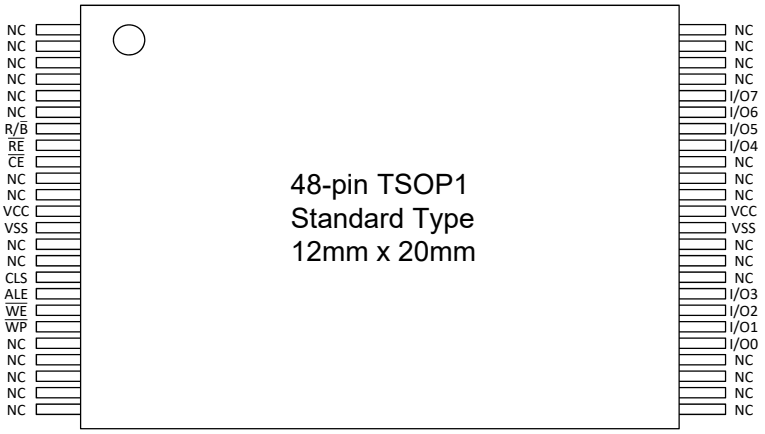
Part Number	Density	Organization	V_{CC} Range	PKG Type
S8F4G08UAM-Yx[1)]B0	4Gb	x8	2.7V ~ 3.6V	48 TSOP1
S8F4G08UAM-Xx[1)]B0	4Gb	x8	2.7V ~ 3.6V	48 FBGA
S8F4G08UAM-Bx[1)]B0	4Gb	x8	2.7V ~ 3.6V	63 FBGA

1) NOTE :
C : Commercial
I : Industrial

1.4 Package

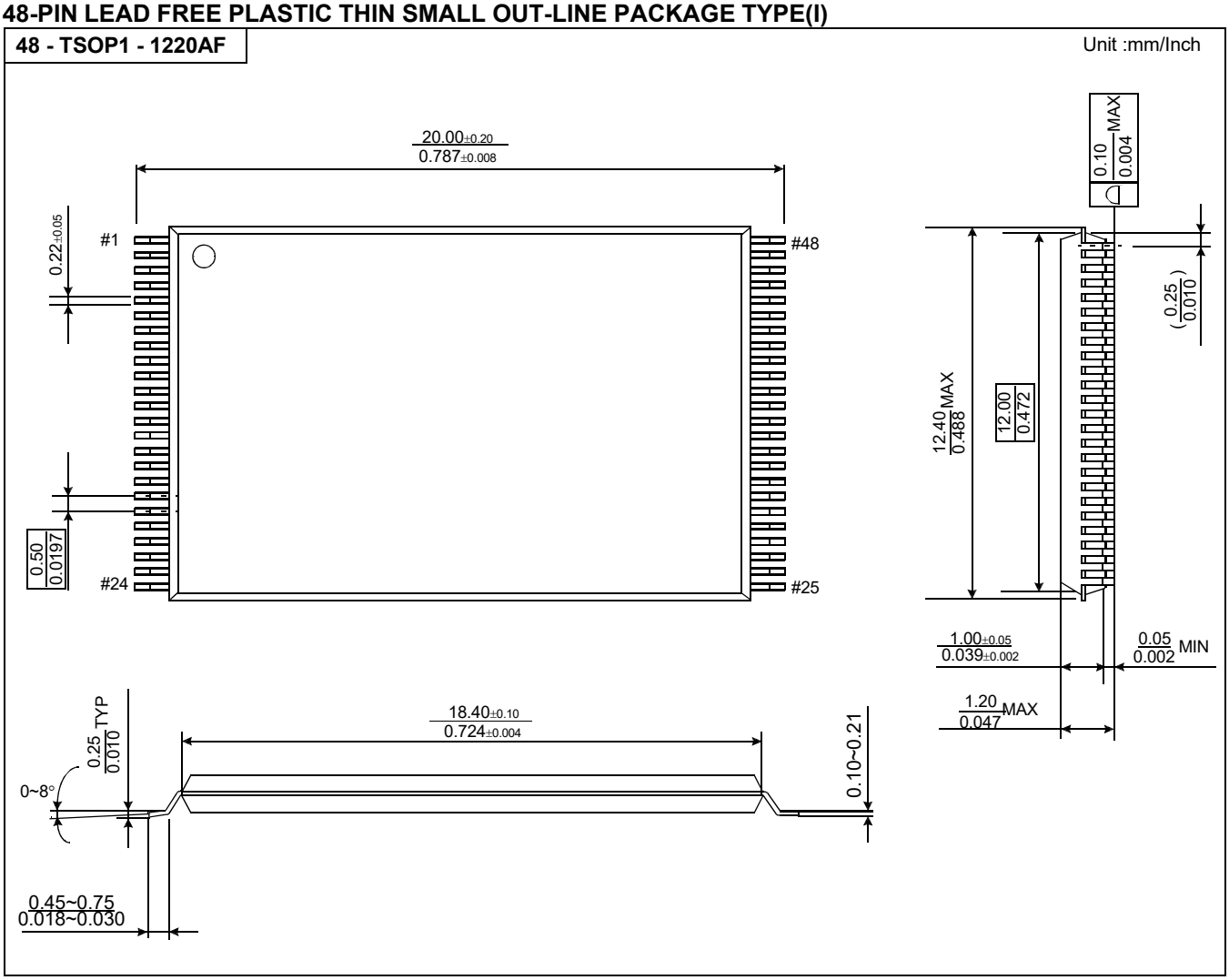
1.4.1 Pin Configuration (48 TSOP1)

S8F4G08UAM-YxB0



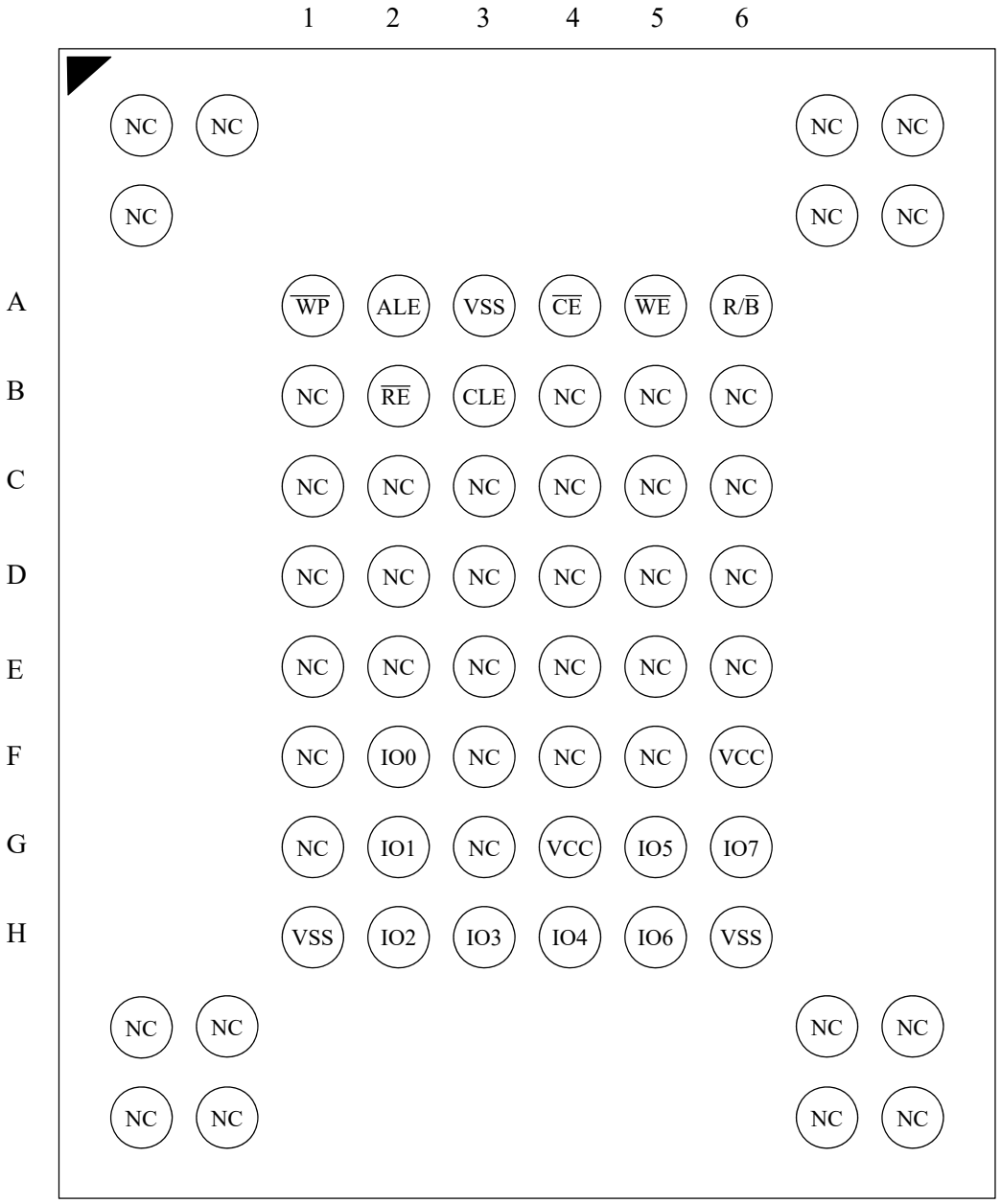
1.4.2 Package Dimensions (48 TSOP1)

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



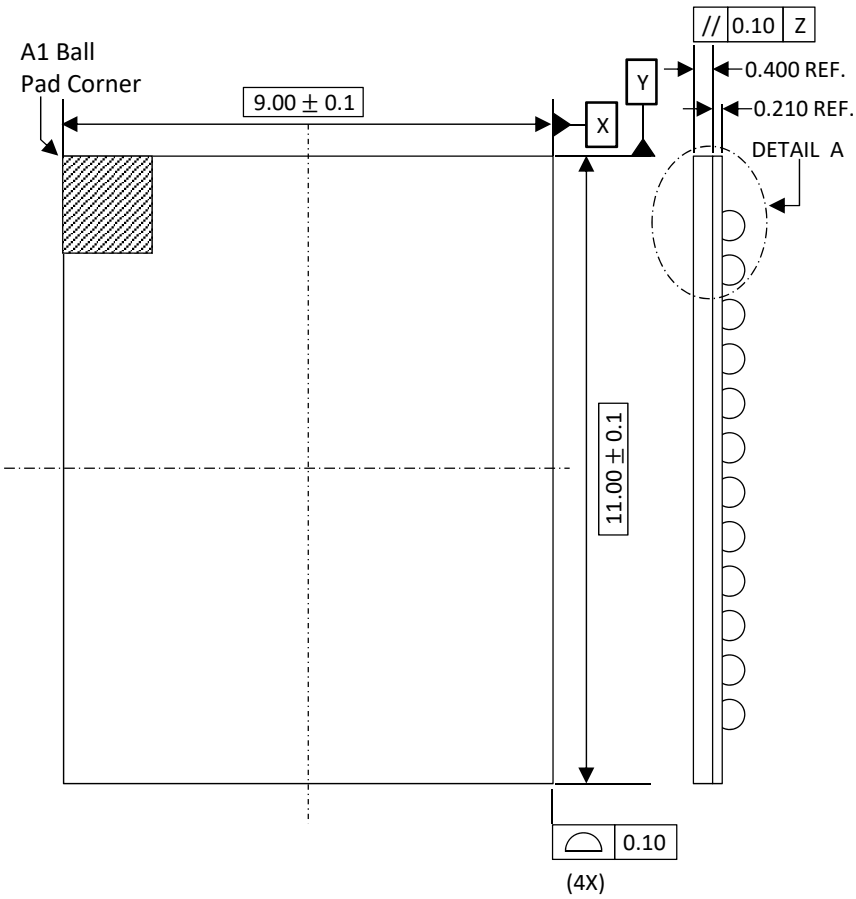
1.4.3 Pin Configuration (63 FBGA 9x11mm)

S8F4G08UAM-BxB0

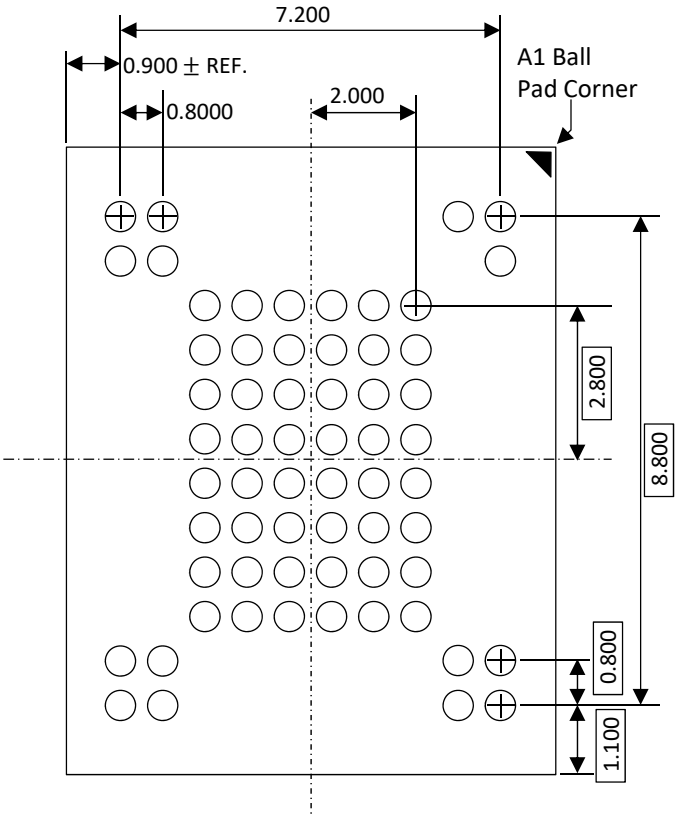


Top View

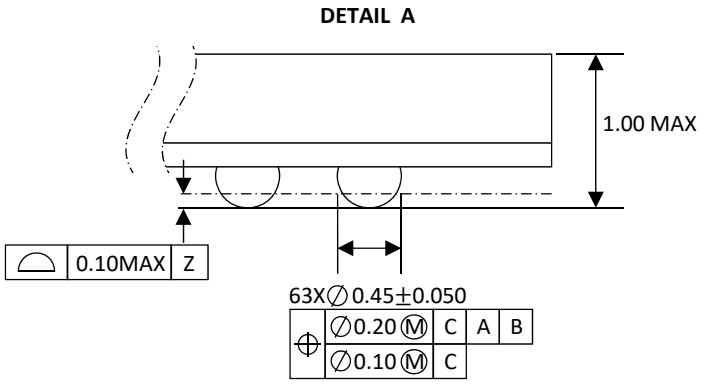
1.4.4 Package Dimensions (63 FBGA 9x11mm)



Top View



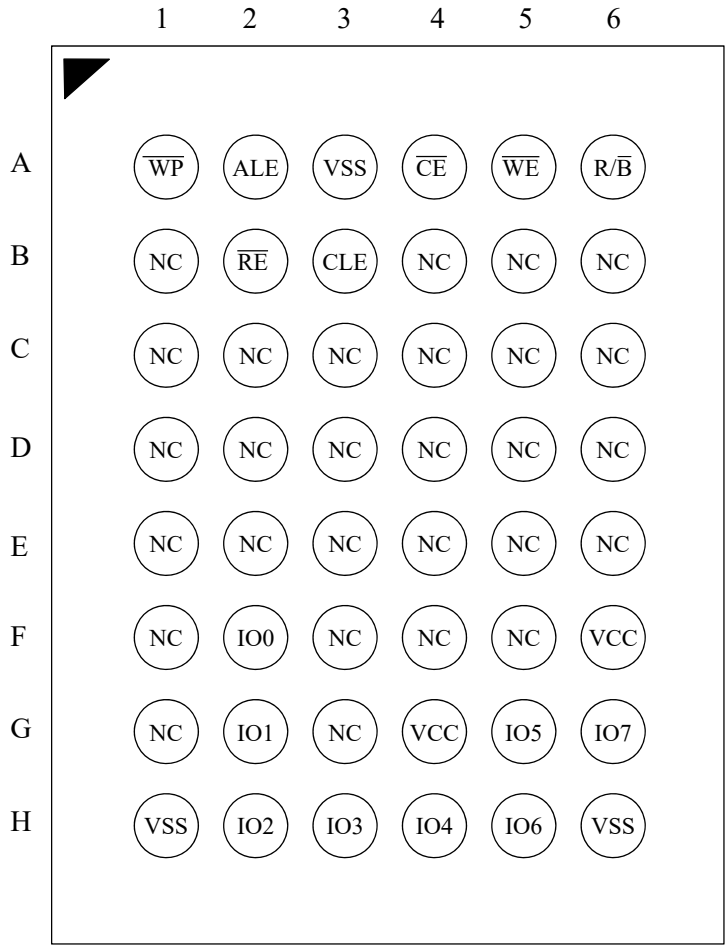
Bottom View



1. All Dimensions are in millimeters.
2. Post Reflow Solder Ball Diameter.
(Pre Reflow Diameter :∅0.40±0.02)

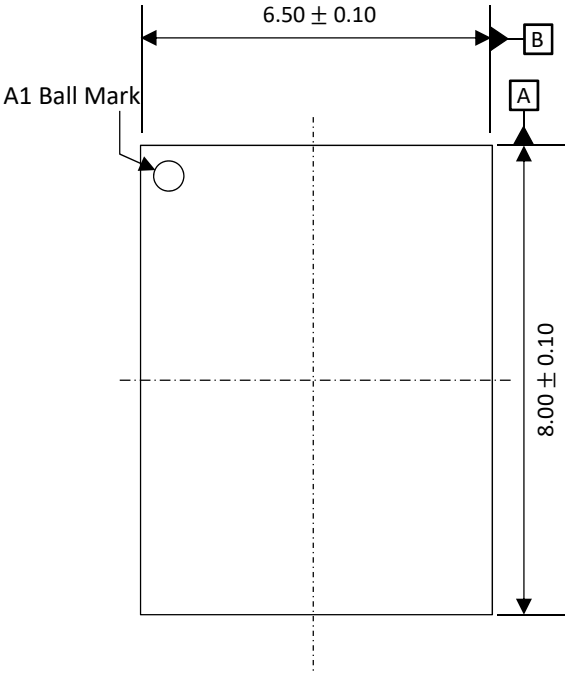
1.4.5 Pin Configuration (48 FBGA 6.5x8mm)

S8F4G08UAM-XxB0

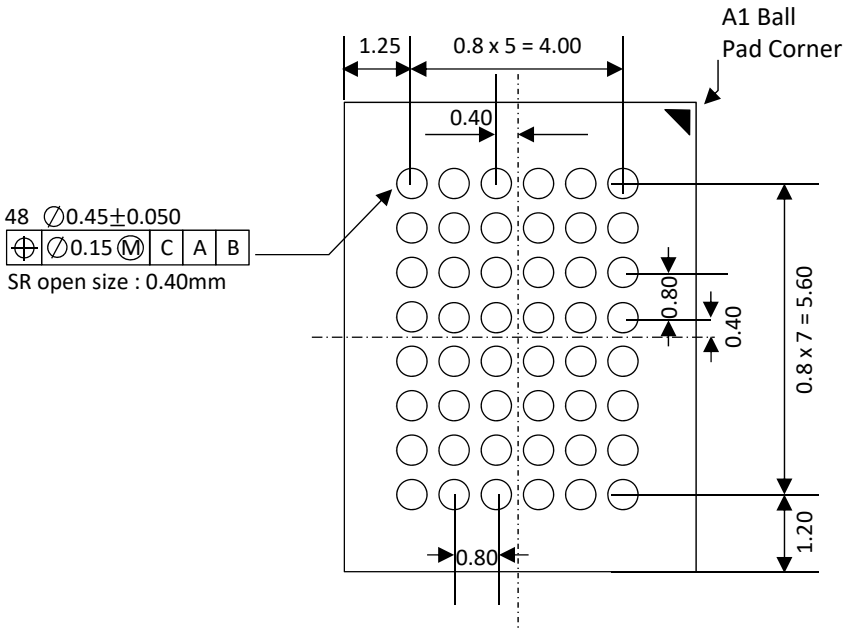


Top View

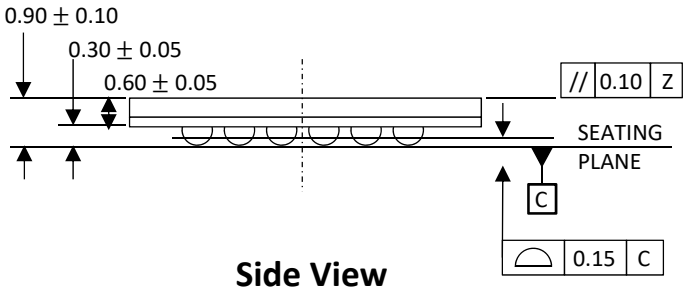
1.4.6 Package Dimensions (48 FBGA 6.5x8mm)



Top View



Bottom View



Side View

1. All Dimensions are in millimeters.
2. Post Reflow Solder Ball Diameter.
(Pre Reflow Diameter :∅0.40±0.02)

1.5 Pin Descriptions

[Table 1] Pin Descriptions

Pin Name	Pin Function
I/O0 ~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the DQ inputs inside the command register on the rising edge of $\overline{WE}$.
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the DQ inputs inside the internal address register on the rising edge of $\overline{WE}$.
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, $\overline{CE}$ high does not deselect the memory. The device goes into Stand-by mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state, and will not enter Standby mode even if the $\overline{CE}$ goes high.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of $\overline{WE}$.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations. Hardware Write Protection is activated when the $\overline{WP}$ pin is low. In this condition modify operation do not start and the content of the memory is not altered. $\overline{WP}$ pin is not latched by Write Enable to ensure the protection even during the power up phases.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output is an Open Drain pin that signals the state of the memory
VCC	**POWER** The V_{CC} supplies the power for all the operations. (Read, Write, and Erase).
VSS	**GROUND**
N/C	**NO CONNECTION / DON'T USE**

NOTE :
A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.6 Block Diagram

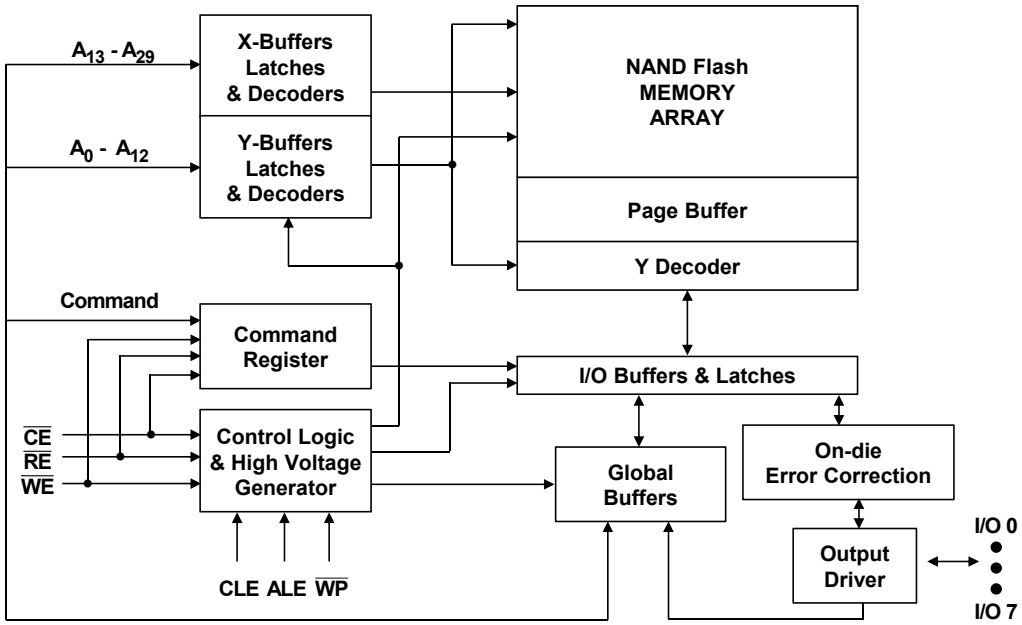


Figure 1. S8F4G08UAM Functional Block Diagram

1.7 Memory Array Organization

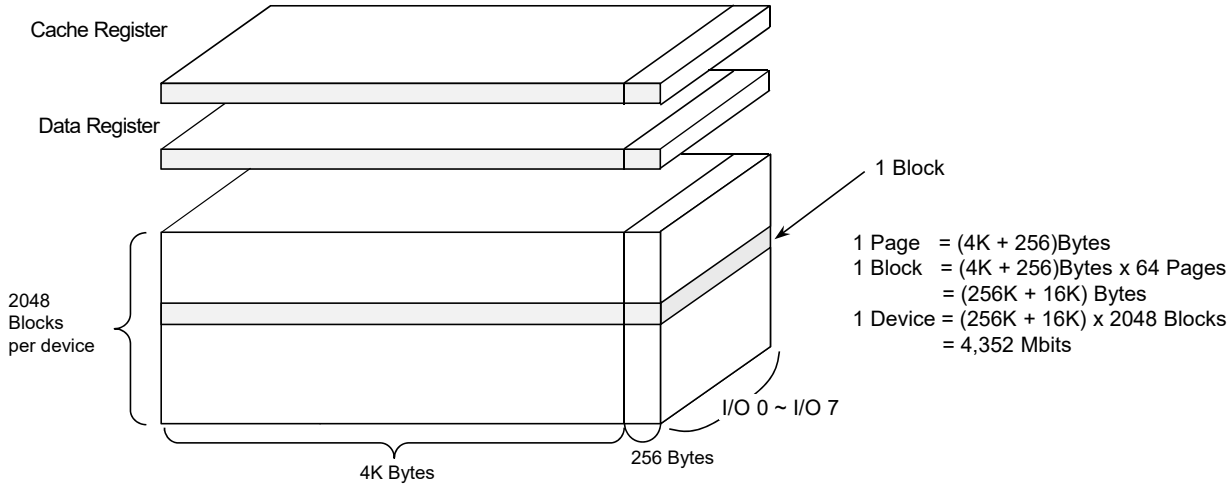


Figure 2. S8F4G08UAM Array Organization

[Table 2] Address Cycle Map

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	A12	*L	*L	*L	
3rd Cycle	A13	A14	A15	A16	A17	A18	A19	A20	Row Address
4th Cycle	A21	A22	A23	A24	A25	A26	A27	A28	
5th Cycle	A29	*L	*L	*L	*L	*L	*L	*L	

NOTE :

1. *L must be set to "Low"
2. A0 – A12 : Column Address in the page
3. A13 – A18 : Page Address in the block
   A19 – A29 : Block Address
4. The device ignores any additional address input cycle than required.

1.8 Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The row address is used to address pages, blocks, and LUNs. When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued. For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero. The row address structure is shown in Figure 3 “Row Address Layout ” with the least significant row address bit to the right and the most significant row address bit to the left.

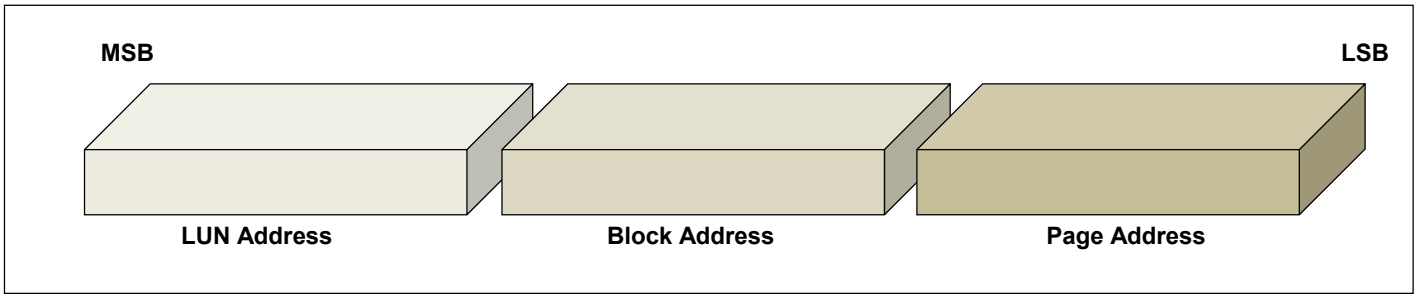


Figure 3. Row Address Layout

The page address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a page address and a LUN address. A host shall not access an address of a page or block beyond maximum Page Address or block address.

[Table 3] Block Arrangement

Row Address	Block Number	
000000h ~ 00003Fh	Block 0 (Plane 0)	Main Block (2,048 Blocks)
000040h ~ 00007Fh	Block 1 (Plane 0)	
000080h ~ 0000BFh	Block 2 (Plane 0)	
0000C0h ~ 0000FFh	Block 3 (Plane 0)	
000100h ~ 00013Fh	Block 4 (Plane 0)	
000140h ~ 00017Fh	Block 5 (Plane 0)	
•••••	•••••	
01FF00h ~ 01FF3Fh	Block 2044 (Plane 0)	
01FF40h ~ 01FF7Fh	Block 2045 (Plane 0)	
01FF80h ~ 01FFBFh	Block 2046 (Plane 0)	
01FFC0h ~ 01FFFFh	Block 2047 (Plane 0)	

2.0 PRODUCT INTRODUCTION

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$ .Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc. require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register.

[Table 4] Command Sets

Function	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable while accessed LUN is busy	Acceptable while other LUNs are busy
RESET	FFh	-	-	-	O	O
READ UNIQUE ID	EDh	-	-	-	-	-
READ PARAMETER PAGE	ECh	-	-	-	-	-
READ ONFI SIGNATURE	90h	20h	-	-	-	-
GET FEATURE	EEh	-	-	-	-	-
SET FEATURE	EFh	-	-	-	-	-
READ STATUS	70h	-	-	-	O	O
READ STATUS ENHANCED	78h	-	-	-	O	O
RANDOM DATA INPUT	85h	-	-	-	-	O
RANDOM DATA OUTPUT	05h	E0h	-	-	-	O
PAGE READ	00h	30h	-	-	-	O
PAGE PROGRAM	80h	10h	-	-	-	O
PAGE RE-PROGRAM	8Bh	10h	-	-	-	O
BLOCK ERASE	60h	D0h	-	-	-	O
READ FOR COPY-BACK	00h	35h	-	-	-	O
COPY-BACK PROGRAM	85h	10h	-	-	-	O
VOLATILE LOCK ALL	2Ah	-	-	-	-	O
BLOCK UNLOCK LOWER	23h	-	-	-	-	O
BLOCK UNLOCK UPPER	24h	-	-	-	-	O
LOCK DOWN	2Ch	-	-	-	-	O
BLOCK PROTECTION STATUS	7Ah	-	-	-	-	O
ONE TIME PROGRAMMABLE (OTP) AREA ENTRY(1)	29h-17h-04h-19h	-	-	-	-	-
OTP PROTECTION SET UP(1)	4Ch-03h-1Dh-41h-80h	10h	-	-	-	-
PROGRAM PBP SETTINGS(1)			-	-	-	-
PROGRAM PBP LOCK DOWN(1)			-	-	-	-
Firmware SLC Mode	DAh	-	-	-	-	O

Note :

1. Once, One Time Programmable (OTP) Area entry command issued, PBP Setting command is not valid.
   Vice versa, PBP settings command is only accepted if OTP Area entry has not been issued.

2.1 Valid Block

[Table 5] The Number of Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	2,008	-	2,048	Blocks

NOTE :
1) The 1st block is guaranteed to be a valid block at the time of shipment.
2) Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment.

2.2 Absolute Maximum DC Ratings

[Table 6] Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C
Voltage on any pin relative to V_{SS}		V_{CC}	-0.6 to + 4.6	V
		$V_{I/O}$	-0.6 to + 4.6	
Temperature Under Bias		T_{BIAS}	-50 to +125	°C
Storage Temperature		T_{STG}	-65 to +150	°C

NOTE :
1) Please contact to Netsol and confirm the availability of the product.
2) Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions
3) Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2.3 Recommended Operating Conditions

[Table 7] Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Ground Supply Voltage	V_{SS}	0	0	0	V

NOTE :
Voltage reference to GND.

2.4 DC Operating Characteristics

[Table 8] DC & Operating Characteristics

Parameter		Symbol	Test Conditions	Vcc = 2.7V~3.6V			Unit
				Min	Typ	Max	
Operation Current	Read	I_{CC1}	tRC=tRC(min), $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	25	35	mA
	Program	I_{CC2}	Normal		25	35	
	Erase	I_{CC3}	-		15	30	
Stand-by Current (CMOS)		I_{SB}	$\overline{CE}$=V_{CC}-0.2,$\overline{WP}$=0V/V_{CC}	-	-	100	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC}(max)	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC}(max)	-	-	±10	
Input High Voltage		V_{IH}1)	-	0.8xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}1)	-	-0.3	-	0.2xV_{CC}	
Output High Voltage Level		V_{OH}	I_{OH}= - 400µA, ($V_{CC.typ}$=3.3V)	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}= 2.1mA, ($V_{CC.typ}$=3.3V)	-	-	0.4	
Output Low Current (R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}= 0.4V, ($V_{CC.typ}$=3.3V)	8	10	-	mA

2.5 Input / Output Capacitance (T_A=25°C, f=1.0Mhz)

[Table 9] Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE :
Capacitance is sampled and not 100% tested.

2.6 AC Test Condition

[Table 10] AC Test Condition

Parameter	Value
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC}/2
Output Load	1 TTL GATE and C_L=50pF

NOTE :
1) These parameters are verified device characterization and are not 100% tested.

2.7 Read / Program / Erase Characteristics

[Table 11] NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Single Plane Read (4KB Page)	t_R	-	55	350	us
Program Time	t_{PROG}	-	350	600	μs
Block Erase Time	t_{BERS}	-	4	10	ms
Number of Partial Program Cycles	Nop	-	-	4	cycles

NOTE :
1) Typical value is measured at V_{CC}=3.3V, T_A=25°C. Not 100% tested.
2) All functions are guaranteed on NOP4 cases while reliability and data retention specification is guaranteed on NOP1 case.

2.8 AC Timing Parameters Table

[Table 12] AC Timing Characteristics

Parameter	Symbol	Vcc,typ = 3.3V		Unit
		Min	Max	
CLE Setup Time	t_{CLS}	10	-	ns
CLE Hold Time	t_{CLH}	5	-	ns
$\overline{CE}$ Setup Time	t_{CS}	15	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	10	-	ns
ALE Setup Time	t_{ALS}	10	-	ns
ALE Hold Time	t_{ALH}	5	-	ns
Data Setup Time	t_{DS}	7	-	ns
Data Hold Time	t_{DH}	5	-	ns
Write Cycle Time	t_{WC}	20	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	7	-	ns
Address to Data Loading Time	t_{ADL}	70	-	ns
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	10	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	20	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	16	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	30	ns
$\overline{CE}$ High to ALE or CLE Don't Care	t_{CSD}	10	-	ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15	-	ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5	-	ns
$\overline{CE}$ High to Output Hold	t_{COH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	7	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low for Random Data Out	t_{WHR2}	200	-	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	t_{CR}	10	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	5/10/500[1)]	μs
Write Protection Time	t_{WW}	100	-	ns

NOTE :
1) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5μs.

3.0 NAND FLASH TECHNICAL NOTES

3.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Netsol. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

3.2 Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Netsol makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the first byte of spare area on the 1st or 2nd page. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart.

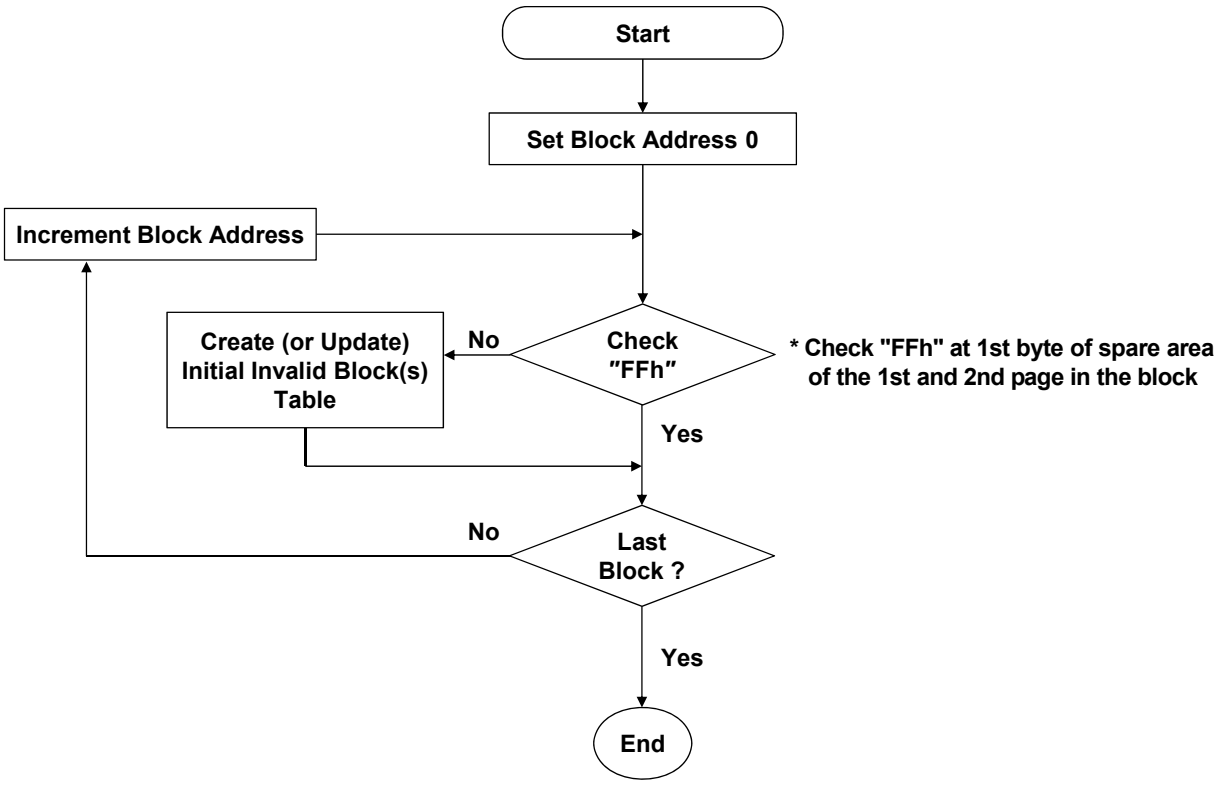


Figure 4. Flow Chart to Create Initial Invalid Block Table

NOTE :
1) Do not try to erase the detected bad blocks, because the bad bock information will be lost.
2) Do not perform program and erase operation in invalid block, it is impossible to guarantee the Input data and to ensure that the function is normal.

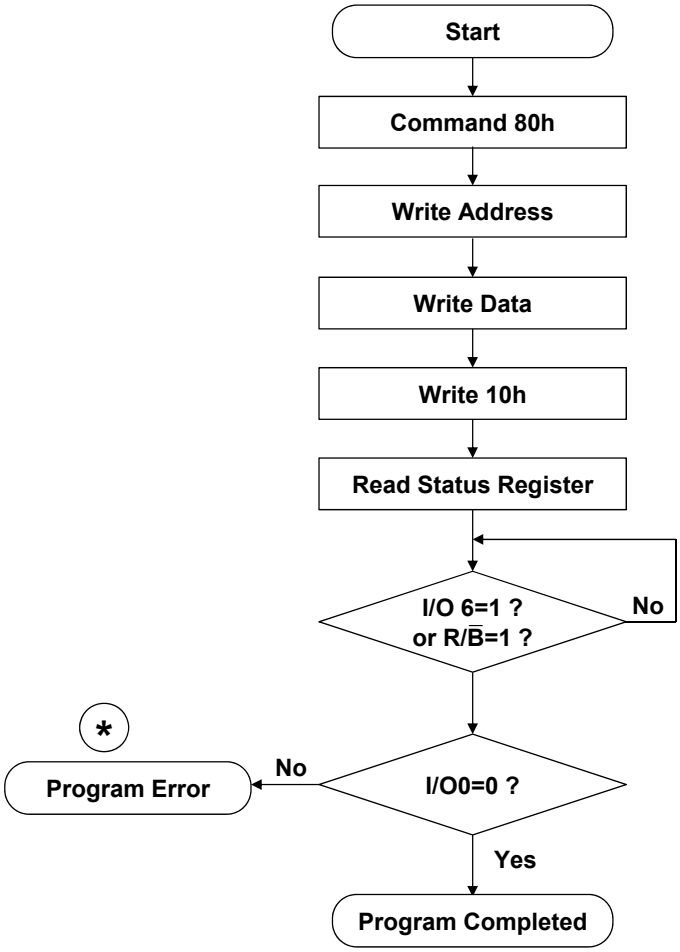
3.3 Error in Write or Read Operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.

[Table 13] Failure Cases

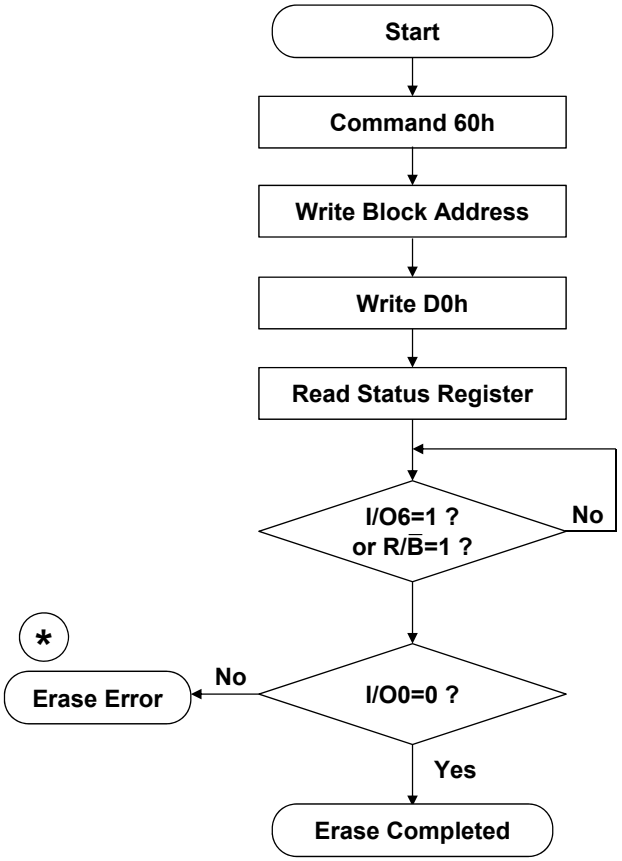
Failure Mode		Detection and Countermeasure Sequence
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

Program Flow Chart



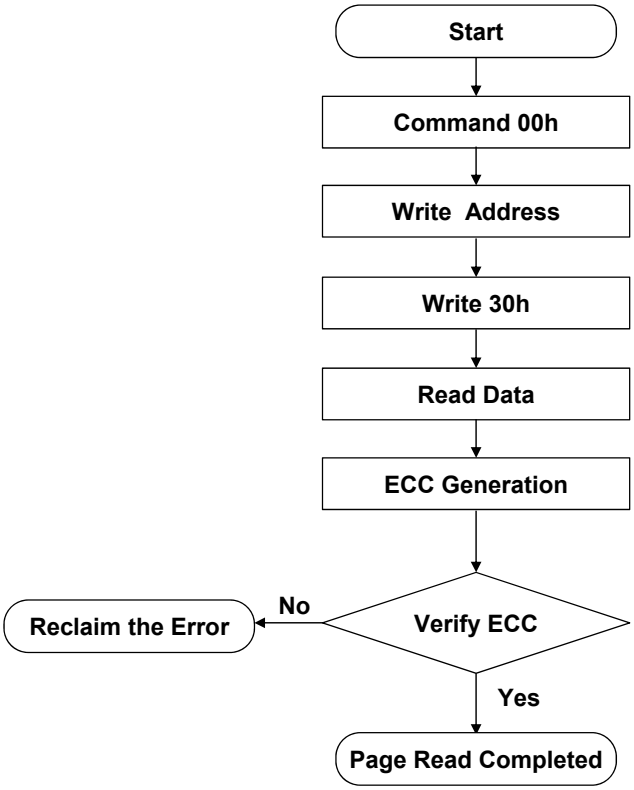
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

Erase Flow Chart

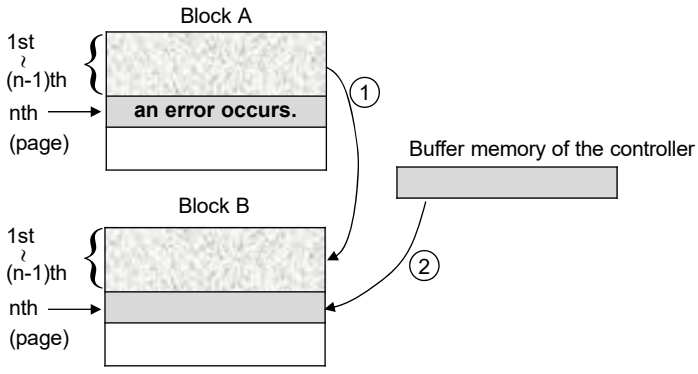


(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Read Flow Chart



Block Replacement



1. When an error happens in the nth page of the Block 'A' during erase or program operation.
2. Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
3. Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
4. Bad block table should be updated to prevent from erasing or programming Block A.

Figure 5. Flow Chart

4.0 DEVICE OPERATION

4.1 Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.8 V (3.3 V Device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power down. A recovery time of minimum 100us is required before internal circuit gets ready for any command sequences. The two-step command sequence for program/erase provides additional software protection.

Issuing of FFh command after Power Up Sequence allows Auto CAM read of the device.

The host must wait for R/$\overline{B}$ to be valid High before issuing RESET command (FFh) to initialize any targets that share same $\overline{CE}$.The R/$\overline{B}$ signal becomes valid after 100us since VCC reaches 2.7V. The RESET command (FFh) must be issued to all targets as the first command after the NAND device is powered up and R/$\overline{B}$ becomes valid. Each target will be busy for a maximum of 2ms after the RESET command (FFh) is issued. The RESET busy time can be monitored by polling R/$\overline{B}$ or issuing the READ STATUS (70h) command (if multi LUNs share same $\overline{CE}$, Read Status Enhanced command should be used instead of READ STATUS). Each NAND die (LUN) may draw less than 10mA for over 1ms prior to the execution of the first RESET command (FFh) after the device is powered up. During the power up sequence including the RESET busy time, each LUN consumes a maximum current of 50mA.

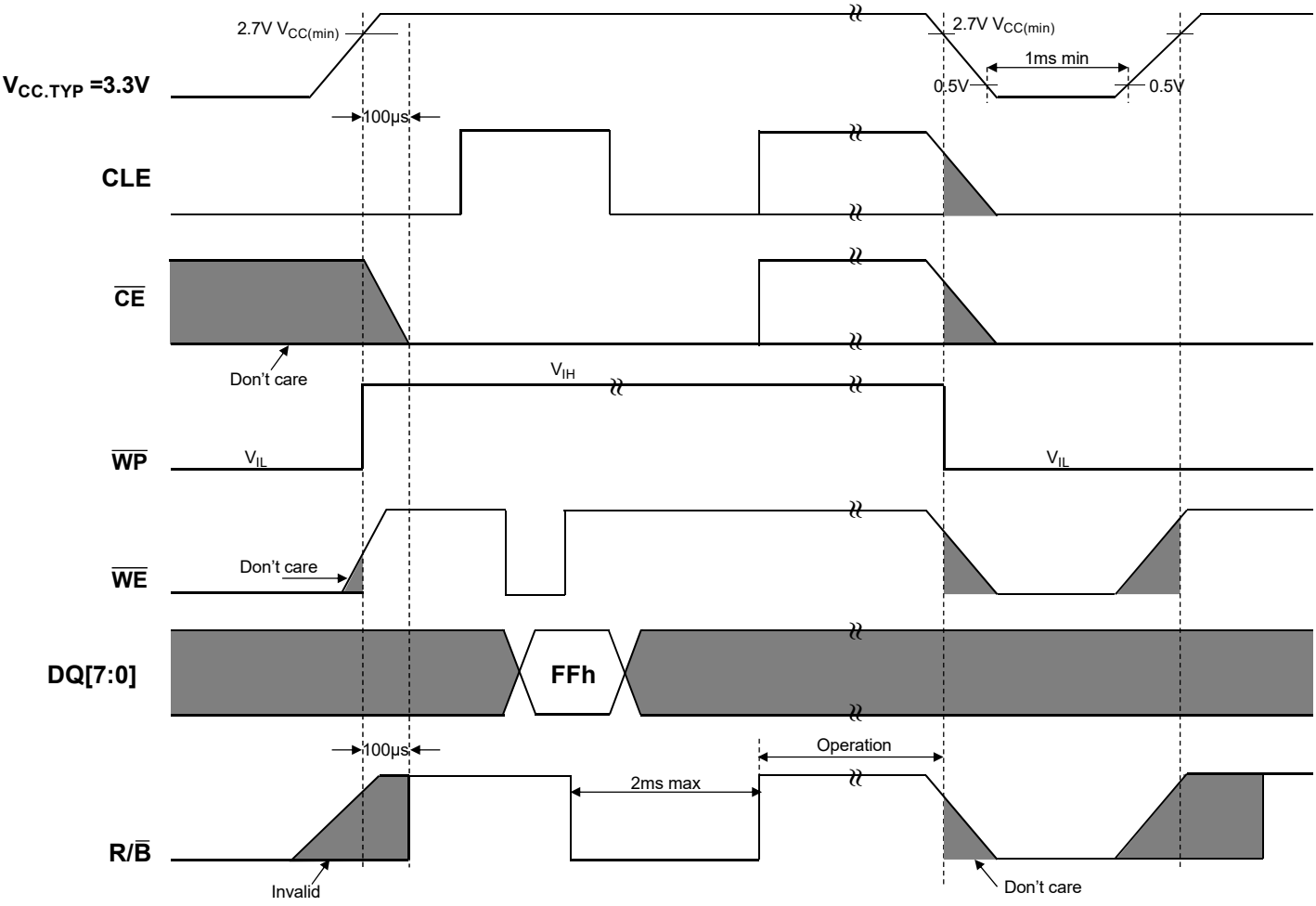


Figure 6. AC Waveforms for Power Transition

NOTE :
1) During the initialization, the device consumes a maximum current of ICC1.
2) Once Vcc drops under 2.5V, it is recommended to drive down Vcc to below 0.5V and stay low for at least 1ms before Vcc powered up. Floating Vcc during power-down is prohibited.

4.2 Mode Selection

[Table 14] Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input(5 cycles)
H	L	L		H	H	Write Mode	Command Input
L	H[1)]	L		H	H		Address Input(5 cycles)
L	L	L		H	H	Data Input	
L	L[1)]	L	H		X	Data Output (on going)	
X	X	L	H	H	X	Data Output (suspended)	
L	L	L	H[3)]	H[3)]	X	During Read(Busy)	
X	X[1)]	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}[2)]	Stand-by	

NOTE :
1) X can be V_{IL} or V_{IH}. H = Logic level HIGH. L = Logic level LOW.
2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
3) $\overline{WE}$ and $\overline{RE}$ during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out.
In this time, only Reset, Read Status, and Multiplane Read Status can be input to the device.

4.3 BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. Typically glitches less than 5ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations. .

Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high.

Address Input

Address Input bus operation allows the insertion of the memory address. 5 clock cycles are needed to input the addresses. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation(write/erase) the Write Protect pin must be high.

Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

Data output

Data Output bus operation allows to read data from the memory array and to check the status register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low.

Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

Standby

In Standby the device is deselected, outputs are disabled and Power Consumption is reduced.

4.4 Page Read Operation

Page Read Operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 4,352 (4KB Page) bytes of data within the selected page are transferred to the data registers in less than 350μs (t_R, 4KB). The system controller may detect the completion of this data transfer (t_R) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 20ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ make the device output the data starting from the selected column address up to the last column address. The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

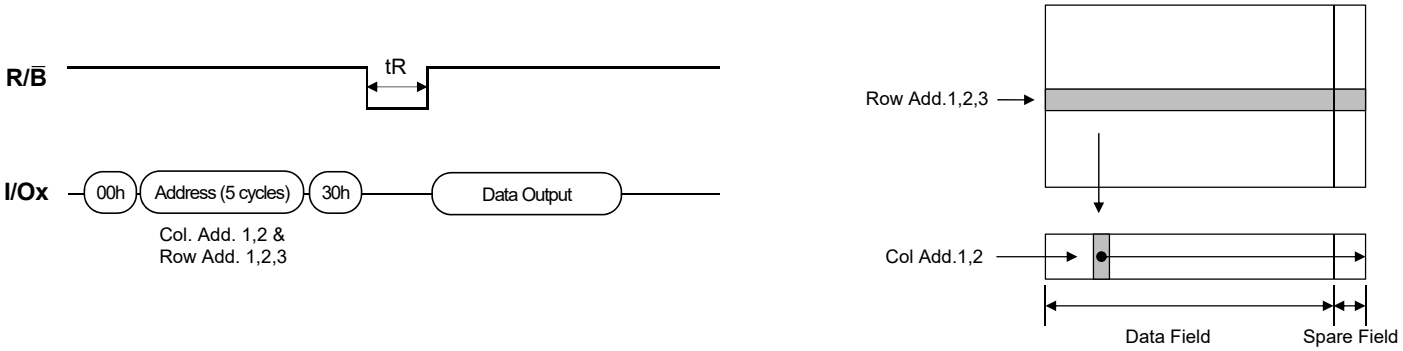


Figure 7. Page Read Sequence

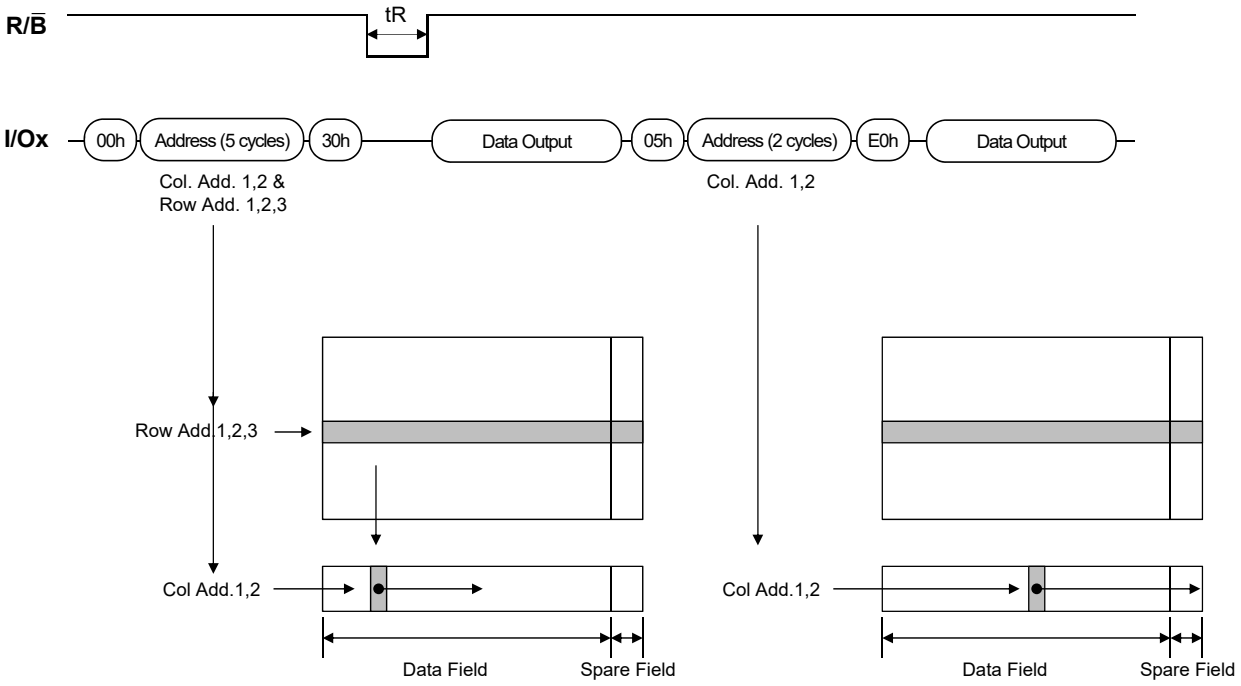


Figure 8. Page Read with Random Data Output Sequence

4.5 Page Program Operation

A page program cycle consists of a serial data loading period in which up to 4,352 bytes (4KB Page) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the R$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. The device is programmed basically by page, but it also allows multiple partial page programming of a word up to consecutive bytes up to 4,352 bytes (4KB Page) in a single page program cycle. The basic unit of Program operation is 32bytes per 1 ECC chunk and Program input shall be made if and only if 32bytes or more input data detected.

The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. For example, 2 times for main array (1time/1,024byte) and 2 times for spare array (1time/64byte). Consequent input of to be programmed main data following with ECC user spare is not allowed. Main data shall be stored in main data region, and then use Random Data Input to change column to the address of user spare for programming of corresponding user spare of input data. Both main data and user spare shall be input for NOP operation; if only user spare input without main data partially programmed (NOP) at the same time, data is no longer guaranteed.

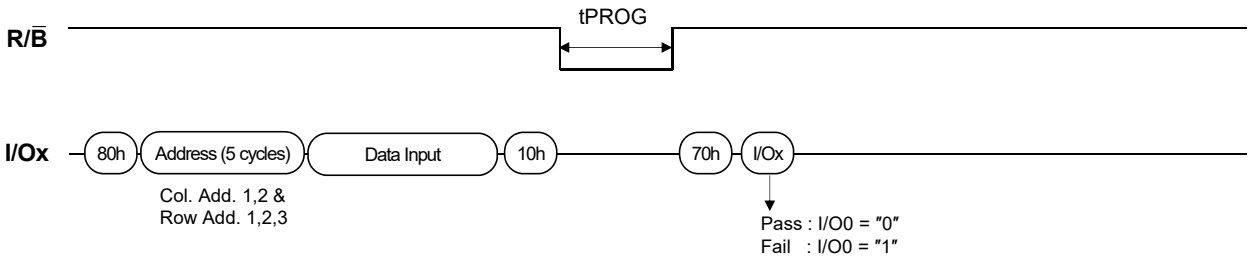


Figure 9. Page Program Sequence

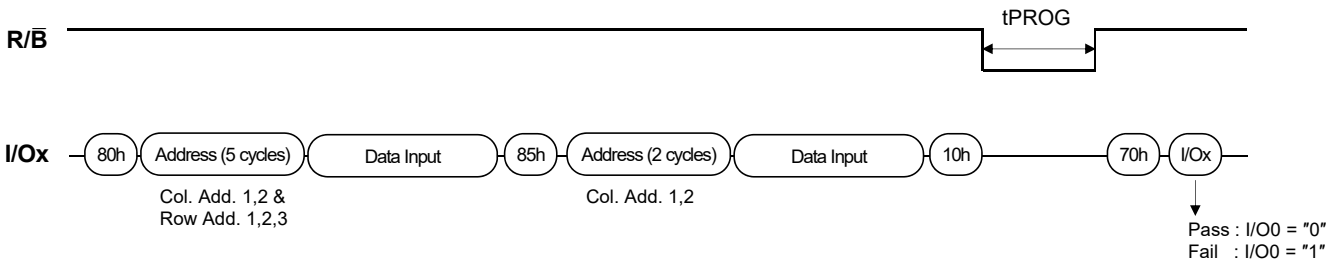


Figure 10. Program Operation with Random Data Input Sequence

4.6 Guidance to User Spare Program

During NOP program, data that is designated to user spare area shall use random data input to change column address. Because NOP is allowed in maximum of 4 times, user spare area is also divided into 4 regions to match up to each NOP area. Main data is divided using NOP, and randomized while programming the data. Although user spare that is included in each NOP is also randomized, randomization done between main data and user spare data are different as below Figure 11. Therefore, for each NOP, column address change shall be kept to match up correct NOP with NOP user spare.

At first, input 512 bytes of data for NOP0, then user spare data for NOP0 shall be inputted after changing of column address using Random Data Input. After programming of data, using of Random Data Input to return back to starting address of NOP1 main data shall be done. Secondly, input 512 bytes of NOP1 data, using Random Data Input to change column address to user spare data for NOP1 inputting. After programming of user spare data for NOP1, return back to starting address of NOP2 main data starting address. NOP2 and NOP3 shall follow same manner as above.

If user decide to follow same order as programming order during data out, read out NOP0 area first, then using of Random Data Output to change column address to read out NOP0 user spare area shall be followed.

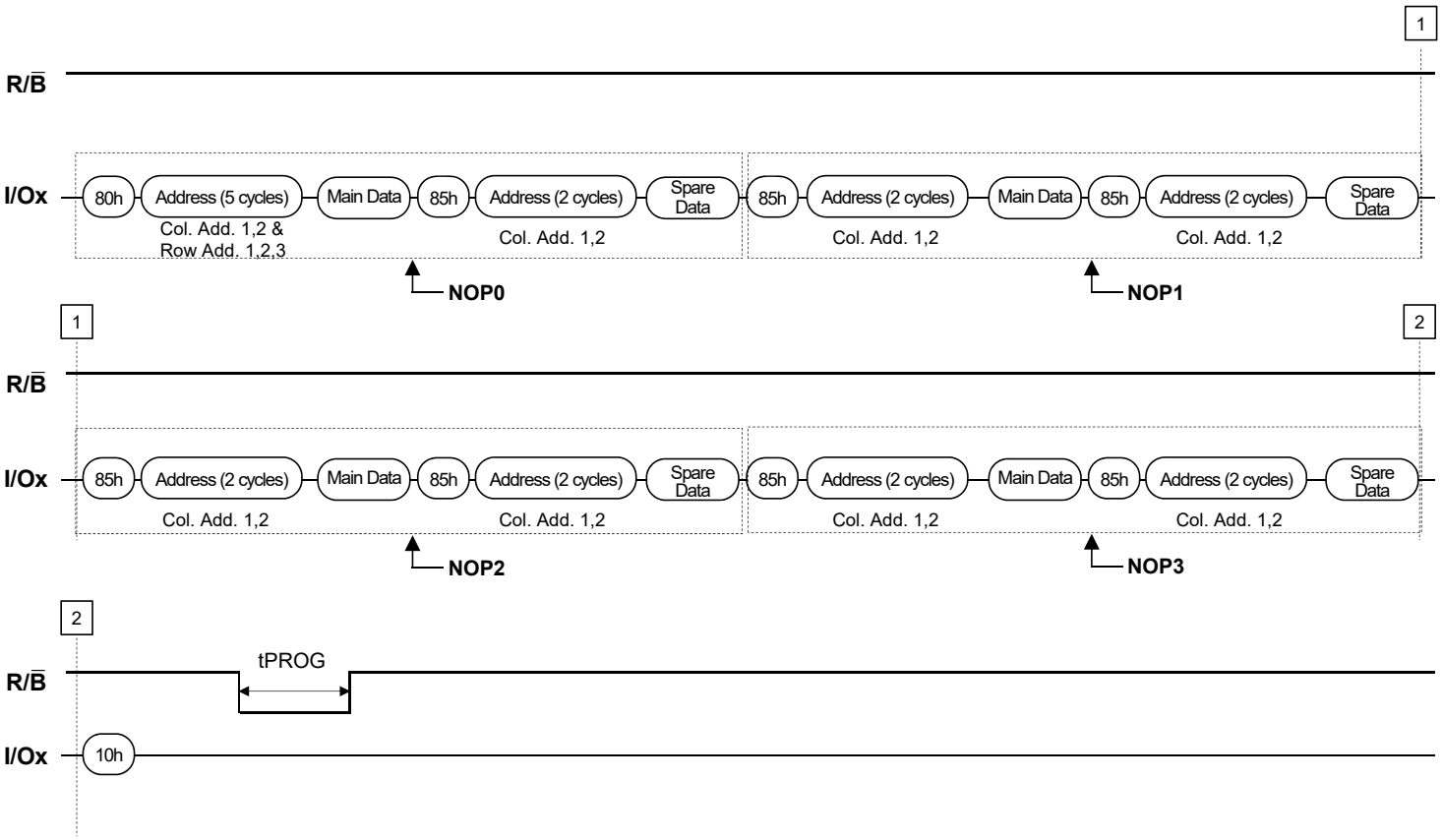


Figure 11. User Spare Program Sequence

[Table 15] NOP Chunk Column Address

NOP0	Column	NOP1	Column	NOP2	Column	NOP3	Column
Chunk0	000~01F	Chunk0	400~41F	Chunk0	800~81F	Chunk0	C00~C1F
Chunk1	020~03F	Chunk1	420~43F	Chunk1	820~83F	Chunk1	C20~C3F
Chunk2	040~05F	Chunk2	440~45F	Chunk2	840~85F	Chunk2	C40~C5F
Chunk3	060~07F	Chunk3	460~47F	Chunk3	860~87F	Chunk3	C60~C7F
Chunk4	080~09F	Chunk4	480~49F	Chunk4	880~89F	Chunk4	C80~C9F
Chunk5	0A0~0BF	Chunk5	4A0~4BF	Chunk5	8A0~8BF	Chunk5	CA0~CBF
Chunk6	0C0~0DF	Chunk6	4C0~4DF	Chunk6	8C0~8DF	Chunk6	CC0~CDF
Chunk7	0E0~0FF	Chunk7	4E0~4FF	Chunk7	8E0~8FF	Chunk7	CE0~CFF
Chunk8	100~11F	Chunk8	500~51F	Chunk8	900~91F	Chunk8	D00~D1F
Chunk9	120~13F	Chunk9	520~53F	Chunk9	920~93F	Chunk9	D20~D3F
Chunk10	140~15F	Chunk10	540~55F	Chunk10	940~95F	Chunk10	D40~D5F
Chunk11	160~17F	Chunk11	560~57F	Chunk11	960~97F	Chunk11	D60~D7F
Chunk12	180~19F	Chunk12	580~59F	Chunk12	980~99F	Chunk12	D80~D9F
Chunk13	1A0~1BF	Chunk13	5A0~5BF	Chunk13	9A0~9BF	Chunk13	DA0~DBF
Chunk14	1C0~1DF	Chunk14	5C0~5DF	Chunk14	9C0~9DF	Chunk14	DC0~DDF
Chunk15	1E0~1FF	Chunk15	5E0~5FF	Chunk15	9E0~9FF	Chunk15	DE0~DFF
Chunk16	200~21F	Chunk16	600~61F	Chunk16	A00~A1F	Chunk16	E00~E1F
Chunk17	220~23F	Chunk17	620~63F	Chunk17	A20~A3F	Chunk17	E20~E3F
Chunk18	240~25F	Chunk18	640~65F	Chunk18	A40~A5F	Chunk18	E40~E5F
Chunk19	260~27F	Chunk19	660~67F	Chunk19	A60~A7F	Chunk19	E60~E7F
Chunk20	280~29F	Chunk20	680~69F	Chunk20	A80~A9F	Chunk20	E80~E9F
Chunk21	2A0~2BF	Chunk21	6A0~6BF	Chunk21	AA0~ABF	Chunk21	EA0~EBF
Chunk22	2C0~2DF	Chunk22	6C0~6DF	Chunk22	AC0~ADF	Chunk22	EC0~EDF
Chunk23	2E0~2FF	Chunk23	6E0~6FF	Chunk23	AE0~AFF	Chunk23	EE0~EFF
Chunk24	300~31F	Chunk24	700~71F	Chunk24	B00~B1F	Chunk24	F00~F1F
Chunk25	320~33F	Chunk25	720~73F	Chunk25	B20~B3F	Chunk25	F20~F3F
Chunk26	340~35F	Chunk26	740~75F	Chunk26	B40~B5F	Chunk26	F40~F5F
Chunk27	360~37F	Chunk27	760~77F	Chunk27	B60~B7F	Chunk27	F60~F7F
Chunk28	380~39F	Chunk28	780~79F	Chunk28	B80~B9F	Chunk28	F80~F9F
Chunk29	3A0~3BF	Chunk29	7A0~7BF	Chunk29	BA0~BBF	Chunk29	FA0~FBF
Chunk30	3C0~3DF	Chunk30	7C0~7DF	Chunk30	BC0~BDF	Chunk30	FC0~FDF
Chunk31	3E0~3FF	Chunk31	7E0~7FF	Chunk31	BE0~BFF	Chunk31	FE0~FFF
User Spare0 Chunk0	1000~101F	User Spare1 Chunk0	1040~105F	User Spare2 Chunk0	1080~109F	User Spare3 Chunk0	10C0~10DF
User Spare0 Chunk1	1020~103F	User Spare1 Chunk1	1060~107F	User Spare2 Chunk1	10A0~10BF	User Spare3 Chunk1	10E0~10FF

4.7 Page Re-program Operation

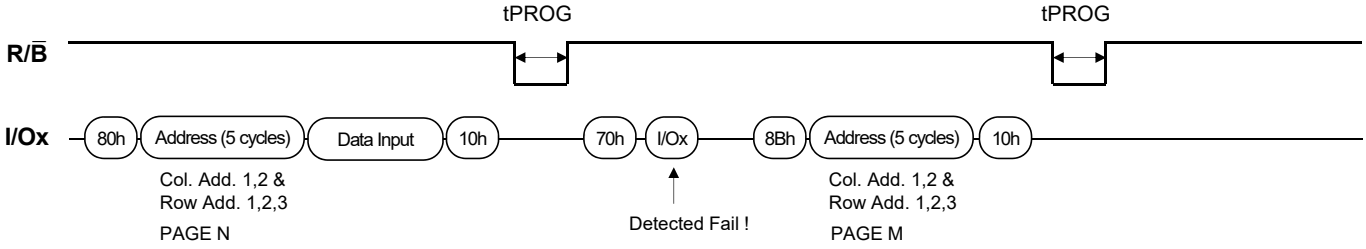
This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle. On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm “10h”

The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The “program confirm” command (10h) initiates the re-programming process.

The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the R$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

*** Page Re-program**



*** Page Re-program with data manipulation**

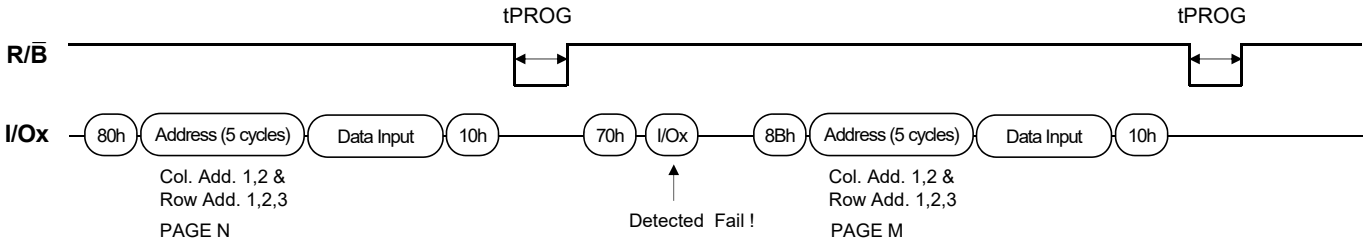


Figure 12. Page Re-program

4.8 Copy-Back Program Operation

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and reloading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block.

The copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 4,352 bytes data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling $\overline{RE}$, or copyback command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed.

When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy- Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, one bit error correction is recommended for the use of Copy- Back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, $\overline{WP}$ value is don't care during Read for copy-back, while it must be set to Vcc When performing the program.

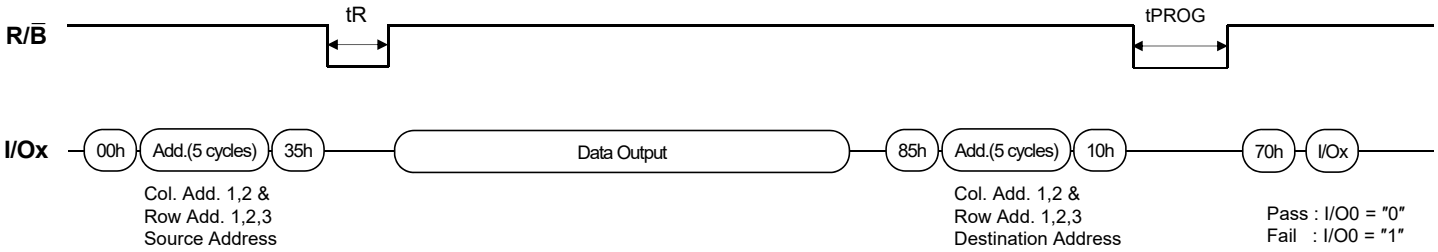


Figure 13. Copy-Back Read with Optional Data Readout

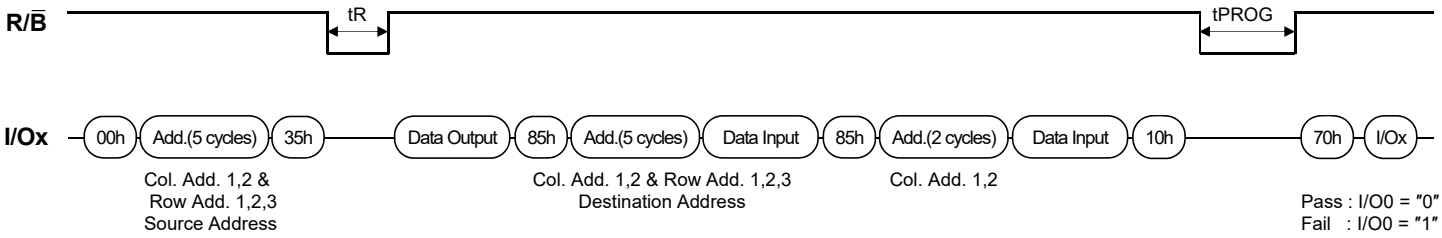


Figure 14. Copy-Back Program with Random Data Input Sequence

NOTE :
1) Because of sub plane structure of the device, copy-back read requires additional read time of 30μs. For detailed value, please refer to copy-back read timing values shown in Table "Copy-Back Function – Read Characteristics".

[Table 16] Copy-Back Function – Read Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Single Plane Read	tR	-	70	365	μs

4.9 Block Erase Operation

The Block Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command (60h). Only addresses A_{19} to A_{29} are valid while A_{13} to A_{18} are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of an erase by monitoring the $\overline{RB}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

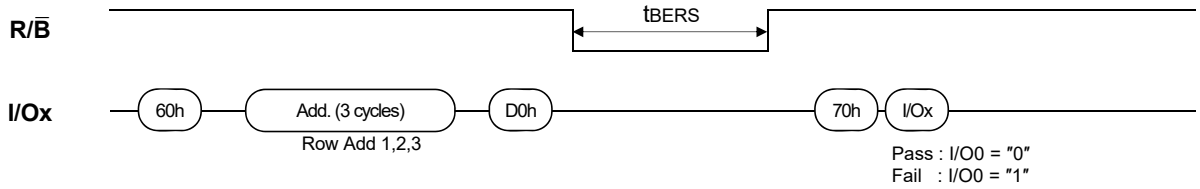


Figure 15. Block Erase Sequence

4.10 Read Status Register

The device contains a Status Register which may be read to find out whether read program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/ O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to following table for specific Status Register definitions. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

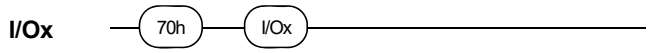


Figure 16. Read Status Register Sequence

[Table 17] Status Register Definition

SR bit	Page Program	Block Erase	Page Read	OTP Block Protect	Definition
I/O 0	Pass / Fail	Pass / Fail	Not use	Program Pass / Fail	Pass : ″0″ Fail : ″1″
I/O 1	Not use	Not use	Not use	Not use	Reserved
I/O 2	Not use	Not use	Not use	Not use	Reserved
I/O 3	Not use	Not use	Not use	Not protected / Protected	OTP not protected : “0” OTP protected : “1”
I/O 4	Not Use	Not Use	1 (default) or 2	Not Use	(1) Page recommended to rewrite : “1” Page normal / on-die ECC disabled : “0” (2) Page uncorrectable : “1” Page normal / on-die ECC disabled : “0”
I/O 5	Program in progress / Completed	Not Use	Not use	Not use	Busy : ″0″ Ready : ″1″
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : ″0″ Ready : ″1″
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Protected : ″0″ Not Protected : ″1″

NOTE :

1.I/O0 : This bit is only valid for Program and Erase operations. If cleared to zero, then the last command was successful. If set to one, then the last command failed. For two plane operation, it indicates that one or both planes failed. The Read Status Enhanced (78h) operation can be used to determine with plane the operation failed. If a block is protected, this bit should fail

2.I/O3 : This bit indicates whether the OTP is lock down, and should be cleared to zero, when not in OTP mode, or FF command is issued, or on power up. This bit should be set to one after lock down command is issued, or when OTP operation command is issued and OTP is lock down.

3.I/O4 : If the internal ECC is On, this bit indicates if the last pare read contained ECC errors. It is supported in two modes of 1(default) or 2, which is selectable using feature register address 90h bit [4]. These registers can be modified using the Set Feature command.

- 1 : The 1 indicates if one page has a high ECC error count and recommending to rewrite the page. If set to one, it is recommended to rewrite the entire page. If cleared to zero, it is in normal state (internal ECC enabled, error counts are in safe level), or UECC, or internal ECC disabled.
- 2 : The 2 indicates if the page has more ECC errors than then internal engine can correct (UECC). If set to one, it is ECC Fail and the page is uncorrectable. If cleared to zero, then it is in normal state (internal ECC enabled, safely working), or internal ECC disabled.

4. I/O5 : If set to one then there is no array operation in progress. If cleared to zero, then there is a command being progressed.

5. I/O7 : If set to one, then the device is not write protected. If cleared to zero, then the device is write protected. This bit shall always be valid regardless of state of the R/$\overline{B}$. For Status Enhanced command, signal follows $\overline{WP}$ pin.

4.11 Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the following cases on a specific die of a multi-dice stack configurations (single $\overline{CE}$), in case of concurrent operations When 4Gbit dies are stacked(*) to form 8Gbit DDP or 16Gbit QDP (single $\overline{CE}$), it is possible to run a first operation on the first 4Gbit, then activate a concurrent operation on the second (or third or fourth) device. (examples: Erase while Read, Read while Program, etc.) - on a specific plane in case of multi-plane operations in the same die.

Following Figure 17 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest. Read Status Enhanced command only shows block status of previously accessed block before issuing the command.

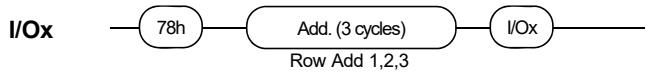


Figure 17. Read Status Register Sequence

[Table 18] Status Register Definition

SR bit	Page Program	Block Erase	Page Read	OTP Block Protect	Definition
I/O 0	Pass / Fail	Pass / Fail	Not use	Not use	Pass : ″0″ Fail : ″1″
I/O 1	Not use	Not use	Not use	Not use	Reserved
I/O 2	Not use	Not use	Not use	Not use	Reserved
I/O 3	Not use	Not use	Not use	Not protected / Protected	OTP not protected : “0” OTP protected : “1”
I/O 4	Not Use	Not Use	1 (default) or 2	Not Use	(1) Page recommended to rewrite : “1” Page normal / on-die ECC disabled : “0” (2) Page uncorrectable : “1” Page normal / on-die ECC disabled : “0”
I/O 5	Program in progress / Completed	Not Use	Not use	Not use	Busy : ″0″ Ready : ″1″
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : ″0″ Ready : ″1″
I/O 7	Write Protect / PBP / VBP	Write Protect / PBP / VBP	Write Protect / PBP / VBP	Write Protect / PBP / VBP	Protected : ″0″ Not Protected : ″1″

NOTE :
I/O4, I/O5 defines ECC status

4.12 Read ID

4.12.1 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. The 5-byte Read ID configuration are supported: The device operation mode (5-byte) is selected through cam setting.

4.12.2 Legacy Read ID

Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it.

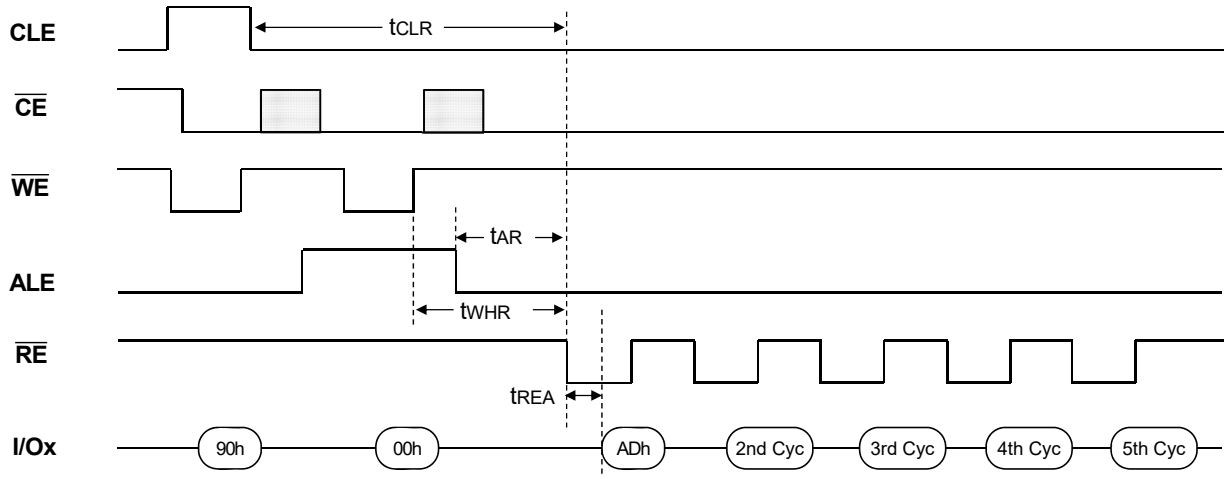


Figure 18. Read ID Sequence

4.12.3 00h Address ID Cycle

[Table 19] 00h Address ID cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle
S8F4G08UAM	ADh	DCh	00h	1Ah	00h

[Table 20] 00 Address ID Definition Table

Device Identifier Byte	Description
1st Byte	Manufacturer Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type
4th Byte	Page Size, Block Size, Spare Size, Organization
5th Byte	Multiplane information

[Table 21] 3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
Cell Type	2 Level Cell					0	0		
Reserved	1	0	0	0	0				

[Table 22] 4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (without spare area)	2KB							0	1
	4KB							1	0
Block Size (without spare area)	128KB	0		0	0				
	256KB	0		0	1				
Spare Area Size	128B					0	1		
	256B					1	0		
Organization	X8		0						

[Table 23] 5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Reserved	Reserved	0	0	0	0			0	0

4.13 Reset Operation

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin changes to low for tRST after the Reset command is written.

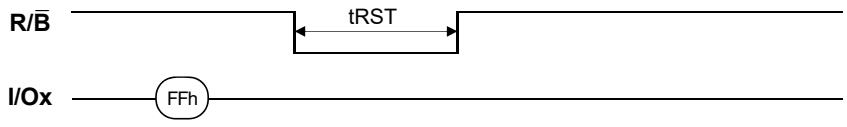


Figure 19. Reset Sequence

4.14 Read Parameter Page Operation

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. The whole data structure is repeated at least three times.
The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.
The Read Status may be used to check the status of Read Parameter Page during execution. After completion of the Read Status command, 00h shall be issued by the host on the command line to continue with the data output flow for the Read Parameter Page command. Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

4.14.1 Parameter Page Data Structure Definition

Following table defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page.
For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

[Table 24] Parameter page data

Byte	O/M	Description
	Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copy back 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copy back 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Cache Read commands 0 1 = supports Page Cache Program command
10-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-79		Reserved (0)
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles

Byte	O/M	Description
	Memory organization block	
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
	Electrical parameters block	
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	t_{PROG} Maximum page program time (µs)
135-136	M	t_{BERS} Maximum block erase time (µs)
137-138	M	t_R Maximum page read time (µs)
139-140	M	t_{CCS} Minimum change column setup time (ns)
141-163		Reserved (0)
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Note : “O” stands for Optional, “M” for Mandatory

4.15 Set Feature and Get Feature

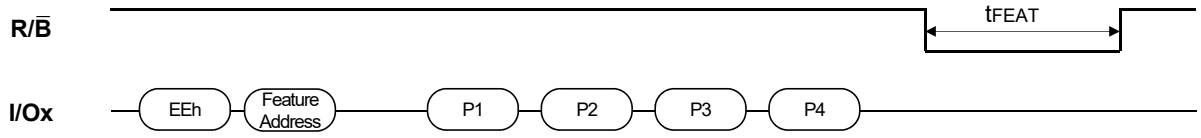


Figure 20. Set Feature Sequence

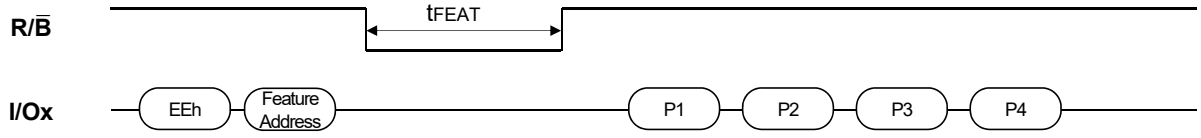


Figure 21. Get Feature Sequence

[Table 25] Feature Address 90h – Array Operation Mode (P1 register)

Bits	Field Name	Function	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	On-die ECC Status Description Select	On-die ECC Read Status Option Select	0	
3	ECC_EN	ECC enable	1	1 : On-die ECC enable (Default) 0 : On-die ECC disable
2	Reserved	Reserved	0	
1	OTP Protection	OTP Area Protect	00	00 : TOP is not selected (Default) 01 : OTP Area Entry 11 : OTP Protection (Lock)
0	Normal vs. OTP operation	Norma (Array Operation)		

Note :
1) P2/P3/P4 are 00h.
2) A software Reset command (FFh) does not alter the content of the 90h feature register.
3) Bit4 of Feature Address 90h allows user to select if Read Status DQ4 shows 1 (default) or 2.
- Page Recommended to Rewrite : “1”, Page Normal/On-die ECC disabled : “0”
- Page Uncorrectable : “1”, Page Normal/On-die ECC disabled : “0”

[Table 26] Feature Address 80h – Programmable Output Strength Mode (P1 register)

Bits	Field Name	Function	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	Reserved	Reserved	0	
3	Output Driver Strength	Output Strength Selection	0000	0000 : Full Strength, 18Ω output impedance, (Default) 0001 : 75% of Full Strength, 25Ω output impedance 0010 : 50% of Full Strength, 35Ω output impedance 0011 : 25% of Full Strength, 50Ω output impedance
2				
1				
0				

Note :
1) P2/P3/P4 are 00h.
2) A software Reset command (FFh) does not alter the content of the 90h feature register.

4.16 Output Driver Strength

The device may be configured with multiple driver strengths with Set Features command. Device supports Underdrive, Nominal, Overdrive1, and Overdrive2 options and each settings comply with the output driver requirements followed in this section.

[Table 27] Output Driver Strength Settings

Setting	Driver Strength	V_{CC}
18 Ohms	2.0x = 18 Ohms	3.3V
25 Ohms	1.4x = 25 Ohms	
35 Ohms	1.0x = 35 Ohms	
50 Ohms	0.7x = 50 Ohms	

[Table 28] Output Driver Strength Impedance Values

Output Strength	Symbol	Vout to V_{SS}	Minimum	Nominal	Maximum	Unit
Underdrive	Rpd	0.2 x V_{CC}	18.4	45.0	80.0	
		0.5 x V_{CC}	25.0	50.0	100.0	
		0.8 x V_{CC}	32.0	57.0	136.0	
	Rpu	0.2 x V_{CC}	32.0	57.0	136.0	
		0.5 x V_{CC}	25.0	50.0	100.0	
		0.8 x V_{CC}	18.4	45.0	80.0	
Nominal	Rpd	0.2 x V_{CC}	12.8	32.0	58.0	
		0.5 x V_{CC}	18.0	35.0	70.0	
		0.8 x V_{CC}	23.0	40.0	95.0	
	Rpu	0.2 x V_{CC}	23.0	40.0	95.0	
		0.5 x V_{CC}	18.0	35.0	70.0	
		0.8 x V_{CC}	12.8	32.0	58.0	
Overdrive1	Rpd	0.2 x V_{CC}	9.3	22.3	40.0	
		0.5 x V_{CC}	12.6	25.0	50.0	
		0.8 x V_{CC}	16.3	29.0	68.0	
	Rpu	0.2 x V_{CC}	16.3	29.0	68.0	
		0.5 x V_{CC}	12.6	25.0	50.0	
		0.8 x V_{CC}	9.3	19.0	40.0	
Overdirve2	Rpd	0.2 x V_{CC}	7.0	16.2	28.7	
		0.5 x V_{CC}	9.0	18.0	36.0	
		0.8 x V_{CC}	11.8	21.0	50.0	
	Rpu	0.2 x V_{CC}	11.8	21.0	50.0	
		0.5 x V_{CC}	9.0	18.0	36.0	
		0.8 x V_{CC}	7.0	14.0	28.7	

Test conditions for impedance value verifications are listed on Following table.

[Table 29] Test Conditions for Impedance Values

Condition	Temperature	V_{CC}	Process
Minimum Impedance	T_{OPER} (Min)	3.6V	Fast-Fast
Nominal Impedance	+25 °C	3.3V	Typical-Typical
Maximum Impedance	T_{OPER} (Max)	2.7V	Slow-Slow

The pull-up and pull-down impedance mismatch requirements are defined in Following table. Impedance mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage. The testing conditions that shall be used to verify the impedance mismatch requirements are V_{CC}= V_{CC} (min), Vout = V_{CC} x 0.5 and TA is across the full operating range.

[Table 30] Pull-up and Pull-down Output Impedance Mismatch

Driver Strength	Minimum	Maximum	Unit
Overdrive2	0	6.3	Ohms
Overdrive1	0	8.8	Ohms
Nominal	0	12.3	Ohms
Underdrive	0	17.5	Ohms

4.17 One-Time Programmable (OTP)

One-Time Programmable (OTP) entry can be done in two ways, by using vendor command set, or issuing Set Feature (EFh) command with Feature address 90h, P1=09h, P2=00h, P3=00h, P4=00h. Get Feature (EEh) to read out information prior to issue Set Feature (EFh) shall be done, and user shall not change any other I/O options from Get Feature read out data. If OTP sequence is detected, On-die ECC Correction is automatically turned on.

By issuing OTP Protection sequence, a page program sequence with an address of 00h-00h-00h-00h-00h and without Data Input is issued by host system to program the control bit for the OTP area. For OTP block access, block#3 should be addressed (Row Address is 80h – 01h - 00h). The Status Read is then used to poll the status register to determine when the program operation is completed and verify that OTP area is protected. User should issue Set Feature (EFh) command with feature address 90h, P1=0Bh, P2=00h, P3=00h, P4=00h.

Copy-back and Reprogram command are not supported in OTP area.

To exit the OTP area, host must issue the Reset FFh if host entered the OTP using vendor command sequence. If host entered the OTP using Feature address 90h, host can exit the OTP by issuing Set Feature (EFh) command with feature address 90h, P1=08h, P2=00h, P3=00h, P4=00h. A software RESET command (FFh) does not alter the content of 90h feature register, and cannot exit out of OTP mode.

If 2 dies are connected to single CE and OTP entry were made using vendor command sequence, then OTP protect will be applied and operated to 1st die only. Else if 2 dies are connected to single CE and OTP entry made by issuing Set Feature (EFh) command with Feature address 90h, then 1st and 2nd dies are OTP protected at the same time, because Set Feature is target level command.

OTP mode blocks are required to have higher retention and protection scheme, which elongates tPROG.

4.18 Permanent Block Protection(PBP)

The device contains a CAM with 16 protection parameter setting entries. Each entry enables protection from program and erase of a group of 4 contiguous blocks (64 blocks total) in the main array. PBP command are only accepted if the device is not in OTP mode.

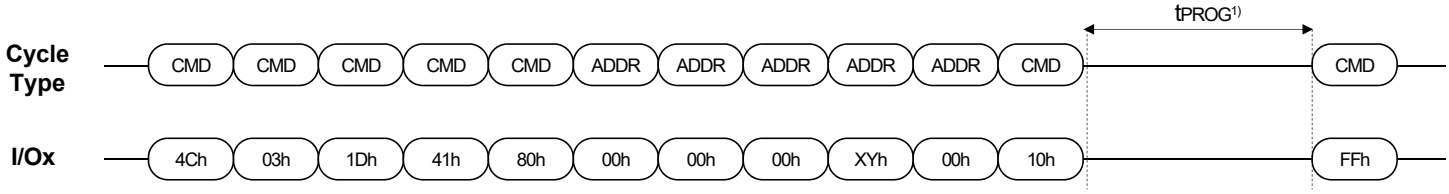
The device ships from the factory with no blocks protected by the PBP method. Because this block protection is permanent, a power-on to power-off sequence does not affect the block protection status after the Permanent block protection command is issued.

The PBP method is used to select a group of blocks in the main array to be protected from program and erase operation. Multiple groups of blocks can be protected at the same time. Once a group of blocks is protected, the group of blocks can no longer be unprotected. During PBP program, operation commands other than Read Status (70h) and Read Status Enhanced (78h) are not supported.

Additional unprotected groups can still be protected using the PBP sequence unless the host issues a Permanent Block Protection Lock-down (PBPLD) command. When this PBPLD command is issued, all groups of blocks protected by PBP are permanently protected from program and erase operations and a PBP operation can no longer be used to protect additional groups.

Each PBP and PBPLD sequence must be exited using the RESET command (FFh).

The PBP parameter settings are stored in CAMs. These settings will be maintained after a power cycle. The PBP method can protect up to 64 blocks (block 0 to 63) organized in groups of 4 contiguous blocks. Each group can be protected individually and are permanently protected. Once a group is protected, the group can no longer be unprotected. The PBP commands are only valid if the device is not in OTP mode. The adding of PBP is only allowed for 1st NAND device. (ex. If 1$\overline{CE}$ QDP, 2nd/3rd/4th LUN cannot add PBP)



Note :
1) PBP blocks are required to have higher retention and protection scheme, which elongates tPROG. Please refer to Table " PBP/OTP-Program Characteristic" for detail value.

Figure 22. PBP Sequence Example

[Table 31] PBP / OTP – Program Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	tPROG	-	550	800	µs

The group of blocks being protected is determined by the value of Y on the fourth address cycle. PBP sequence can be only issued for maximum of 16 times, so if Y value or protected group is selected more than 2 times, then there will be a group that would not be able to be protected by PBP. Issuing of PBPLD sequence will both protect and lock down of the Protected Group.

[Table 32] Fourth Address Cycle (ADDR4) Protection Scheme

Y Value	Protected Group	Protected Block
0000	0	0,1,2,3
0001	1	4,5,6,7
0010	2	8,9,10,11
0011	3	12,13,14,15
0100	4	16,17,18,19
0101	5	20,21,22,23
0110	6	24,25,26,27
0111	7	28,29,30,31
1000	8	32,33,34,35
1001	9	36,37,38,39
1010	10	40,41,42,43
1011	11	44,45,46,47
1100	12	48,49,50,51
1101	13	52,53,54,55
1110	14	56,57,58,59
1111	15	60,61,62,63

[Table 33] Fourth Address Cycle (ADDR4) Protection Command Example

Description	Entry Sequence				CMD Cycle	Address Cycle	CMD Cycle	Read Status or Monitor R/B Output Cycle	Reset (exit)
PBP Sequence	CMD1 (4Ch)	CMD2 (03h)	CMD3 (1Dh)	CMD4 (41h)	80h	00h,00h,00h,0Yh,00h	10h	70h or 78h (Program Operation forces R/$\overline{B}$ Low)	FFh
PBPLD Sequence						00h,00h,00h,1Yh,00h			

Note :
1. When Y value or protected group address is valid, then PBPLD Sequence will protect and lockdown of the protected group at once.

4.19 Block Protection Status Read

The Block Protection Status Read command (7Ah) is followed by 3 address cycles and one data cycle. This register indicates whether a given block (addressed in the Block protection read address command field : Block address) is locked-down, locked or unlocked using the VBP or PBP protection methods.

4.20 Block Lock Status Register

This register indicates whether a given block (addressed in the Block protection read address command field: BA[13:0]) is locked-down, locked or unlocked using the VBP or PBP protection methods.

[Table 34] Block Lock Status Register

Bits	Field Name	Function	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	Permanent Lockdown Status	Permanent Lockdown	0	0: PBP NOT Lockdown 1: PBP Lockdown
3	PBP Lock/Unlock	Permanent Block Protection Lock Status	1	0: The address selected block is locked by PBP 1: The address selected block is not locked by PBP
2	VBP Block-unlock	Volatile Block Protection Block unlocked	1	001: Block is locked down by VBP 010: Block is locked by VBP 101: Block is unlocked, Device is locked-down by VBP 110 (default) : Block is unlocked, Device is not locked- down by VBP
1	VBP Not Locked-down	Volatile Block Protection Not Locked-down	1	
0	VBP Locked-down	Volatile Block Protection Locked-down	0	

4.21 Write protect ($\overline{WP}$) handling

Erase and program operations are a aborted if $\overline{WP}$ is driven low during busy time, and kept low for about 100nsec. Switching $\overline{WP}$ low during this time is equivalent to issuing a Reset command (FFh).

The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/$\overline{B}$ pin will stay low for t_{RST}. At the end of this time, the command register is ready to process the next command, and the status bit SR[I/O 6] will be cleared to "1", while the status bit SR[I/O 7] value will be related to the $\overline{WP}$ value. Erase and program operations are enabled or disabled by setting $\overline{WP}$ to high or low respectively prior to issuing the setup commands (80h or 60h). The level of $\overline{WP}$ shall be set t_{WW} prior to raising the $\overline{WE}$ pin for the set up command. The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low (t_{WW}=100ns,min)

4.22 Firmware SLC

There is a unique given mode for storing Firmware codes for a controller management, called Firmware SLC mode. For Firmware SLC mode, DAh command is newly implemented to provide an user access to specific register area that is designated. To exit from Firmware SLC mode RESET FFh command can be used. If data is programmed with Page Program for Firmware SLC mode, then page read for Firmware SLC mode must be used to read out the data.

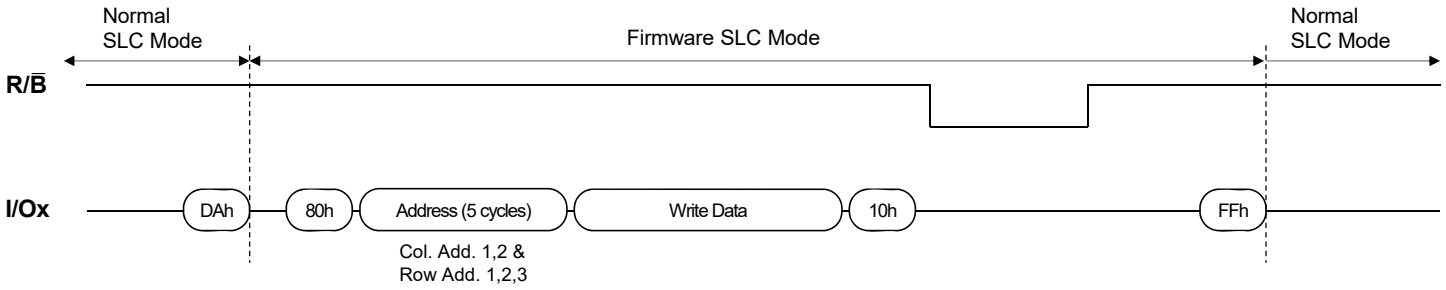


Figure 23. Firmware SLC Mode

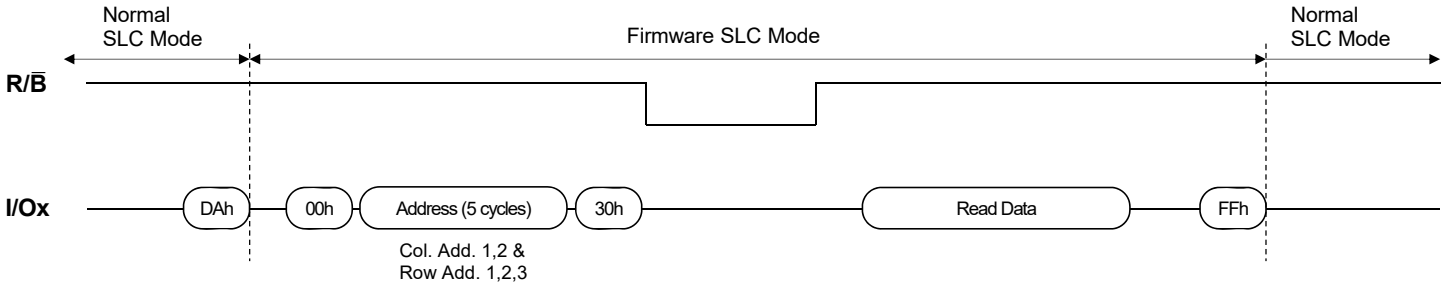


Figure 24. Page Read for Firmware SLC Mode

[Table 35] Firmware SLC Mode – Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	550	800	µs
Number of Partial Program Cycles in the same page	NOP	-	-	1	Cycles
Single Plane Read	t_R	-	55	450	µs
Block Erase Time	t_{BERS}	-	-	10	ms

4.23 Open Block Guideline

When not all the wordlines within the block is programmed, it is called Open block; if all wordlines in the blocks are fully programmed, it is called Closed block. Because remaining wordlines or region of the block is in erased status as a default, voltage difference between last programmed block and the remaining region of the block results read disturbance that causes Vt shift of programmed or erased bits in Open block case.

For S8F4G08UAM product, Open block case shall not be allowed. During program, program all wordlines using dummy to make Close block to ensure NAND reliability. Otherwise, if in case of Open block, it is must to program at least one page of dummy data at the end of last programmed worldline.

Wordline 0	Program
Wordline 1	Program
…	Program
Wordline 57	Program
Wordline 58	Program
Wordline 59	Program
Wordline 60	Program
Wordline 61	Program
Wordline 62	Program
Wordline 63	Program

Figure 25. Closed Block Example

Wordline 0	Program
Wordline 1	Program
…	Program
Wordline 57	Program
Wordline 58	Program
Wordline 59	Program
Wordline 60	**Dummy Program**
Wordline 61	Erase
Wordline 62	Erase
Wordline 63	Erase

Figure 26. Open Block Example

4.24 Small Data Input Guideline

Within NOP1, if input data size is bigger than 2 Bytes, small data input is possible by following two conditions. 1) Data size shall be 2 bytes within single NOP, and 2) 2 byte data input column address shall start from xxxx0h, xxx4h, xxx8h, and xxxCh. For 4KB-single Plane, the size of data input should be more than 4 byte if random data input command is used.

4.25 Ready/$\overline{\text{Busy}}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to t_R (R/$\overline{B}$) and current drain during busy(ibusy), an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.

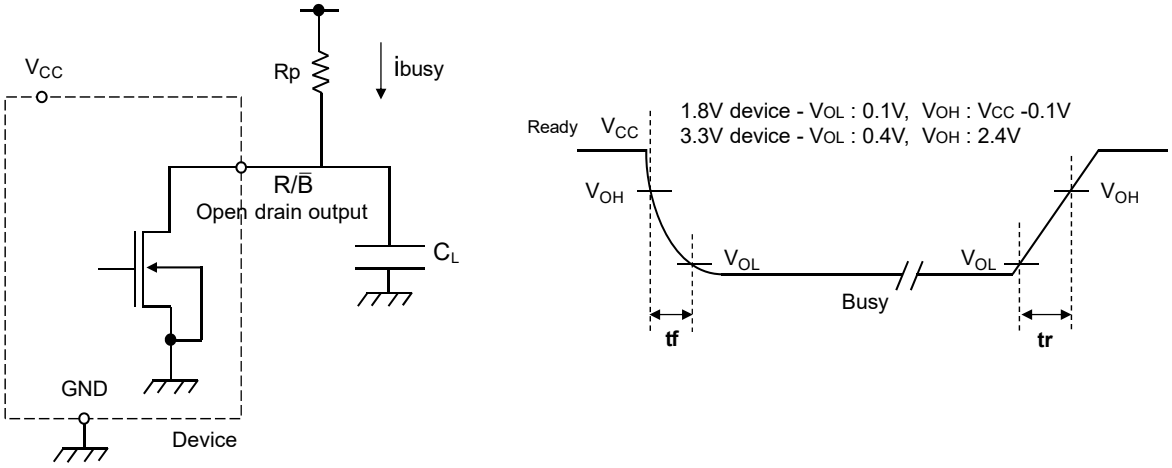
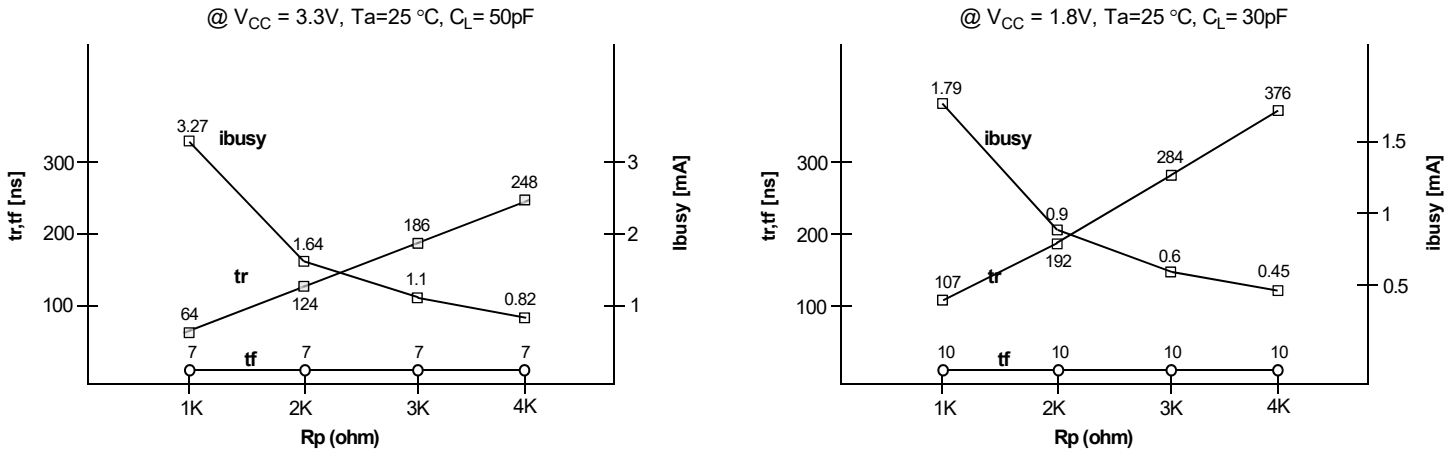


Figure 27. Rp vs tr, tf & Rp vs ibusy



Rp value guidance

$$Rp(min, 3.3V\ device) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

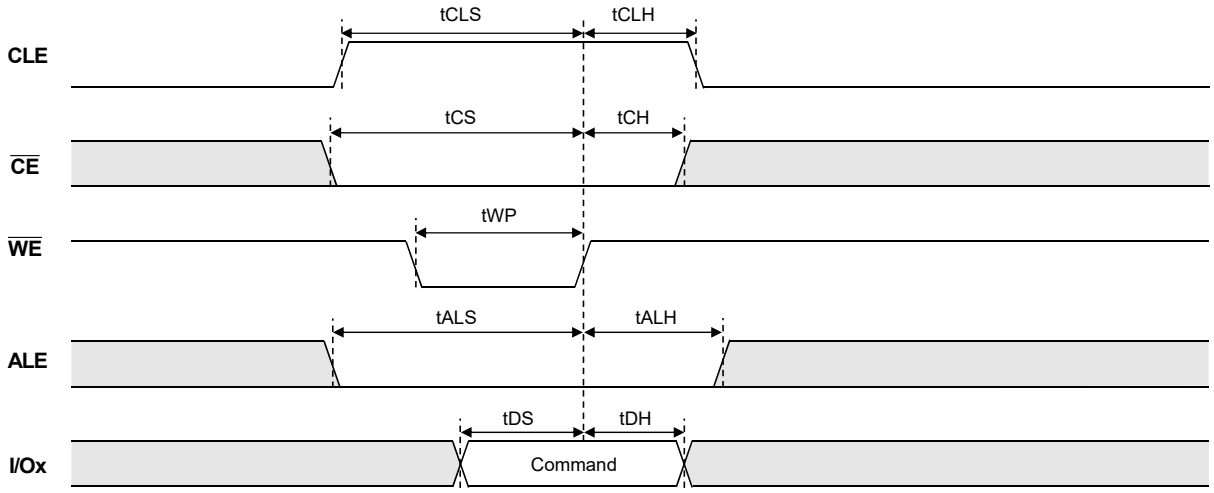
$$Rp(min, 1.8V\ device) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

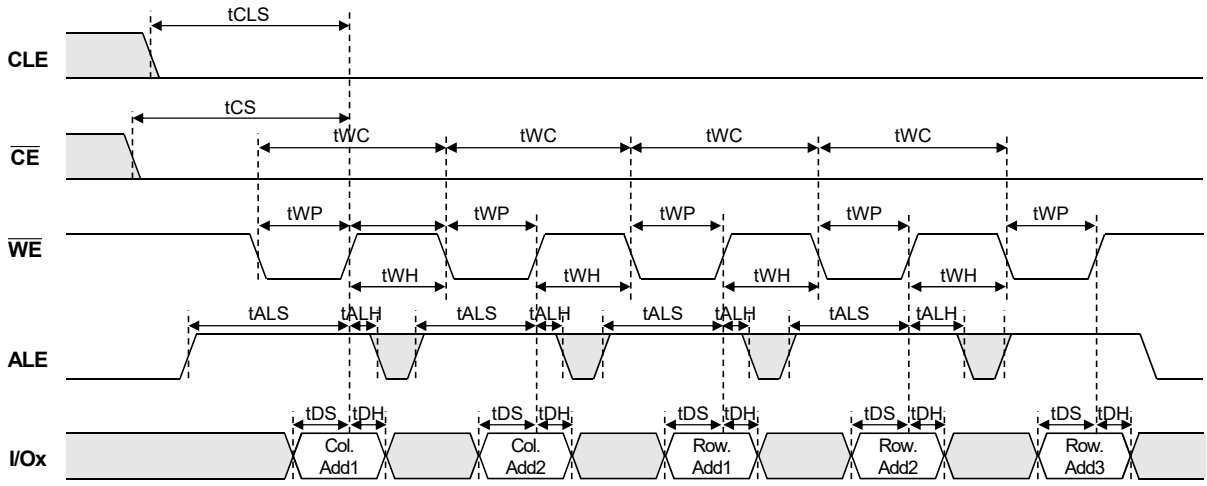
5.0 TIMING DIAGRAM

5.1 General Timing

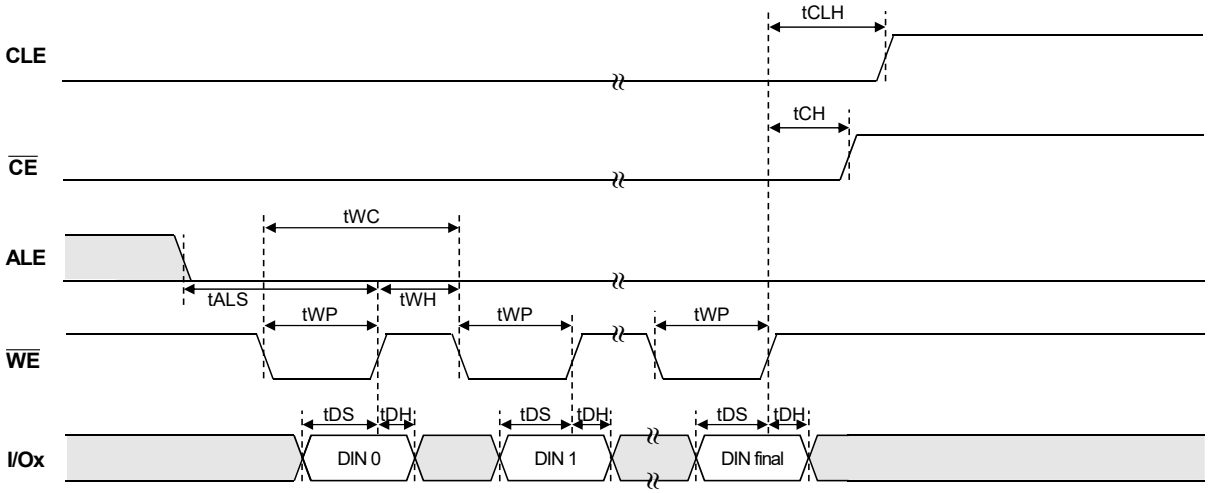
5.1.1 Command Latch Cycle



5.1.2 Address Latch Cycle

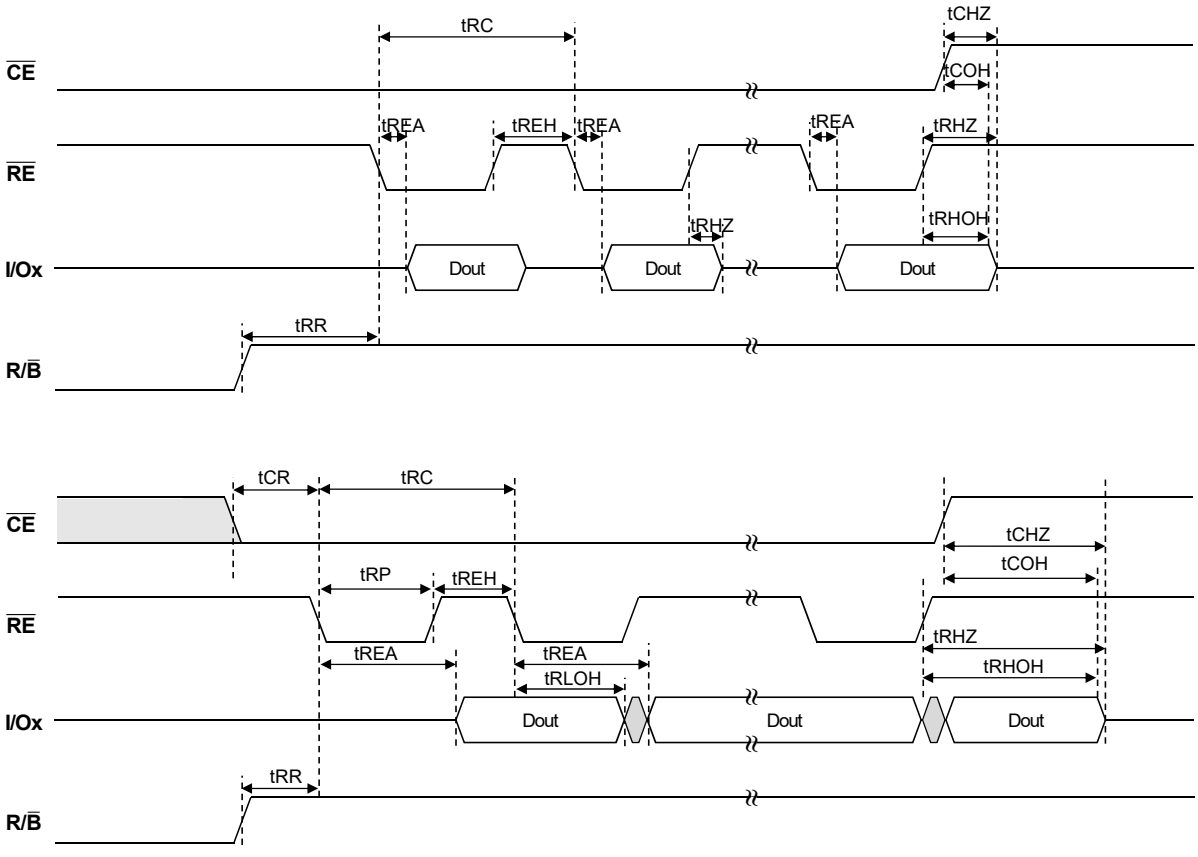


5.1.3 Input Data Latch Cycle



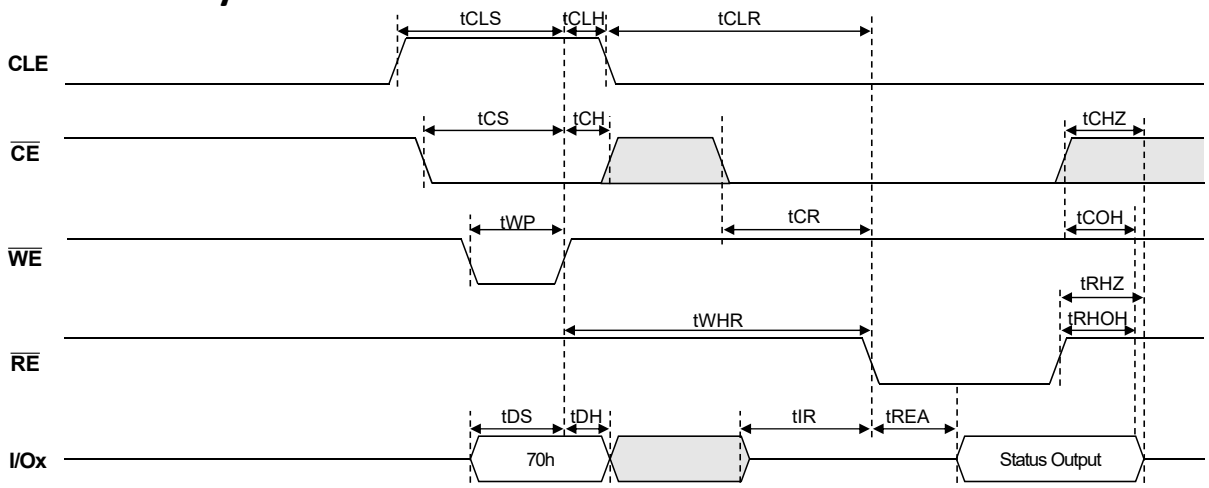
NOTE : Data Input cycle is accepted to data register on the rising edge of $\overline{WE}$, when CLE and $\overline{CE}$ and ALE are low, and device is not Busy state.

5.1.4 Serial Access Cycle after Read

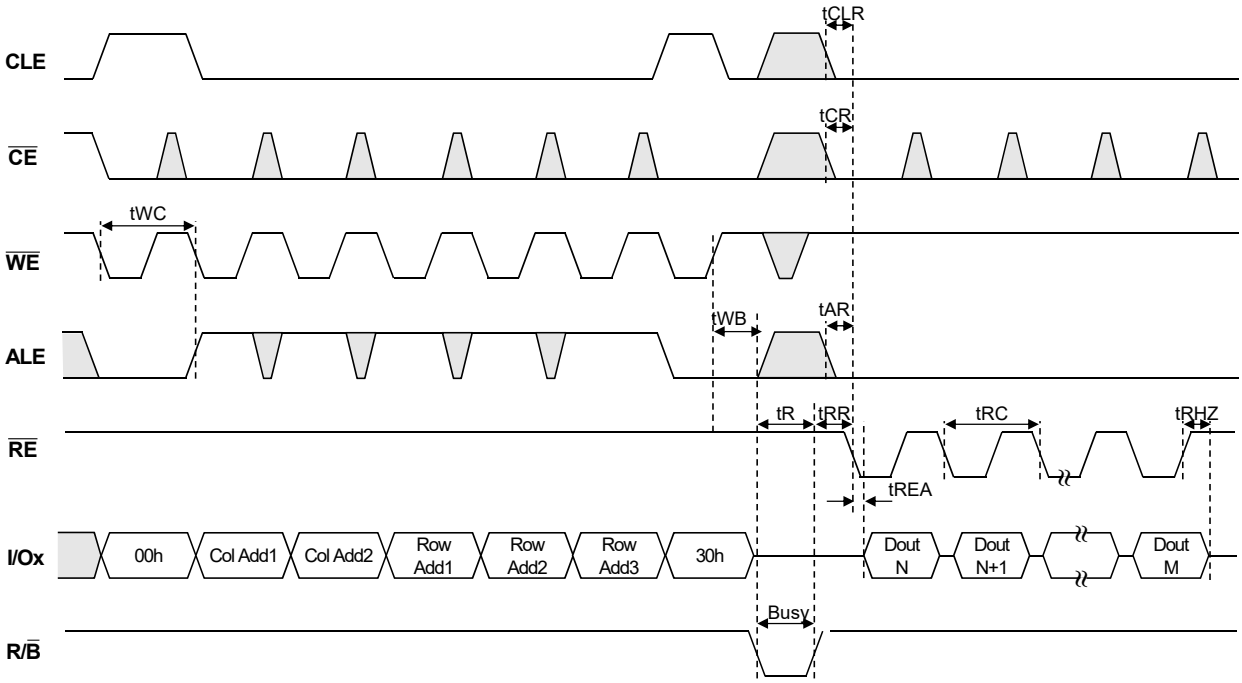


NOTE :
1)Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2) tRHOH starts to be valid when frequency is lower than 33Mhz.
3) tRLOH is valid when frequency is higher than 33MHz

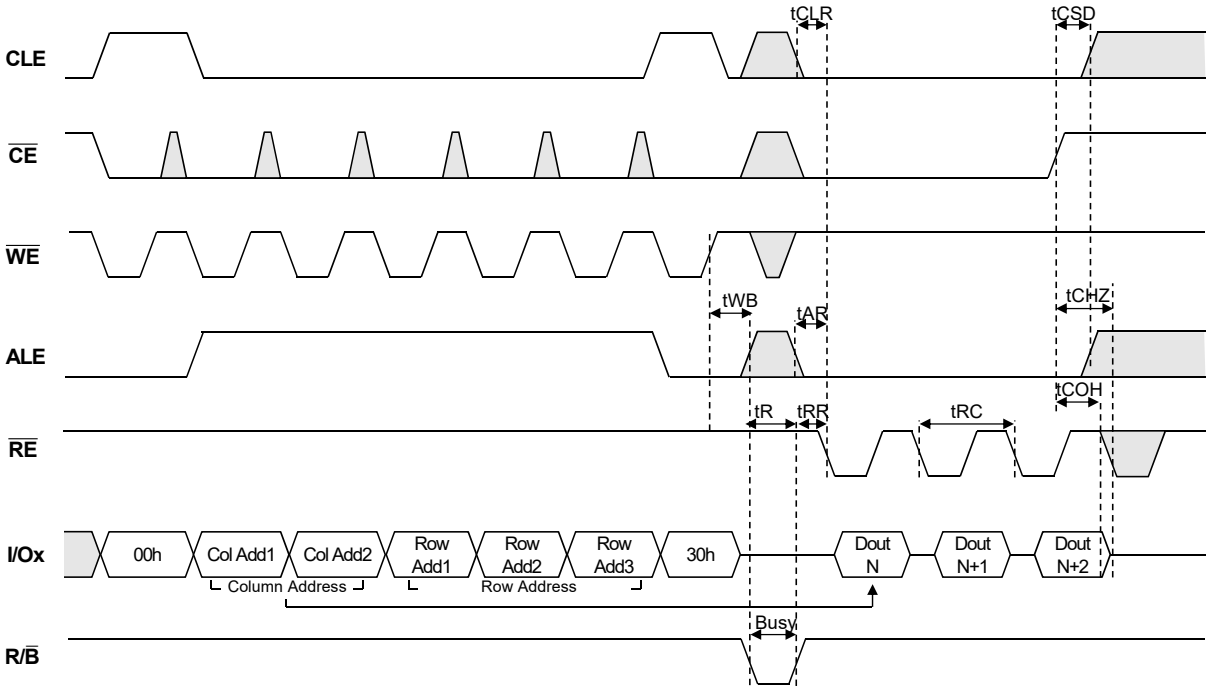
5.2 Read Status Cycle



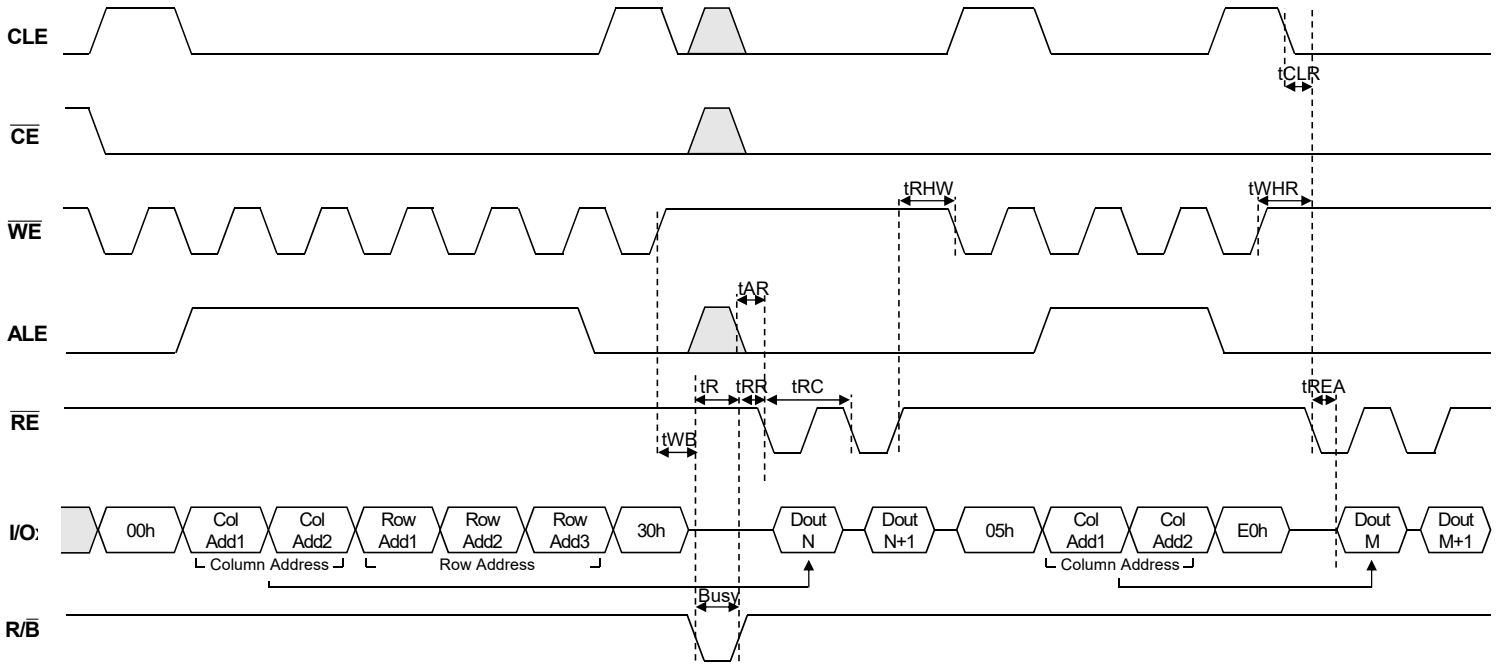
5.3 Read Operation (with $\overline{CE}$ don't care)



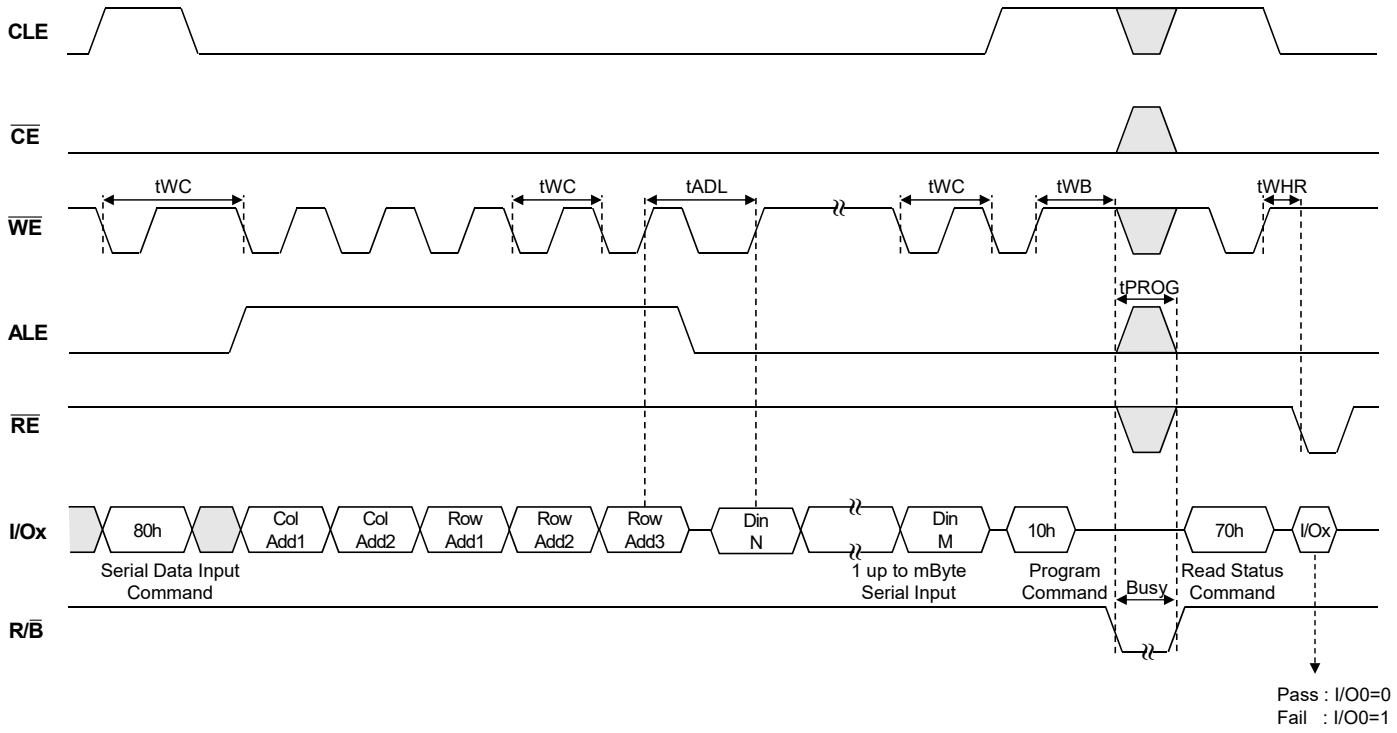
5.4 Read Operation (Intercepted by $\overline{CE}$)



5.5 Random Data Output In a Page Operation

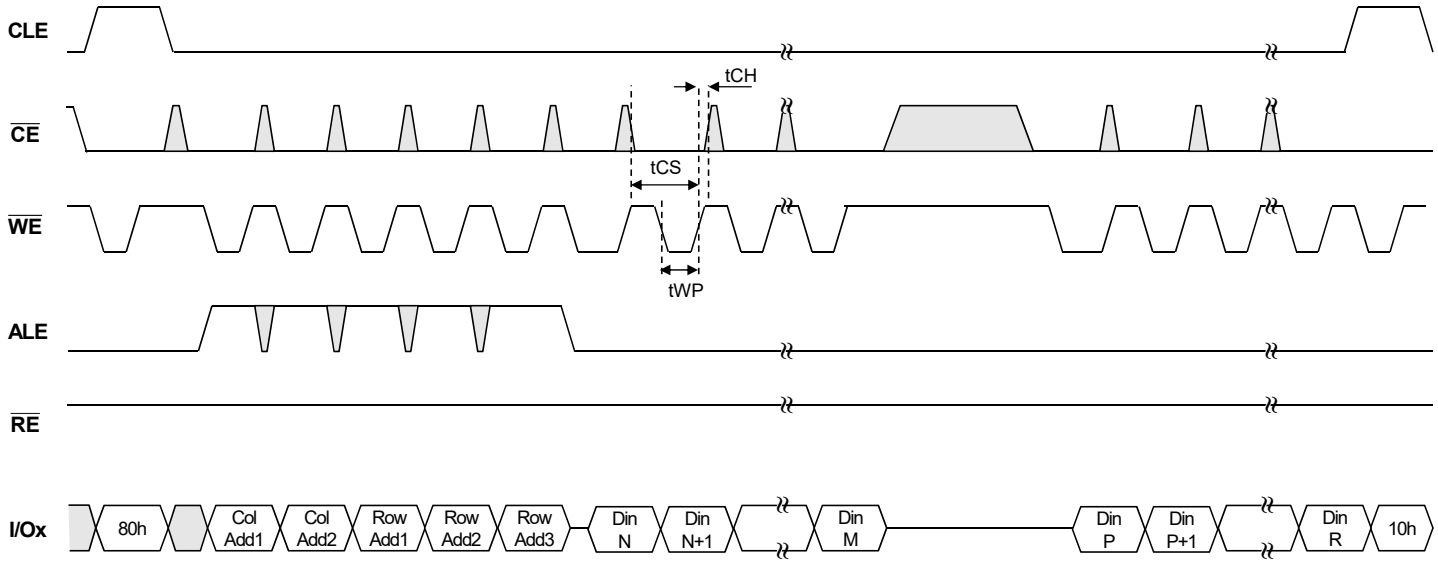


5.6 Page Program Operation



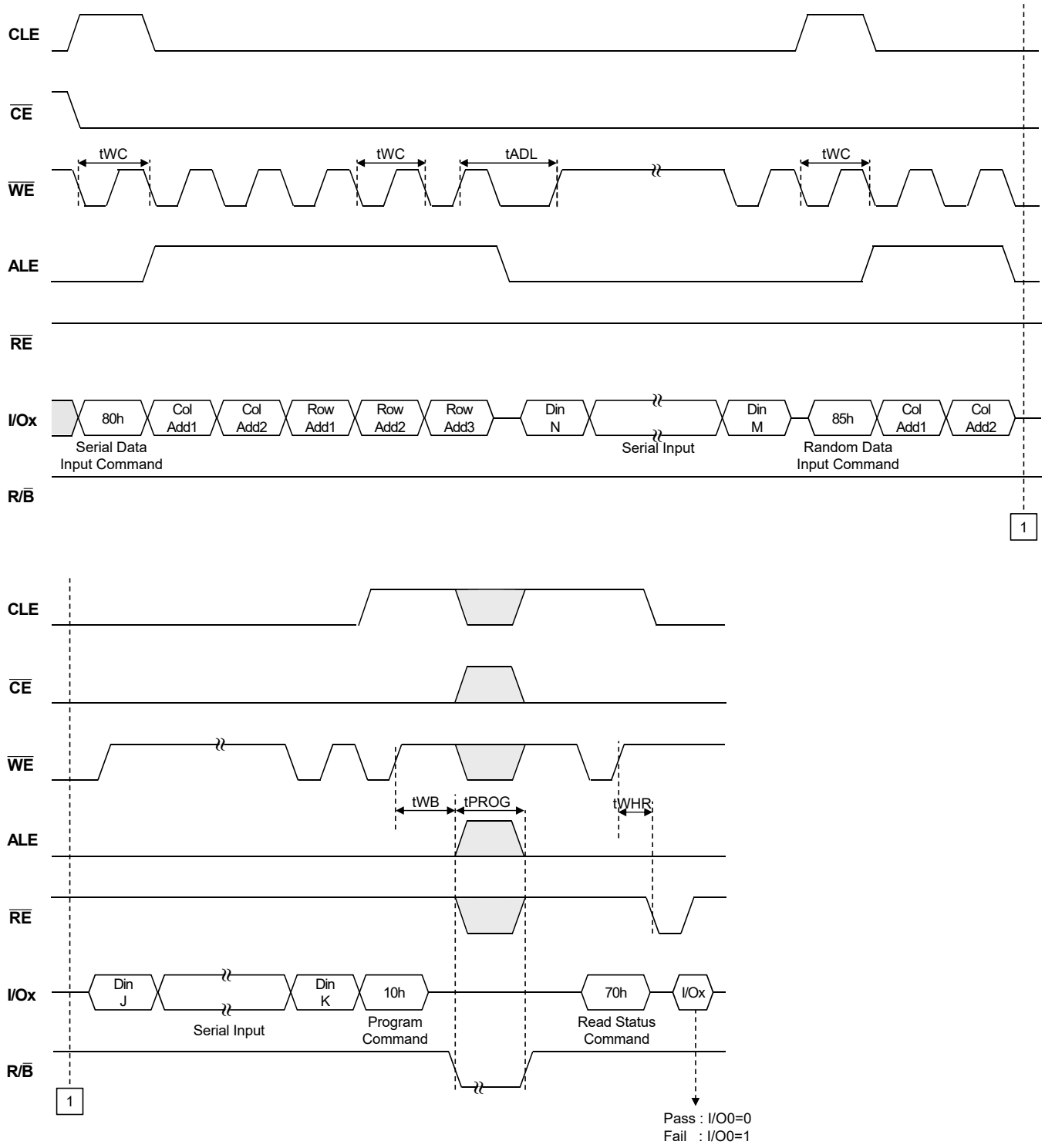
NOTE :
tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

5.7 Page Program Operation (with $\overline{CE}$ don't care)



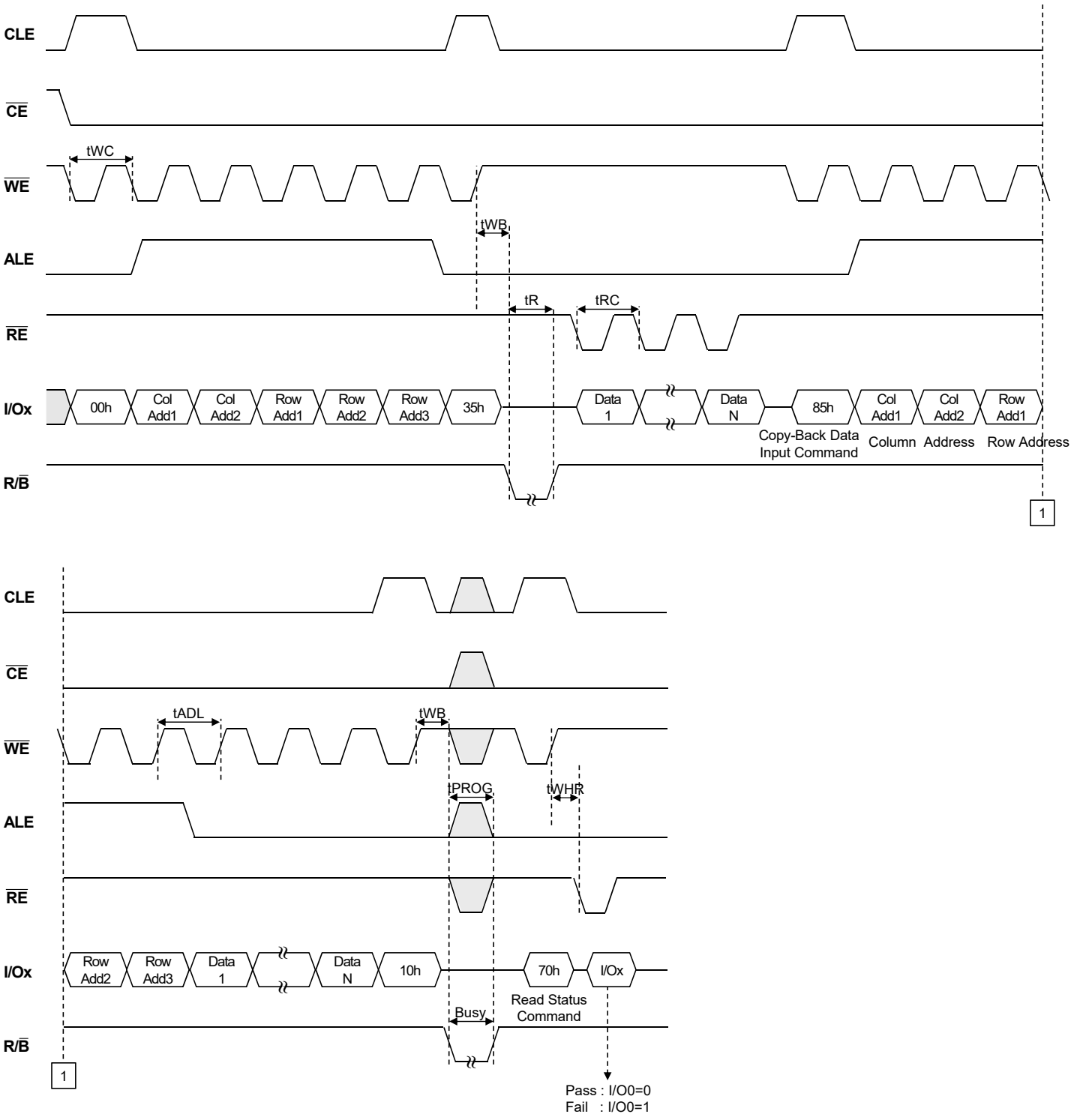
NOTE :
tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

5.8 Page Program Operation with Random Data Input Operation



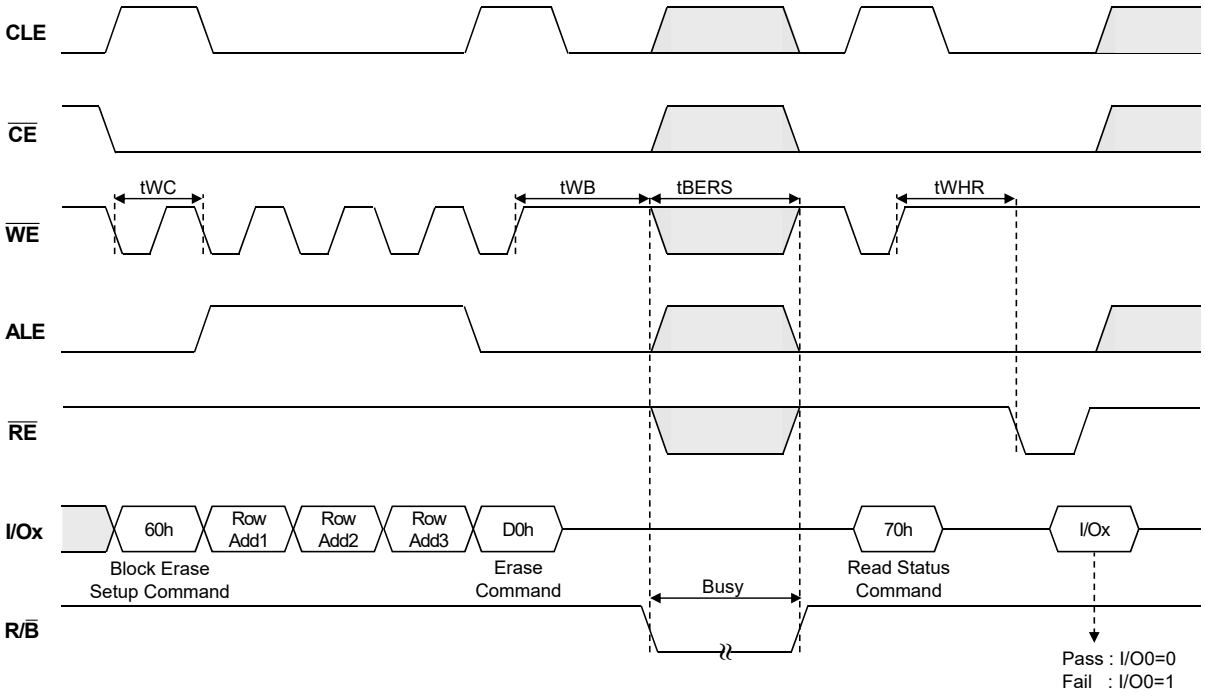
NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
2) Random data input can be performed in a page.

5.9 Copy-Back Program Operation with Random Data Input Operation

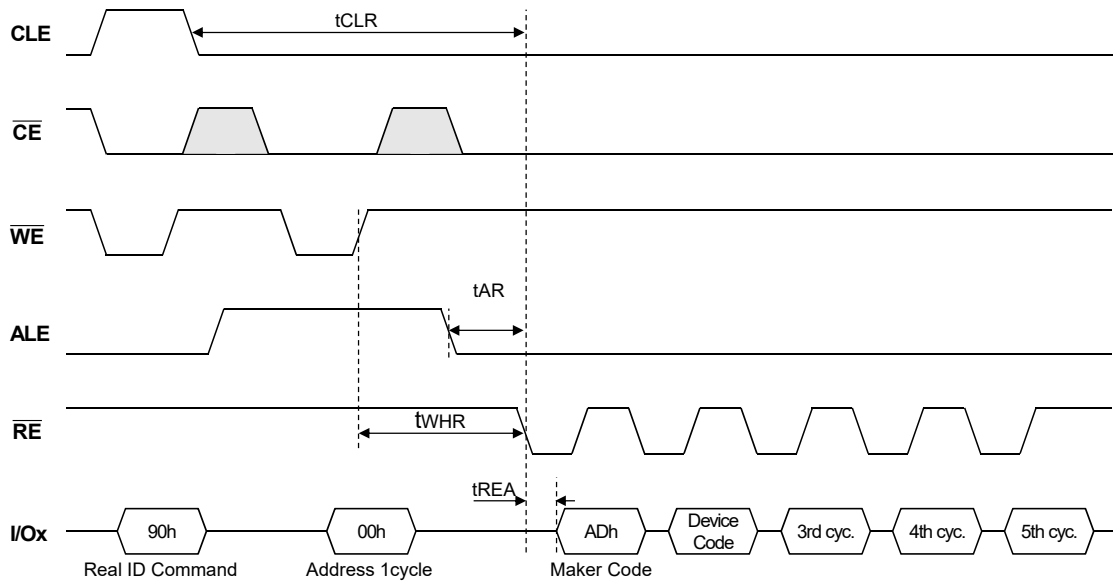


NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
2) Because of sub plane structure of the device, copy-back read requires additional read time of 30µs.

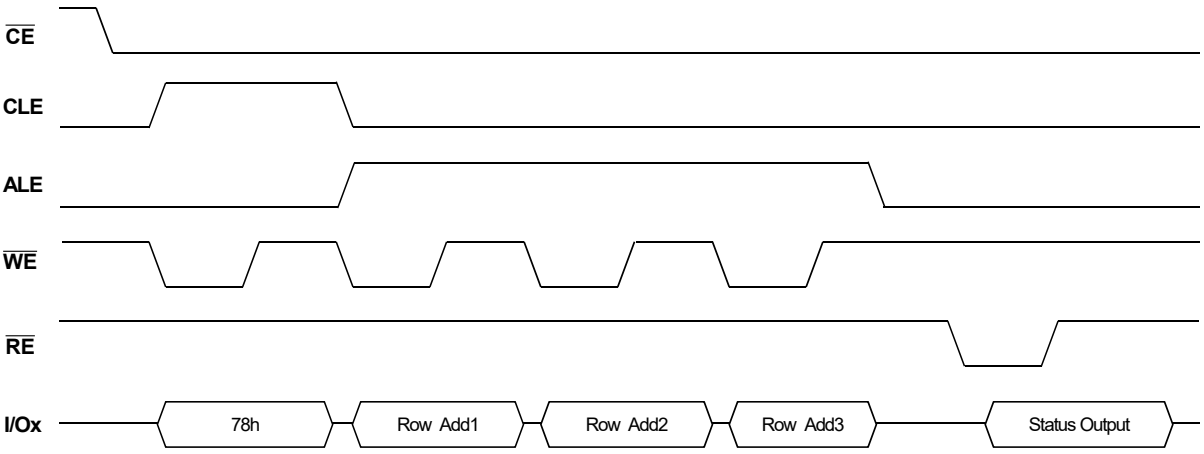
5.10 Block Erase Operation



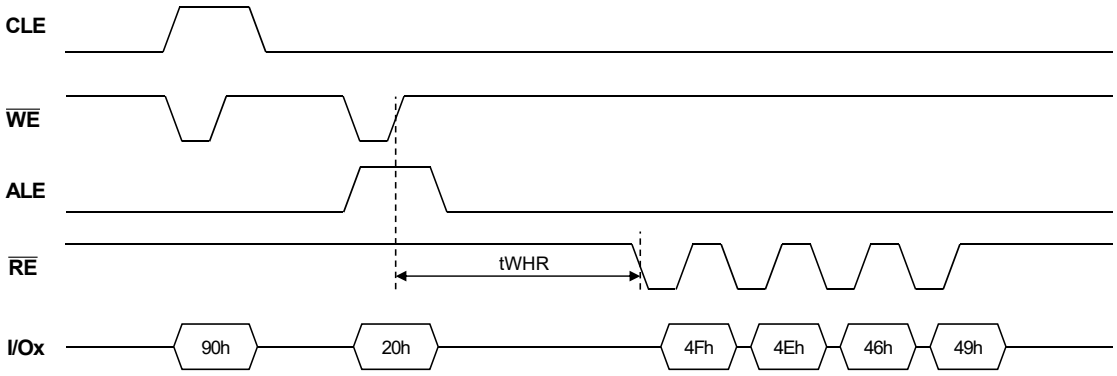
5.11 Read ID Operation



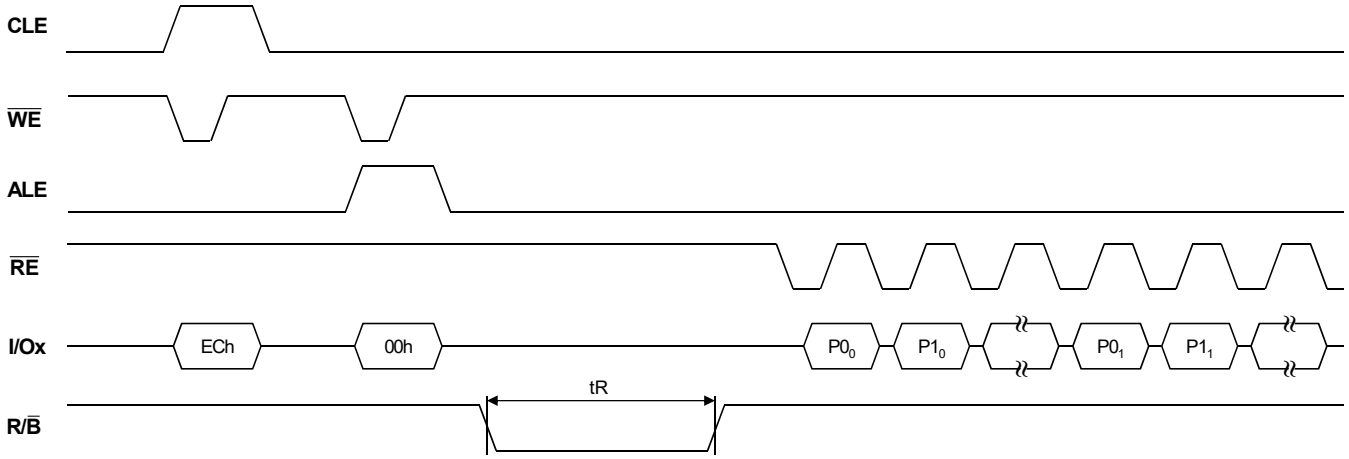
5.12 Read Status Enhanced



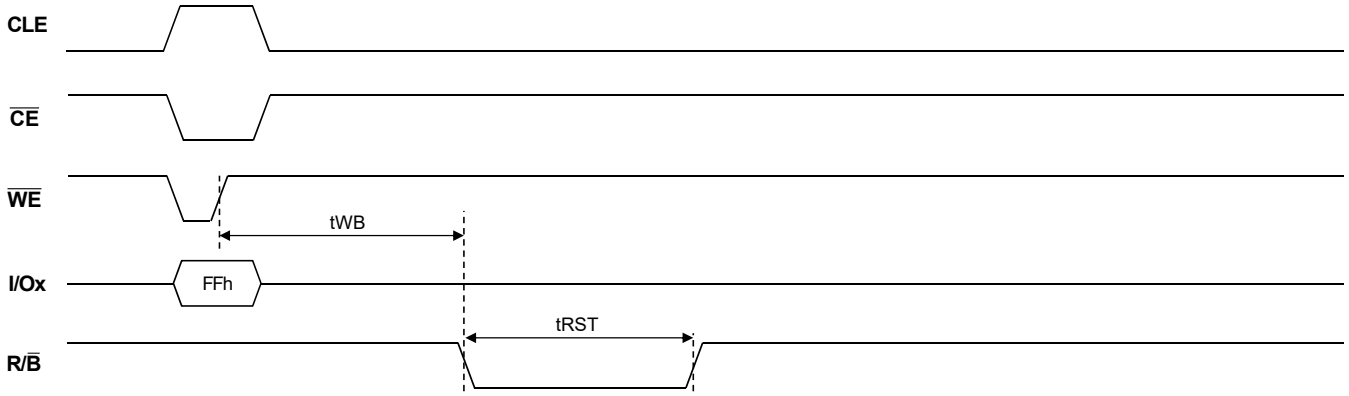
5.13 ONFI Signature Operation



5.14 Read Parameter Page Operation



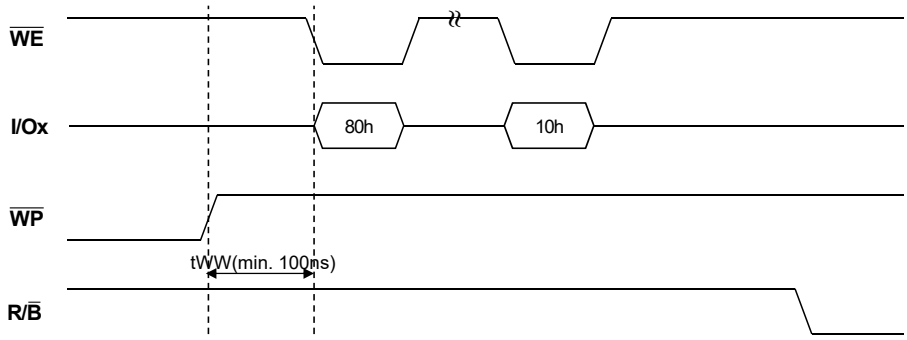
5.15 Reset Operation



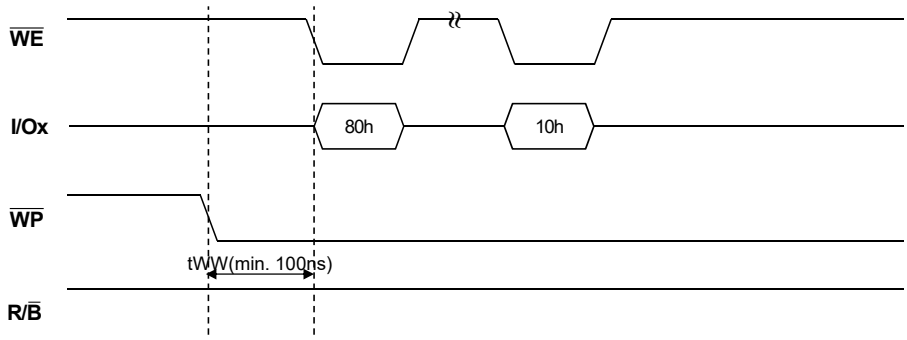
5.16 Write Protection Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min).
The operations are enabled and disabled as follows.

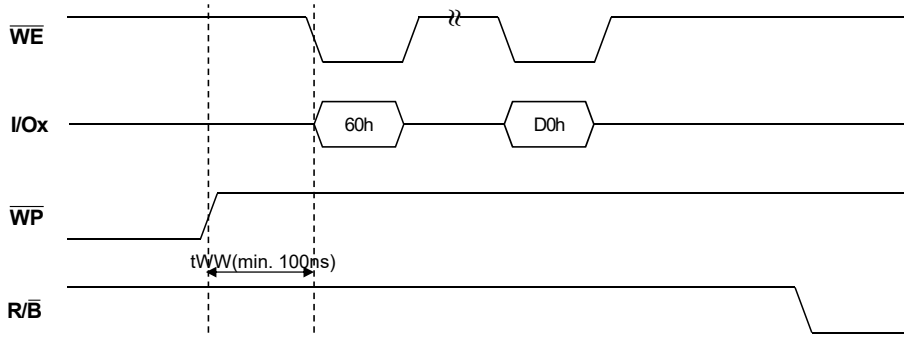
- **Program Enable Mode**



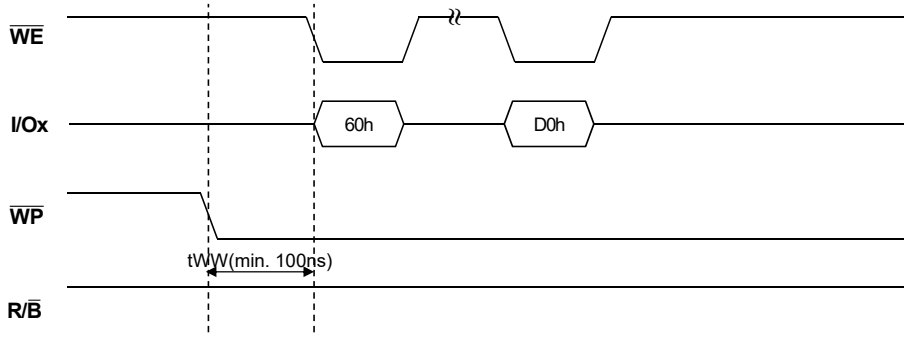
- **Program Disable Mode**



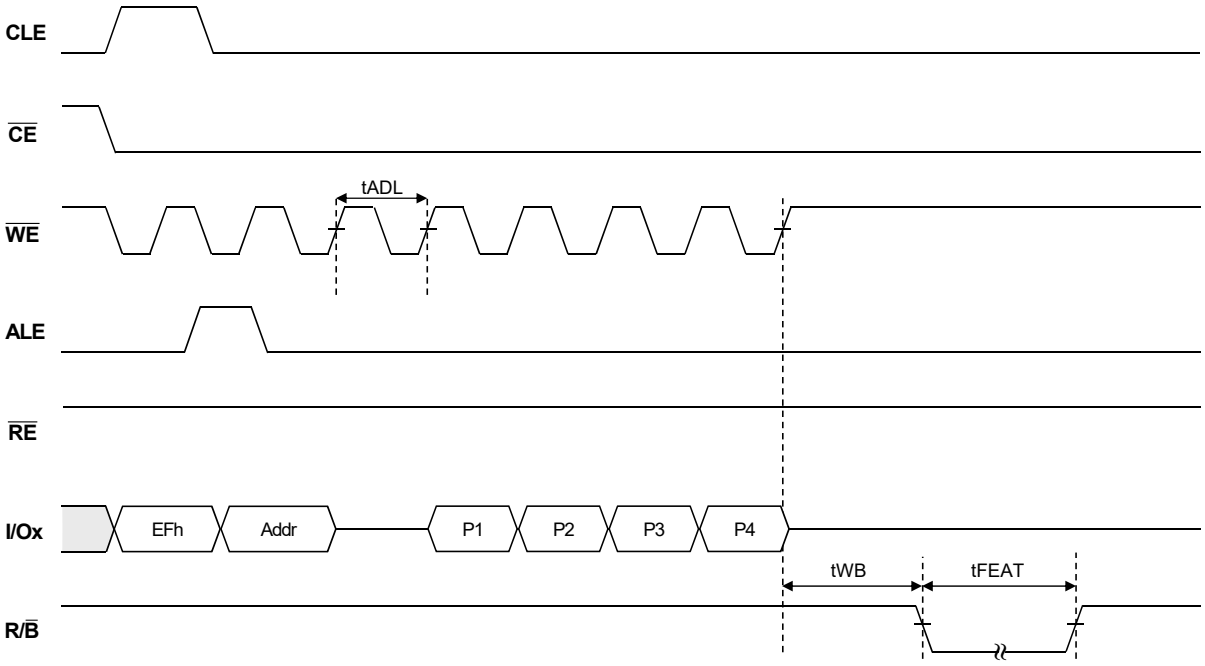
- **Erase Enable Mode**



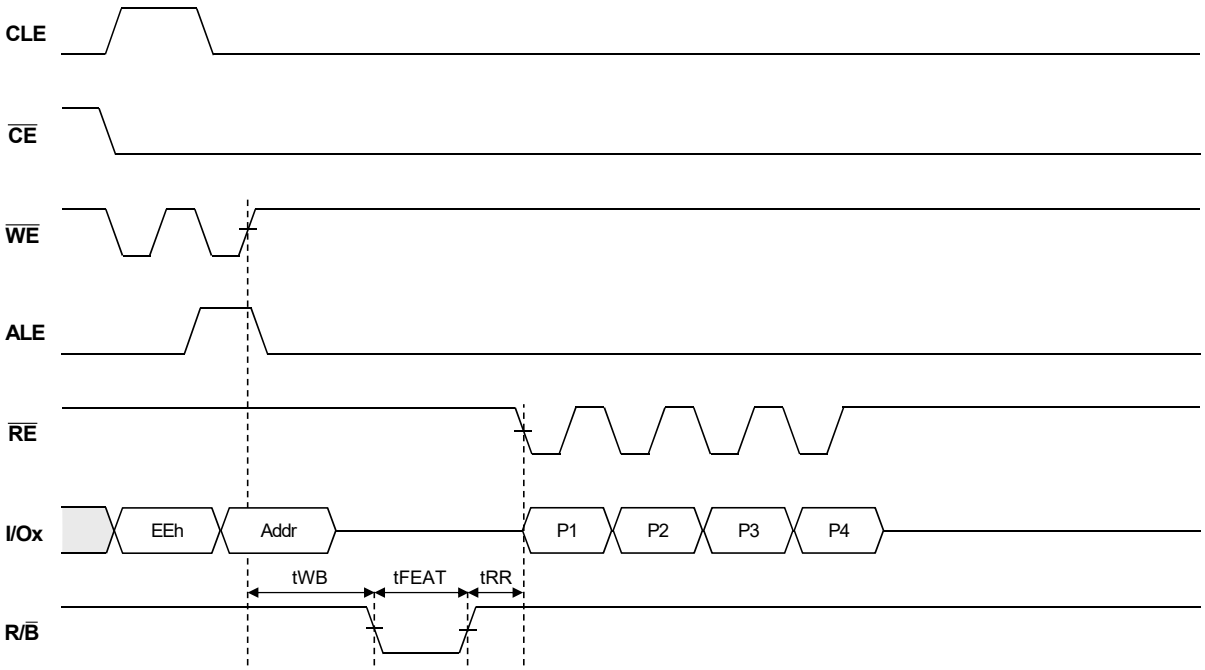
- **Erase Disable Mode**



5.17 Set Feature Timing



5.18 Get Feature Timing



5.19 Block Protection Status Read operation