2Gb A-die NAND Flash

Single-Level-Cell (1bit/Cell)

datasheet

Revision History

Revision No.	History	Draft Date	Remark
1.0	Final version release	Sep. 2018	Final
1.1	Add 48FBGA and 63FBGA	Jan. 2019	Final
1.2	Change spare byte size for 3.3V from 64bytes to 128bytes	Mar. 2019	Final

Table Of Contents

1.0 INTRODUCTION 5
1.1 General Description 5
1.2 Features 5
1.3 Product List 6
1.4 Package 7
1.4.1 Pin Configuration (48 TSOP1) 7
1.4.2 Package Dimensions (48 TSOP1) 7
1.4.3 Package Configuration (63 FBGA) 8
1.4.4 Package Dimensions (63 FBGA) 9
1.4.5 Package Configuration (48 FBGA) 10
1.4.6 Package Dimensions (48 FBGA) 11
1.5 Pin Descriptions 12
1.6 Block Diagram 13
1.7 Memory Array Organization 13
2.0 PRODUCT INTRODUCTION 14
2.1 Valid Block 15
2.2 Absolute Maximum DC Ratings 15
2.3 Recommended Operating Conditions 15
2.4 DC Operating Characteristics 16
2.5 Input / Output Capacitance 16
2.6 AC Test Conditions 16
2.7 Read / Program / Erase Characteristics 17
2.8 AC Timing Parameters Table 17
3.0 NAND FLASH TECHNICAL NOTES 18
3.1 Initial Invalid Block(s) 18
3.2 Identifying Initial Invalid Block(s) 18
3.3 Error in Write or Read Operation 19
4.0 DEVICE OPERATION 21
4.1 Power Up Sequence 21
4.2 Mode Selection 21
4.3 Bus Operation 22
4.4 Page Read Operation 23
4.5 Cache Read Operation 24
4.6 Page Program Operation 25
4.7 Page Re-Program Operation 26
4.8 Multiplane Program Operation 27
4.9 Copy-Back Program Operation 28
4.10 Multiplane Copy-Back Program Operation 29
4.11 Special read for Copy-back Operation 30
4.12 Cache Program Operation 31
4.13 Multiplane Cache Program Operation 32
4.14 Block Erase Operation 34
4.15 Multiplane Block Erase Operation 34
4.16 Read Status Register 35
4.17 Read Status Enhanced 35
4.18 Read ID 36
4.18.1 00h Address ID Definition 36
4.18.2 00h Address ID Cycle 36
4.19 Reset Operation 37
4.20 Read Parameter Page Operation 38
4.20.1 Parameter Page Data Structure Definition 38
4.21 Ready / $\overline{\text{Busy}}$ 40
4.22 Write protect handling 41

Table Of Contents

5.0 TIMING DIAGRAM 42
5.1 General Timing 42
5.1.1 Command Latch Cycle 42
5.1.2 Address Latch Cycle 42
5.1.3 Input Data Latch Cycle 43
5.1.4 Serial Access Cycle after Read 43
5.2 Read Status Cycle 44
5.3 Read Operation (with $\overline{CE}$ don't care) 44
5.4 Read Operation (Intercepted by $\overline{CE}$) 45
5.5 Random Data Output In a Page Operation 45
5.6 Cache Read Operation 46
5.7 Page Program Operation 47
5.8 Page Program Operation (with $\overline{CE}$ don't care) 47
5.9 Page Program Operation with Random Data Input Operation 48
5.10 Copy-Back Program Operation with Random Data Input Operation 49
5.11 Cache Program Operation 50
5.12 Block Erase Operation 51
5.13 Read ID Operation 52
5.14 Read Status Enhanced 52
5.15 ONFI Signature Operation 53
5.16 Read Parameter Page Operation 53
5.17 Reset Operation 53
5.18 Write Protection Operation 54

1.0 INTRODUCTION

1.1 General Description

S8F2G08(U/S)0A is a 2G-bit NAND Flash Memory with spare 128M-bit. The device is offered in 3.3V/1.8V V_{CC}. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 300μs per one page and an erase operation can be performed in typical 3.5ms per one block. Data in the data register can be read out at 25ns cycle time per Byte for 3.3V product or 45ns cycle time per Byte for 1.8V product. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The write operations can be locked using $\overline{WP}$ input pin.

This device supports ONFI 1.0 specification.

The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.

The devices is available to support below three security features:

- OTP (one time programmable) area which is a restricted access area where sensitive data/code can be store permanently.
- Serial number(unique identifier) which allows the devices to be uniquely identified.
- Non-volatile protection to lock sensible data permanently.

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, not described in the datasheet.

1.2 Features

• Voltage Supply
- V_{CC} : 3.3V (2.7V ~ 3.6V)
- V_{CC} : 1.8V (1.7V ~ 1.95V)

• NAND Interface
- Command/Address/Data Multiplexed I/O Port
- X8 I/O Bus
- ONFI 1.0 Command Set

• Organization
[VCC 3.3V]
- Memory Cell Array : (256M + 16M) x 8bit
- Page Size : (2K + 128)Byte
- Data Register : (2K + 128)Byte

[VCC 1.8V]
- Memory Cell Array : (256M + 16M) x 8bit
- Page Size : (2K + 128)Byte
- Data Register : (2K + 128)Byte

• Automatic Program and Erase
[VCC 3.3V]
- Page Program : (2K + 128)Byte
- Block Erase : (128K + 8K)Byte

[VCC 1.8V]
- Page Program : (2K + 128)Byte
- Block Erase : (128K + 8K)Byte

• Page Read Operation
- Random Read : 30μs(Max.)
- Serial Access 3.3V : 25ns(Min.)
- Serial Access 1.8V : 45ns(Min.)

• Fast Write Cycle Time
- Page Program time : 300μs(Typ.)
- Block Erase Time : 3.5ms(Typ.)

• Copy Back Program
- Fast data copy without external buffering

• Cache Program
- Internal buffer to improve the program throughput

• Cache Read
- Internal buffer to improve the read throughput

• Security
- OTP area
- Serial number (unique ID)
- Non-volatile protection

• Electronic Signature
- 1st cycle: Manufacturer Code
- 2nd cycle: Device Code
- 3rd cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages, interleaved Program, Write Cache
- 4th cycle: Page size, Block size, Organization, Spare size, Serial access time
- 5th cycle : ECC, Multi-plane information

• Hardware Data Protection
- Program/Erase Lockout During Power Transitions

• Data Retention
- 50K Program / Erase Cycles
- Data Retention : 10 years (4bit/512B ECC)

• Chip Enable don't care option
- Simple interface with microcontrollers Data Retention

• Package :
- 48 pin TSOP (12 x 20mm)
- 48 Ball FBGA (6.5 x 8.0mm)
- 63 Ball FBGA (9.0 x 11.0mm)

1.3 Product List

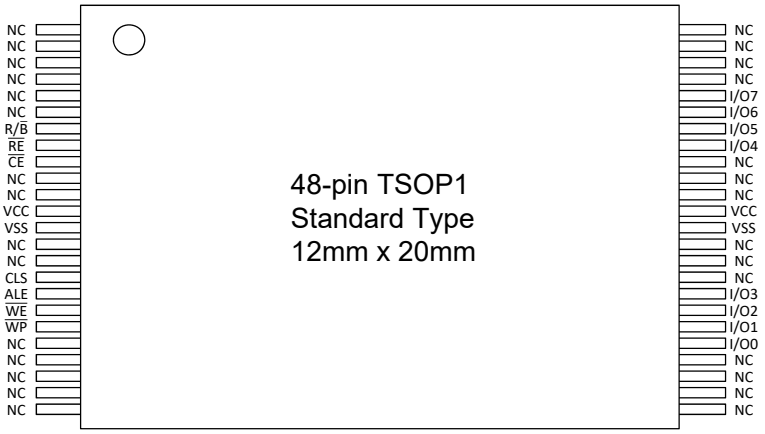
Part Number	Density	Organization	V_{CC} Range	PKG Type
S8F2G08U0A-Yx[1)]B0	2Gb	x8	2.7V ~ 3.6V	48 TSOP1
S8F2G08S0A-Yx[1)]B0	2Gb	x8	1.7V ~ 1.95V	48 TSOP1
S8F2G08U0A-Xx[1)]B0	2Gb	x8	2.7V ~ 3.6V	48 FBGA
S8F2G08S0A-Xx[1)]B0	2Gb	x8	1.7V ~ 1.95V	48 FBGA
S8F2G08U0A-Bx[1)]B0	2Gb	x8	2.7V ~ 3.6V	63 FBGA
S8F2G08S0A-Bx[1)]B0	2Gb	x8	1.7V ~ 1.95V	63 FBGA

1) NOTE :
C : Commercial
I : Industrial

1.4 Package

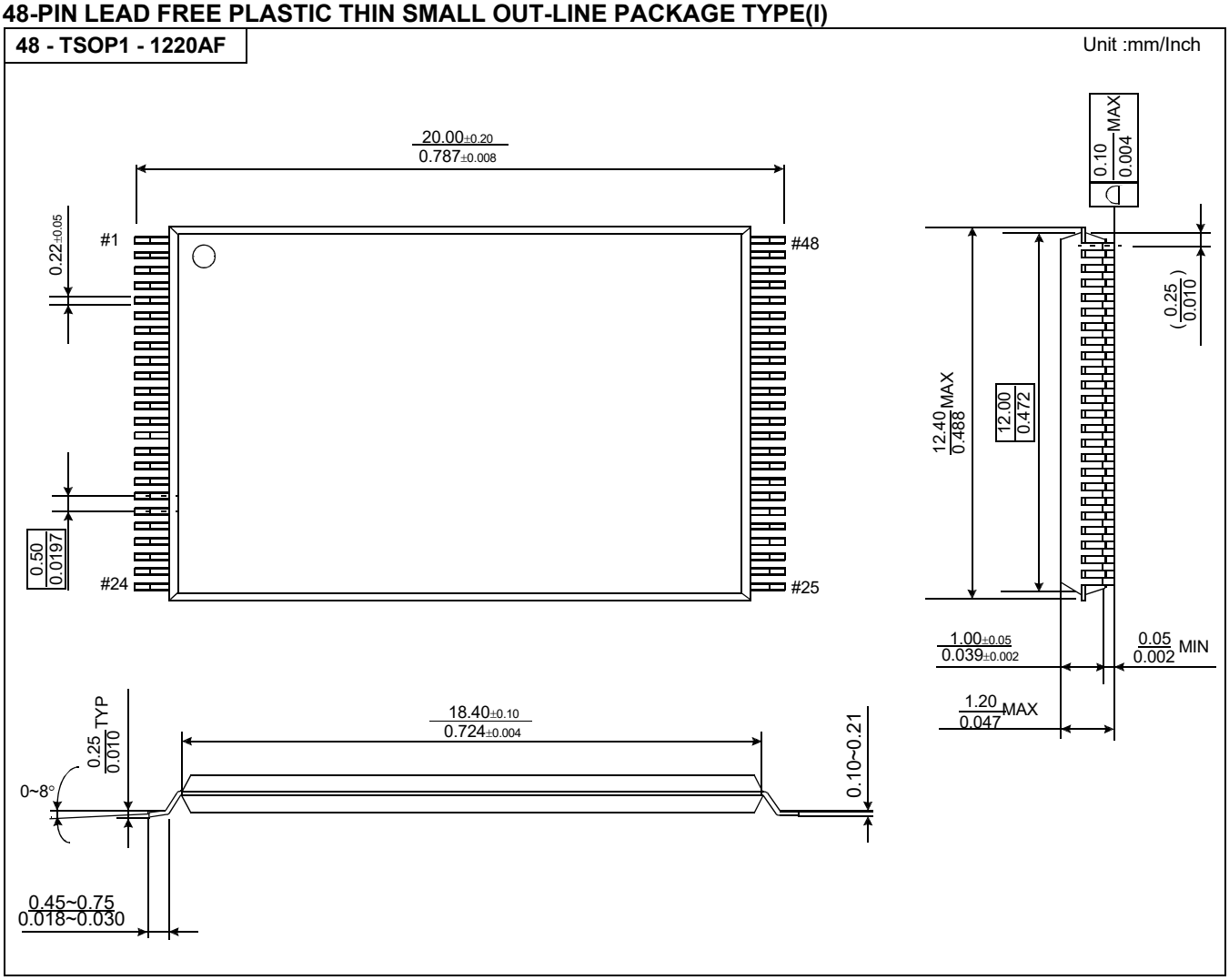
1.4.1 Pin Configuration (48 TSOP1)

S8F2G08(U/S)0A-YxB0



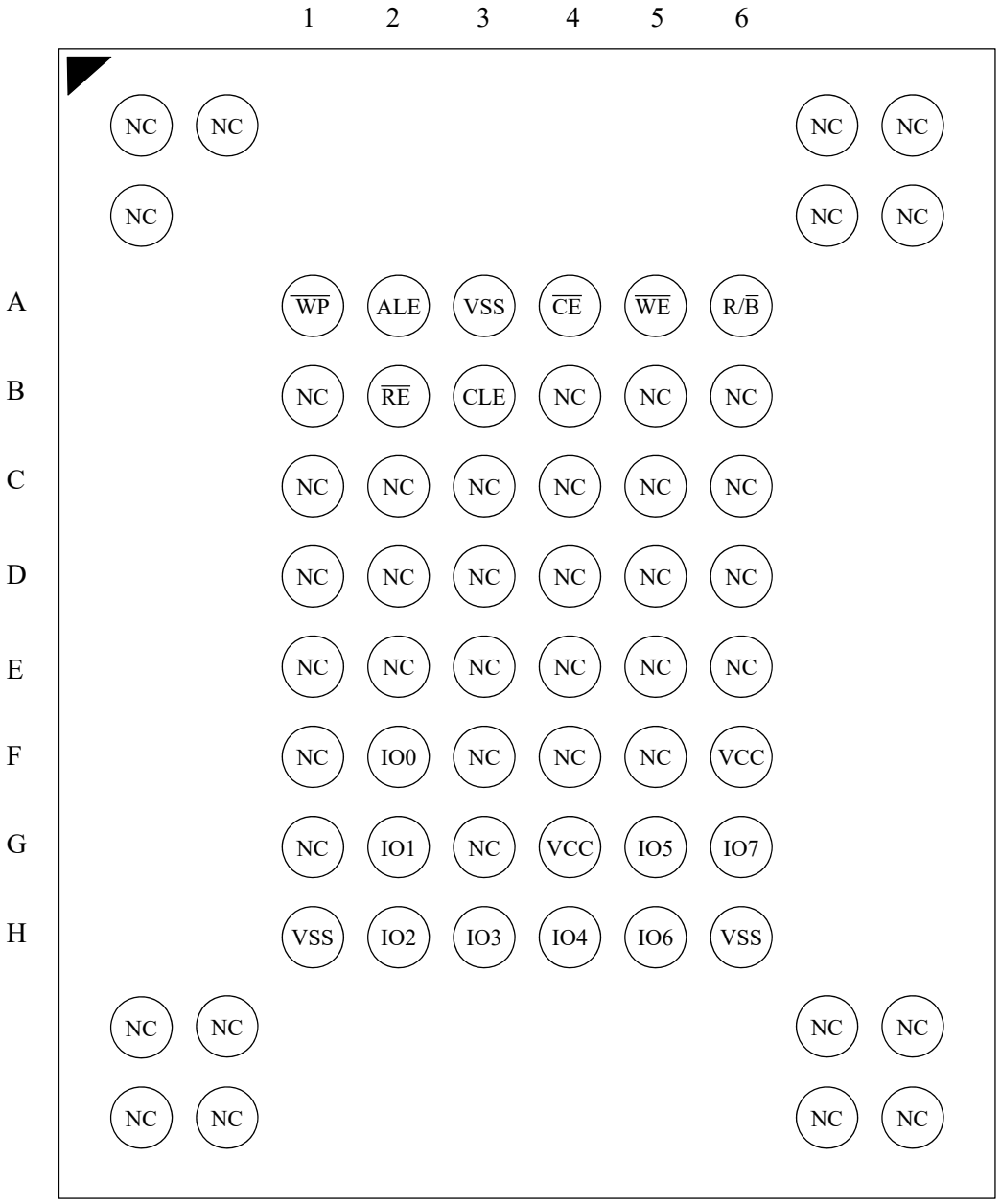
1.4.2 Package Dimensions (48 TSOP1)

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



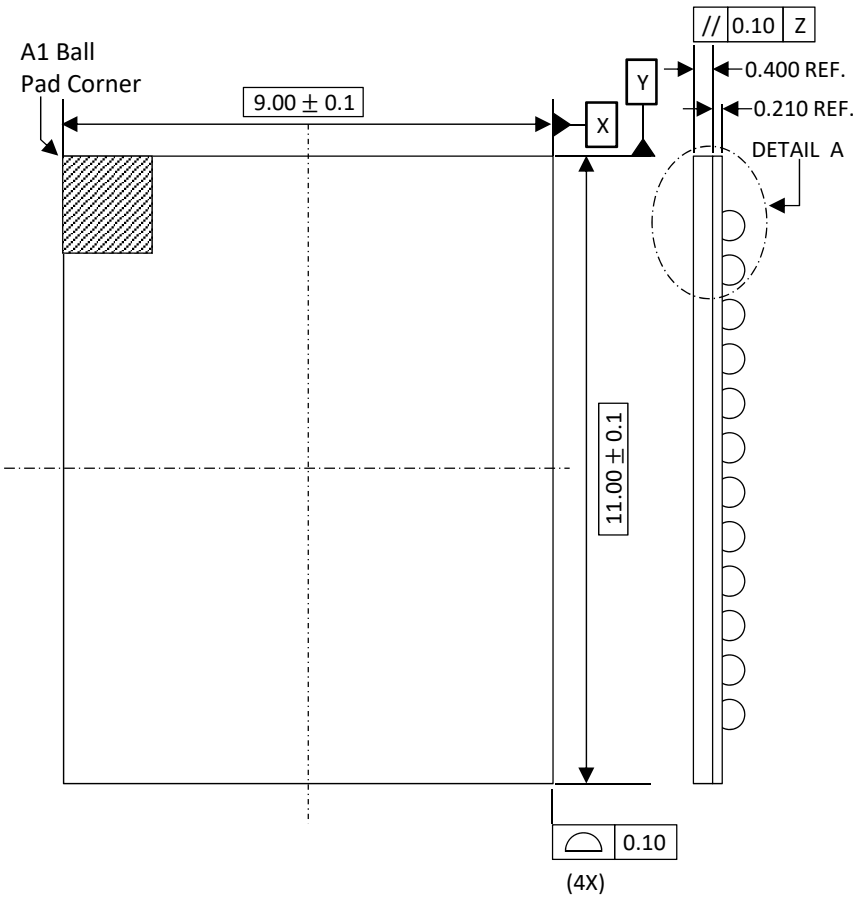
1.4.3 Pin Configuration (63 FBGA 9x11mm)

S8F2G08(U/S)0B-BxB0

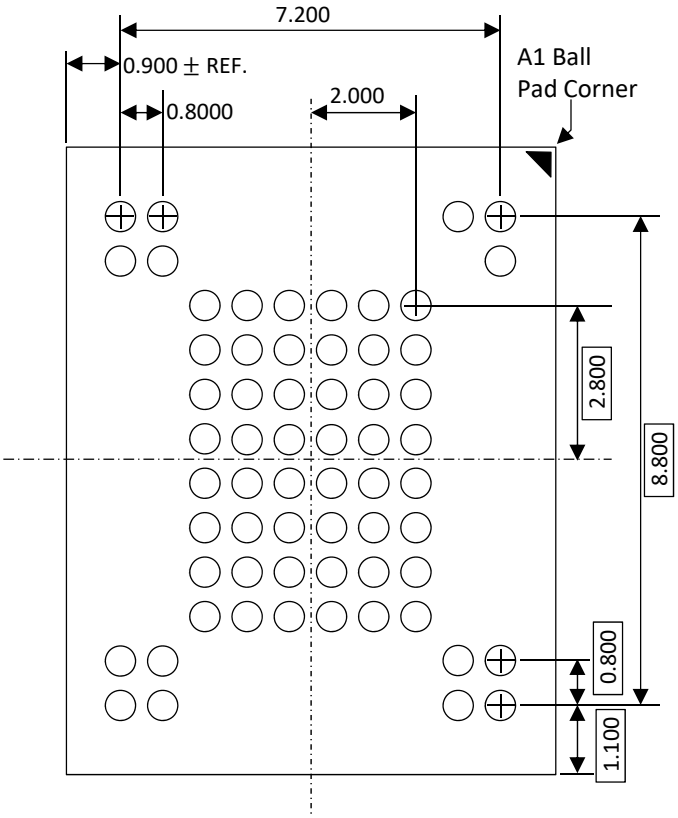


Top View

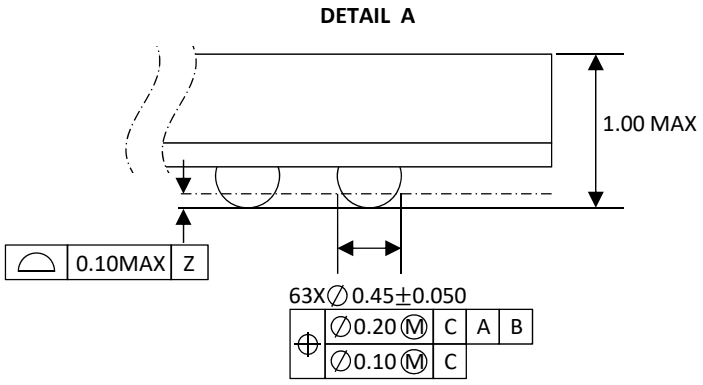
1.4.4 Package Dimensions (63 FBGA 9x11mm)



Top View



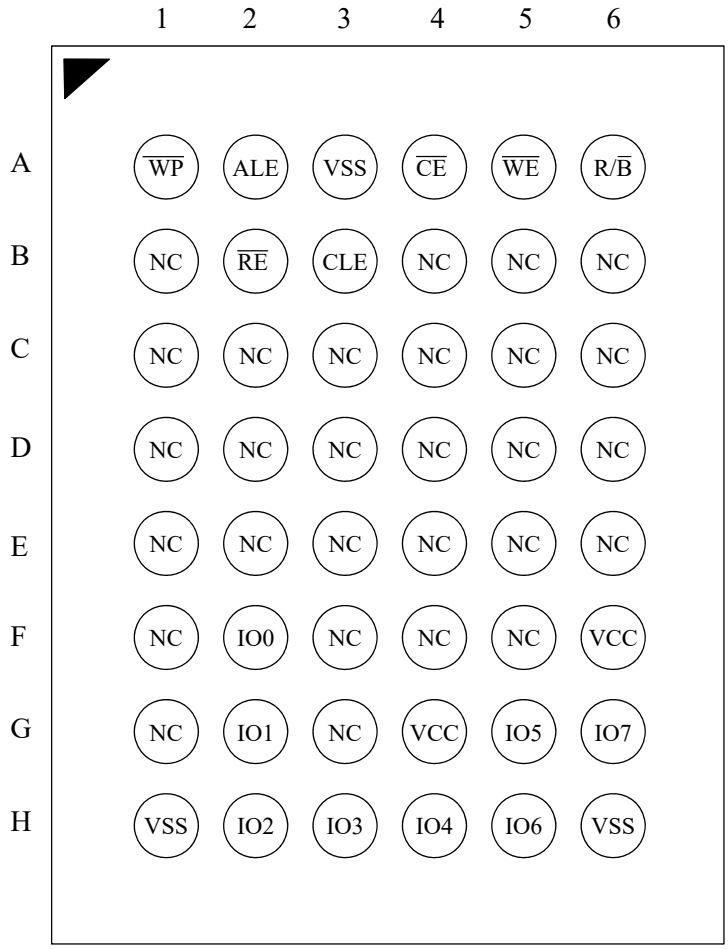
Bottom View



1. All Dimensions are in millimeters.
2. Post Reflow Solder Ball Diameter.
(Pre Reflow Diameter :∅0.40±0.02)

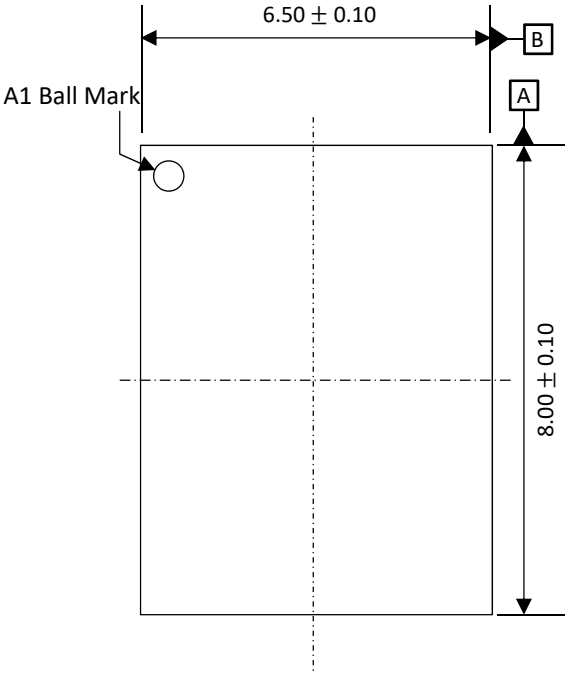
1.4.5 Pin Configuration (48 FBGA 6.5x8mm)

S8F2G08(U/S)0B-XxB0

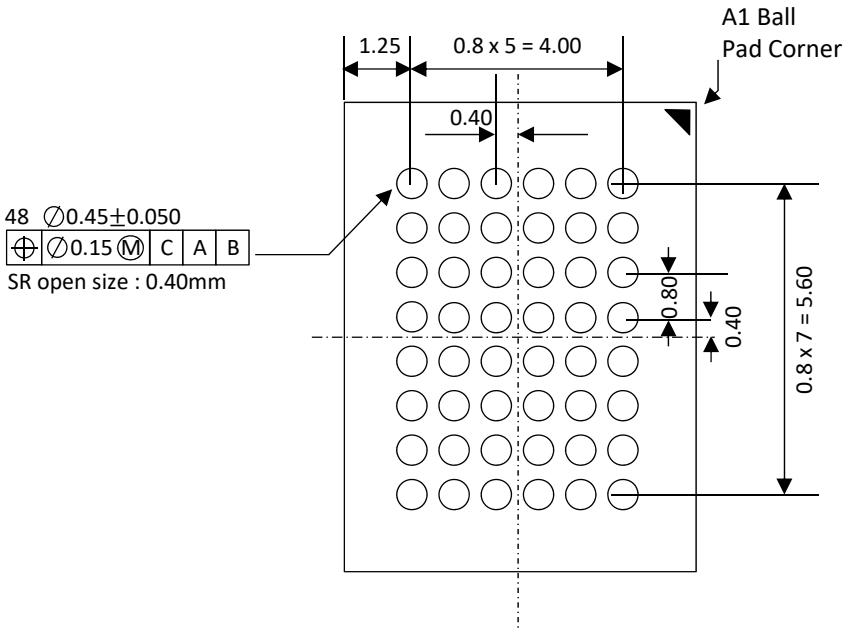


Top View

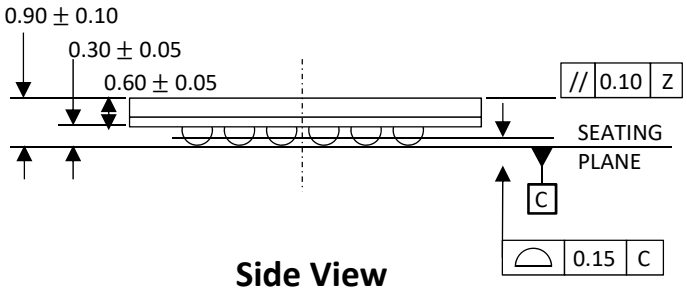
1.4.6 Package Dimensions (48 FBGA 6.5x8mm)



Top View



Bottom View



Side View

1. All Dimensions are in millimeters.
2. Post Reflow Solder Ball Diameter.
(Pre Reflow Diameter :∅0.40±0.02)

1.5 Pin Descriptions

[Table 1] Pin Descriptions

Pin Name	Pin Function
I/O0 ~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the DQ inputs inside the command register on the rising edge of $\overline{WE}$.
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the DQ inputs inside the internal address register on the rising edge of $\overline{WE}$.
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, $\overline{CE}$ high does not deselect the memory. The device goes into Stand-by mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state, and will not enter Standby mode even if the $\overline{CE}$ goes high.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of $\overline{WE}$.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations. Hardware Write Protection is activated when the $\overline{WP}$ pin is low. In this condition modify operation do not start and the content of the memory is not altered. $\overline{WP}$ pin is not latched by Write Enable to ensure the protection even during the power up phases.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output is an Open Drain pin that signals the state of the memory
VCC	**POWER** The V_{CC} supplies the power for all the operations. (Read, Write, and Erase).
VSS	**GROUND**
N/C	**NO CONNECTION / DON'T USE**

NOTE :
A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.6 Block Diagram

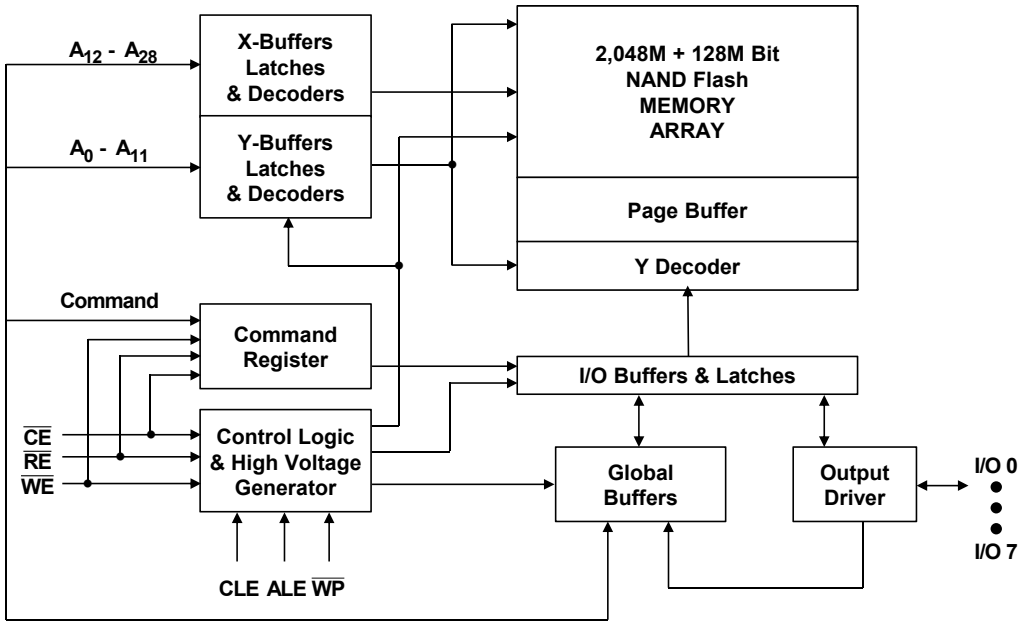


Figure 1. S8F2G08U0A Functional Block Diagram

1.7 Memory Array Organization

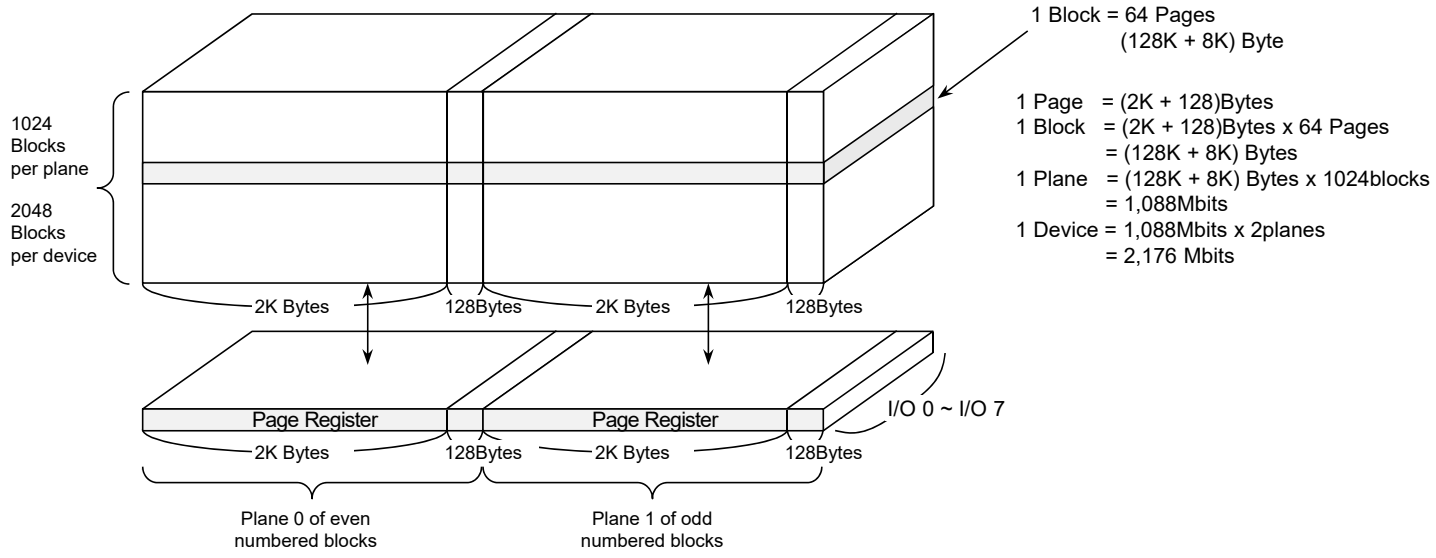


Figure 2. S8F2G08U0A Array Organization

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	
5th Cycle	A28	*L	*L	*L	*L	*L	*L	*L	

NOTE :

1. *L must be set to "Low"
2. A0 – A11 : Column Address in the page
3. A12 – A17 : Page Address in the block
   A18 : Plane Address for multi-plane operation s or Block Address for normal operations
   A19 – A28 : Block Address
4. The device ignores any additional address input cycle than required.

2.0 PRODUCT INTRODUCTION

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$ .Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc. require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 2 defines the specific commands of the S8F2G08U0A.

[Table 2] Command Sets

Function	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable command during busy
Page Read	00h	30h	-	-	
Read for Copy Back	00h	35h	-	-	
Special Read for Copy Back	00h	36h	-	-	
Read ID	90h	-	-	-	
Reset	FFh	-	-	-	O
Page Program(Start) Cache Program(End)	80h	10h	-	-	
Cache Program(Start)	80h	15h	-	-	
Page re-Program	8Bh	10h	-	-	
Copy Back Program	85h	10h	-	-	
(Traditional) Multiplane Program	80h	11h	81h	10h	
ONFI Multiplane Program	80h	11h	80h	10h	
Multiplane Page re-Program	8Bh	11h	8Bh	10h	
(Traditional) Multiplane Cache Program Start/Continue	80h	11h	81h	15h	
ONFI Multiplane Cache Program Start/Continue	80h	11h	80h	15h	
(Traditional) Multiplane Cache Program End	80h	11h	81h	10h	
ONFI Multiplane Cache Program End	80h	11h	80h	10h	
(Traditional) Multiplane Copy Back Program	85h	11h	81h	10h	
ONFI Multiplane Copy Back Program	85h	11h	85h	10h	
Block Erase	60h	D0h	-	-	
(Traditional) Multiplane Block Erase	60h	60h	D0h	-	
ONFI Multiplane Block Erase	60h	D1h	60h	D0h	
Read Status Register	70h	-	-	-	O
Read Status Enhanced	78h	-	-	-	O
Random Data Input	85h	-	-	-	
Random Data Output	05h	E0h	-	-	
Cache Read (Sequential)	31h	-	-	-	
Cache Read Enhanced (Random)	00h	31h	-	-	
Cache Read End	3Fh	-	-	-	
Read Parameter Page	ECh	-	-	-	

Caution :
Any undefined command inputs are prohibited except for above command set of Table 2.

2.1 Valid Block

[Table 3] The Number of Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	2,008	-	2,048	Blocks

NOTE :
1) The 1st block is guaranteed to be a valid block at the time of shipment.
2) Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment.

2.2 Absolute Maximum DC Ratings

[Table 4] Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C
Voltage on any pin relative to V_{SS}		V_{CC}	-0.6 to + 4.6	V
		$V_{I/O}$	-0.6 to + 4.6	
Temperature Under Bias		T_{BIAS}	-50 to +125	°C
Storage Temperature		T_{STG}	-65 to +150	°C

NOTE :
1) Please contact to Netsol and confirm the availability of the product.
2) Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions
3) Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2.3 Recommended Operating Conditions

[Table 5] Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	V_{CC} (S8F2G08U0A)	2.7	3.3	3.6	V
	V_{CC} (S8F2G08S0A)	1.7	1.8	1.95	V
Ground Supply Voltage	V_{SS}	0	0	0	V

NOTE :
Voltage reference to GND.

2.4 DC Operating Characteristics

[Table 6] DC & Operating Characteristics

Parameter		Symbol	Test Conditions	Vcc,typ = 3.3V			Vcc,typ = 1.8V			Unit
				Min	Typ	Max	Min	Typ	Max	
Power on Reset Current		I_{CC0}	FFh command input after power on	-	-	50 per device	-	-	50 per device	mA
Operation Current	Read	I_{CC1}	tRC=tRC(min), $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	15	30	-	10	20	mA
	Program	I_{CC2}	Normal			30			20	
			Cache			40			30	
	Erase	I_{CC3}	-		15	30		10	20	
Stand-by Current (TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	-	-	1	
Stand-by Current (CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2,$\overline{WP}$=0V/V_{CC}	-	10	50	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC}(max)	-	-	±10	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC}(max)	-	-	±10	-	-	±10	
Input High Voltage		V_{IH}[1)]	-	0.8xV_{CC}	-	V_{CC}+0.3	0.8xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}[1)]	-	-0.3	-	0.2xV_{CC}	-0.3	-	0.2xV_{CC}	
Output High Voltage Level		V_{OH}	I_{OH}= - 400µA, ($V_{CC.typ}$=3.3V) I_{OH}= - 100µA, ($V_{CC.typ}$=1.8V)	2.4	-	-	V_{CC}-0.1	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}= 2.1mA, ($V_{CC.typ}$=3.3V) I_{OL}= 100µA, ($V_{CC.typ}$=1.8V)	-	-	0.4	-	-	0.1	
Output Low Current (R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}= 0.4V, ($V_{CC.typ}$=3.3V) V_{OL}= 0.1V, ($V_{CC.typ}$=1.8V)	8	10	-	3	4	-	mA

2.5 Input / Output Capacitance (T_A=25°C, f=1.0Mhz)

[Table 7] Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE :
Capacitance is sampled and not 100% tested.

2.6 AC Test Condition

[Table 8] AC Test Condition

Parameter	S8F2G08U0A / S8F2G08S0A
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC}/2
Output Load	1 TTL GATE and C_L=50pF

NOTE :
1) These parameters are verified device characterization and are not 100% tested.

2.7 Read / Program / Erase Characteristics

[Table 9] NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	t_R	-	-	30	µs
Program Time	t_{PROG}	-	300	700	µs
Cache Read busy time	t_{CBSYR}	-	5	t_R	µs
Cache Program short busy time	t_{CBSYW}	-	5	t_{PROG}	µs
Cache Program busy time(ONFI)	t_{PCBSY}	-	5	t_{PROG}	µs
Multi-plane Erase busy time	t_{IEBSY}		0.5	1	µs
Multi-plane Program busy time(traditional)	t_{DBSY}	-	0.5	1	µs
Multi-plane Program busy time(ONFI)	t_{IPBSY}		0.5	1	µs
Number of Partial Program Cycles	Nop	-	-	4	cycle
Block Erase Time	t_{BERS}	-	3.5	10	ms

NOTE :
1) Typical value is measured at V_{CC}=3.3V, T_A=25°C(3.3V Device) or V_{CC}=1.8V, T_A=25°C(1.8V Device). Not 100% tested.

2.8 AC Timing Parameters Table

[Table 10] AC Timing Characteristics

Parameter	Symbol	Vcc,typ = 3.3V		Vcc,typ = 1.8V		Unit
		Min	Max	Min	Max	
CLE Setup Time	t_{CLS}	12	-	25	-	ns
CLE Hold Time	t_{CLH}	5	-	10	-	ns
$\overline{CE}$ Setup Time	t_{CS}	20	-	35	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	-	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	12	-	25	-	ns
ALE Setup Time	t_{ALS}	12	-	25	-	ns
ALE Hold Time	t_{ALH}	5	-	10	-	ns
Data Setup Time	t_{DS}	12	-	20	-	ns
Data Hold Time	t_{DH}	5	-	10	-	ns
Write Cycle Time	t_{WC}	25	-	45	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	10	-	15	-	ns
Address to Data Loading Time	t_{ADL}	70	-	100	-	ns
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	12	-	25	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	-	100	ns
Read Cycle Time	t_{RC}	25	-	45	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	20	-	30	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	100	-	100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	30	-	50	ns
$\overline{CE}$ High to ALE or CLE Don't Care	t_{CSD}	10	-	10	-	ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15	-	15	-	ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5	-	-	-	ns
$\overline{CE}$ High to Output Hold	t_{COH}	15	-	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	10	-	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	0	-	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	-	100	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	60	-	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	t_{CR}	10	-	10	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	5/10/500[1)]	-	5/10/500[1)]	µs
Write Protection Time	t_{WW}	100	-	100	-	ns

NOTE :
1) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5µs.

3.0 NAND FLASH TECHNICAL NOTES

3.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Netsol. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

3.2 Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Netsol makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the first byte of spare area on the 1st or 2nd page. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3).

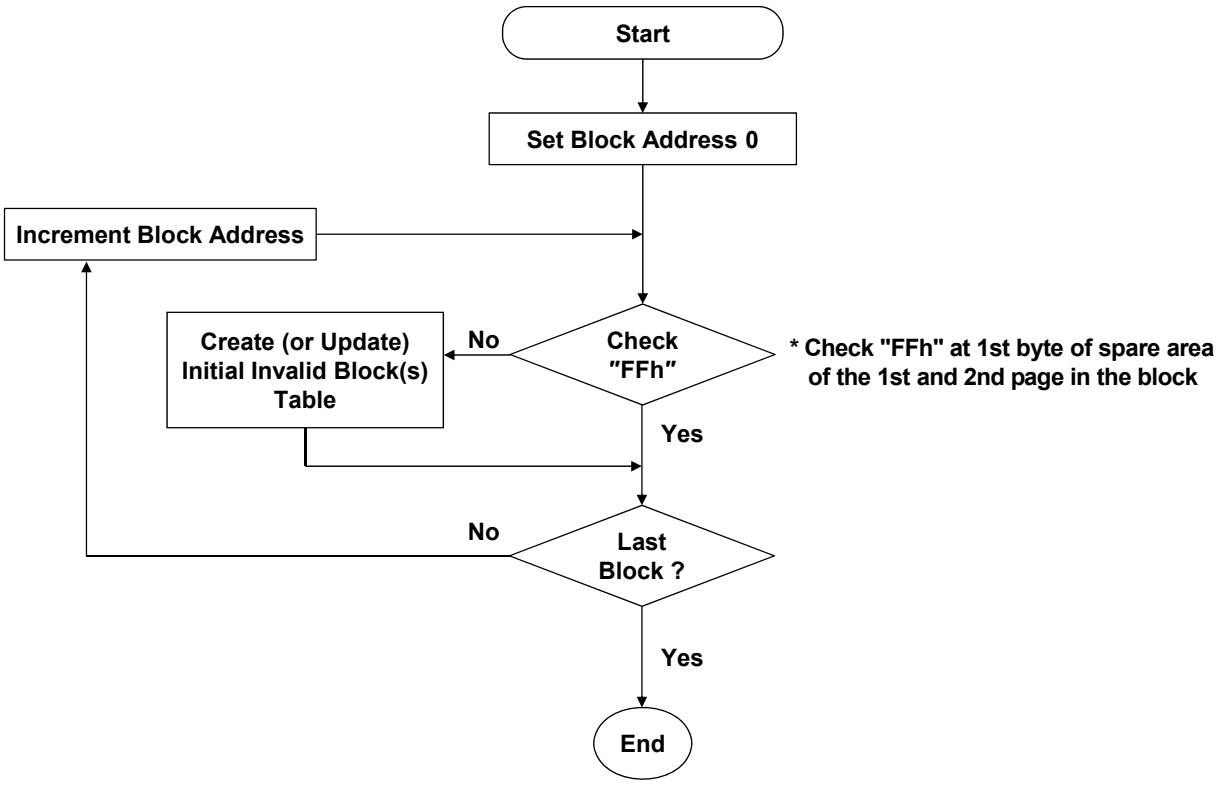


Figure 3. Flow Chart to Create Initial Invalid Block Table

NOTE :
1) Do not try to erase the detected bad blocks, because the bad bock information will be lost.
2) Do not perform program and erase operation in invalid block, it is impossible to guarantee the Input data and to ensure that the function is normal.

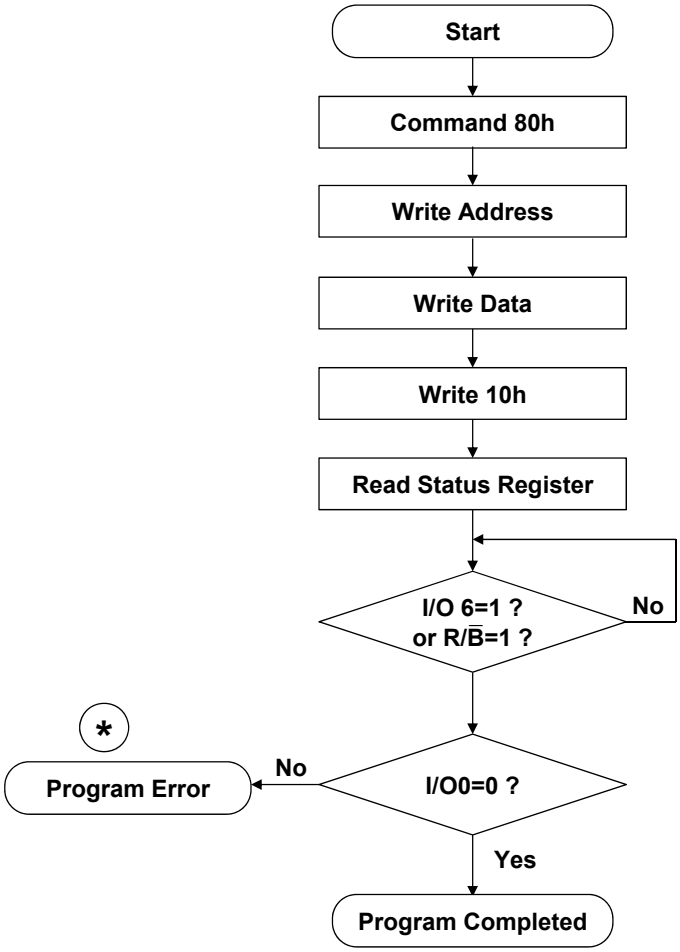
3.3 Error in Write or Read Operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.

[Table 11] Failure Cases

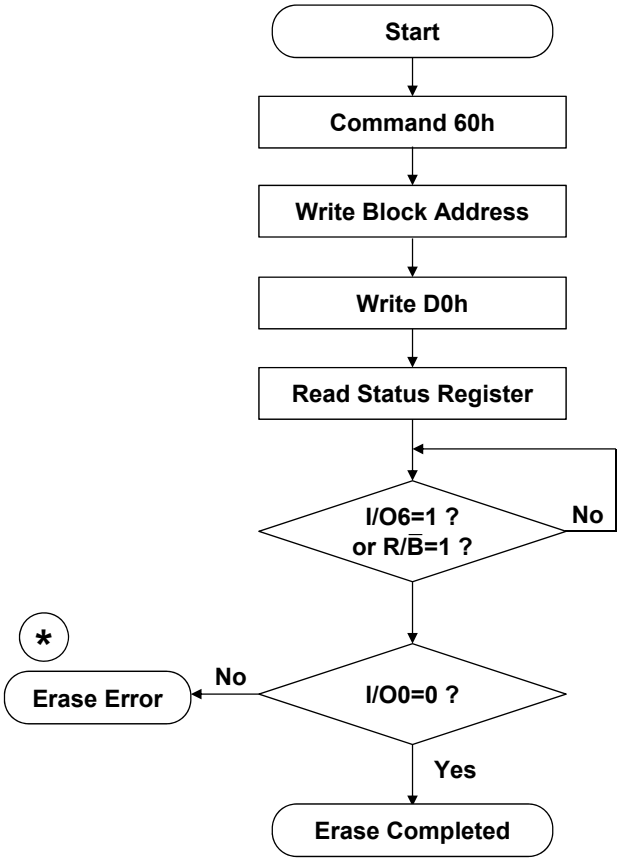
Failure Mode		Detection and Countermeasure Sequence
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

Program Flow Chart



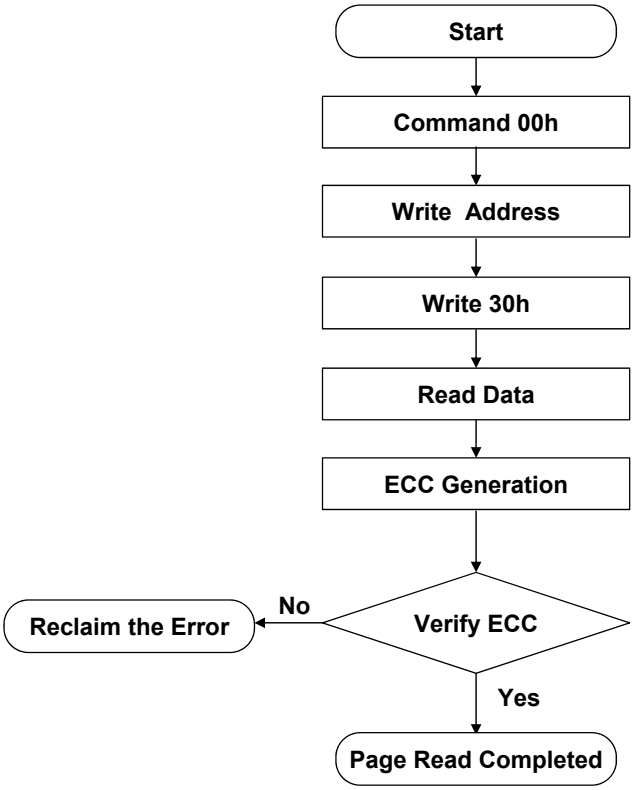
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

Erase Flow Chart

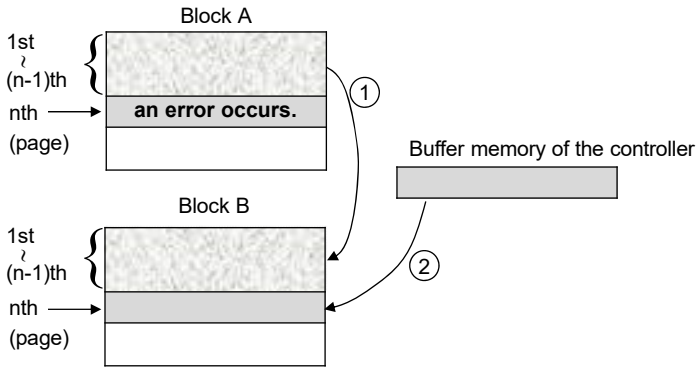


(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Read Flow Chart



Block Replacement



1. When an error happens in the nth page of the Block 'A' during erase or program operation.
2. Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
3. Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
4. Bad block table should be updated to prevent from erasing or programming Block A.

Figure 4. Flow Chart

4.0 DEVICE OPERATION

4.1 Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.8 V (3.3 V Device) or 1.1 V (1.8 V Device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power down. A recovery time of minimum 100us is required before internal circuit gets ready for any command sequences. The two-step command sequence for program/erase provides additional software protection.

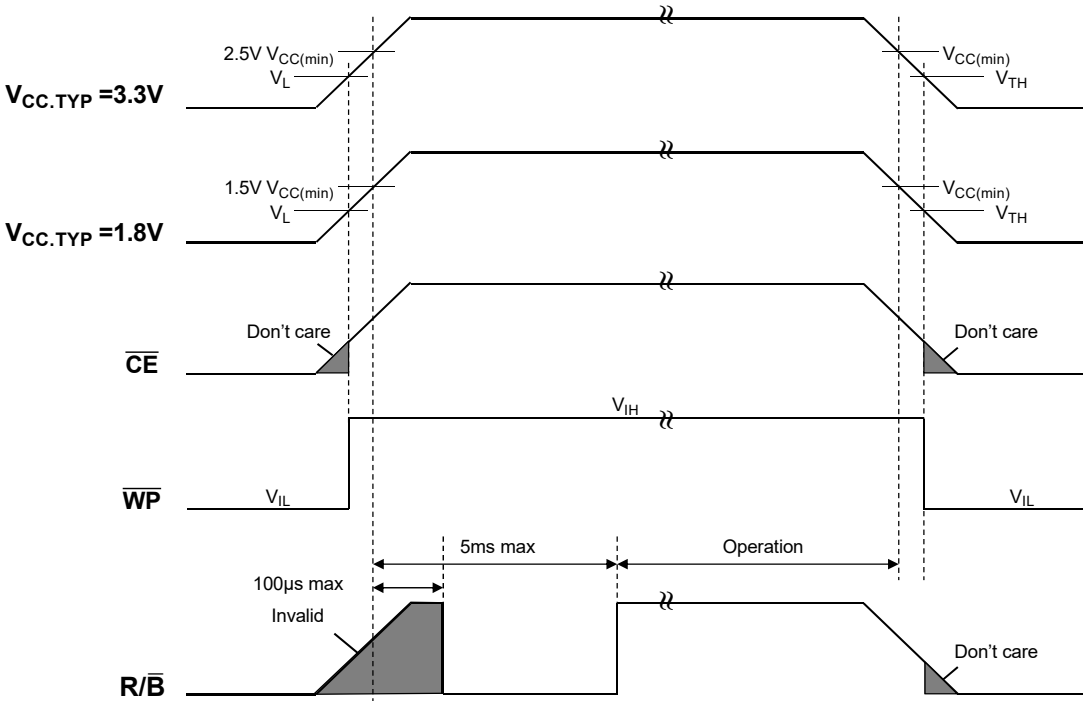


Figure 5. AC Waveforms for Power Transition

4.2 Mode Selection

[Table 12] Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(5 cycles)
H	L	L	↑	H	H	Write Mode	Command Input
L	H[1)]	L	↑	H	H		Address Input(5 cycles)
L	L	L	↑	H	H	Data Input	
L	L[1)]	L	H	↓	X	Data Output (on going)	
X	X	L	H	H	X	Data Output (suspended)	
L	L	L	H[3)]	H[3)]	X	During Read(Busy)	
X	X[1)]	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}[2)]	Stand-by	

NOTE :
1) X can be V_{IL} or V_{IH}. H = Logic level HIGH. L = Logic level LOW.
2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
3) $\overline{WE}$ and $\overline{RE}$ during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset, Read Status, and Multiplane Read Status can be input to the device.

4.3 BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. Typically glitches less than 5ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations. .

Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See “2.8. AC Timing Parameters Table" for details of the timings requirements.

Address Input

Address Input bus operation allows the insertion of the memory address. 5 clock cycles are needed to input the addresses. (refer to “1.7 Memory Array Organization”). Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation(write/erase) the Write Protect pin must be high. See “2.8. AC Timing Parameters Table” for details of the timings requirements.

Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Dat a are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latche d on the rising edge of Write Enable. See “2.8. AC Timing Parameters Table" for details of the timings requirements.

Data output

Data Output bus operation allows to read data from the memory array and to check the status register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See “2.8. AC Timing Parameters Table" for details of the timings requirements.

Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

Standby

In Standby the device is deselected, outputs are disabled and Power Consumption is reduced.

4.4 Page Read Operation

Page read is initiated by writing 00h-30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2,176 bytes of data within the selected page are transferred to the data registers in less than 30μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns (3V version) and 45ns (1.8V version) cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

After power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.

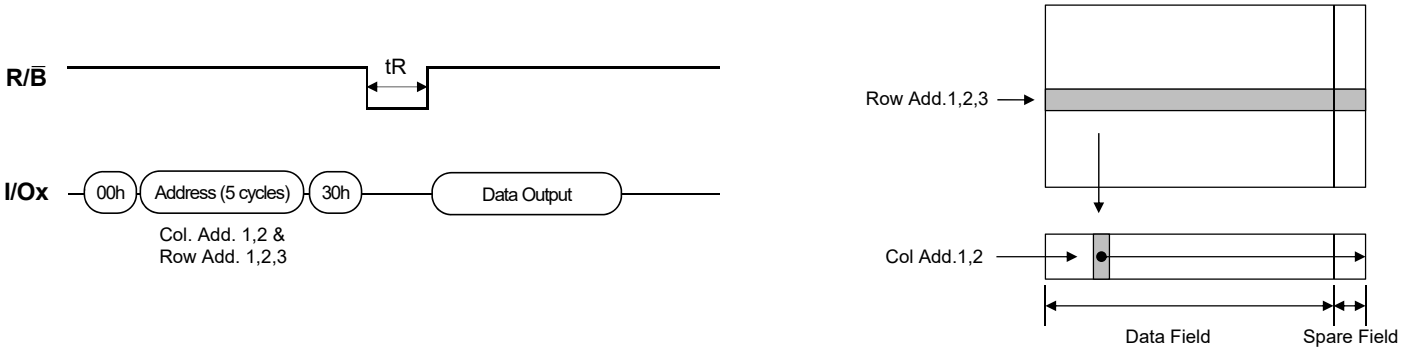


Figure 6. Page Read Sequence

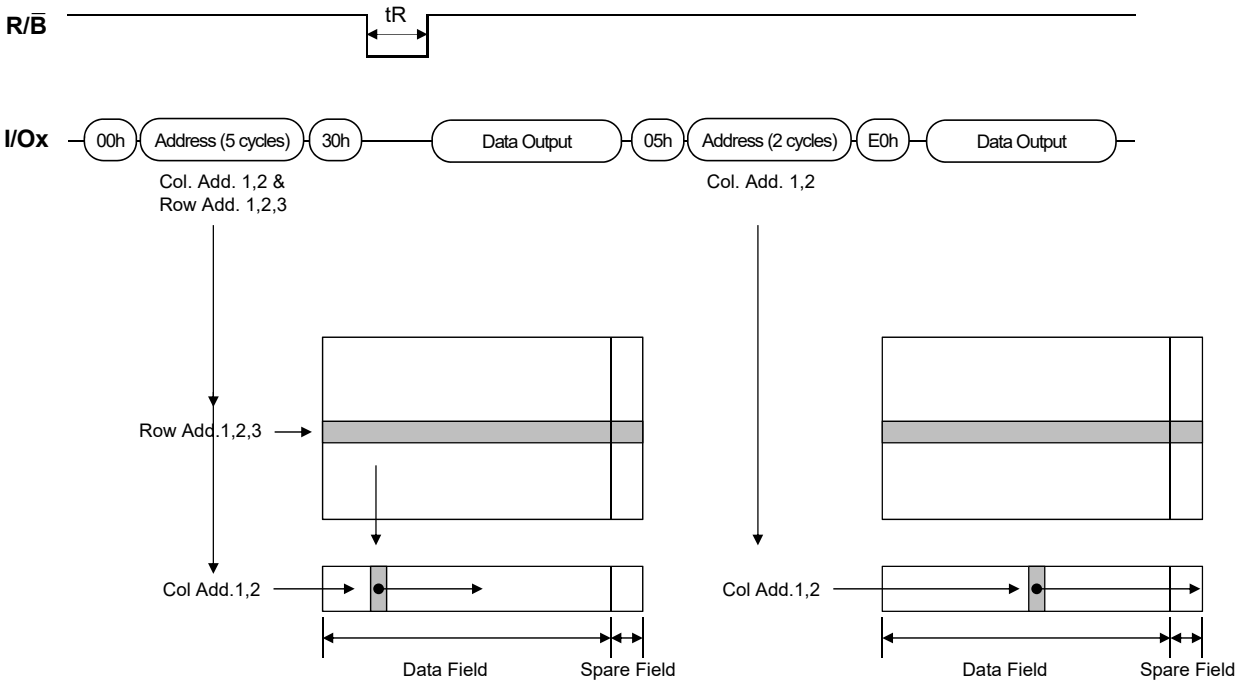


Figure 7. Page Read with Random Data Output Sequence

4.5 Cache Read Operation (available only within a block)

The Cache Read function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, as defined in 4.4, shall be issued prior to the initial sequential or random Cache Read command in a Cache Read sequence. A Cache Read Sequential or Cache Read Random command shall be issued prior to a Cache Read End (3Fh) command being issued.

The Cache Read function may be issued after the Read function is complete (the status bit SR[I/O 6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Cache Read function is issued, SR[I/O 6] is cleared to zero (busy). After the operation is begun SR[I/O 6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache Read function. Issuing an additional Cache Read function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[I/O 6] is set to one (ready). When the 31h and 3Fh commands are issued, SR[I/O 6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a sequential Cache Read (31h) command after the last page of the device is read. SR[I/O 6] conveys whether the next selected page can be read from the page register. During Cache Read operation the only acceptable commands are Read Status, Random Data Output and Reset.

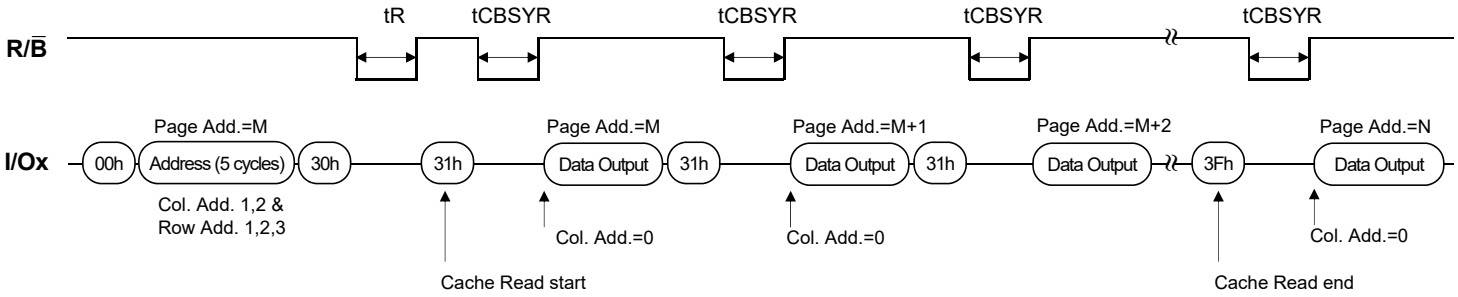


Figure 8. Sequential Cache Read Sequence

4.6 Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased. A page program cycle consists of a serial data loading period in which up to 2,176 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command(10h) initiates the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks.

Once the program process starts, the Read Status Register command (70h or 78h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the status bit SR[I/O 6]. Only the Read Status command or Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit SR[I/O 0] may be checked(Figure 9 and 10). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

The device is programmed basically by page, but it also allows multiple partial page programming of a word or consecutive bytes up to 2176 in a single page program cycle. The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. For example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/32byte).

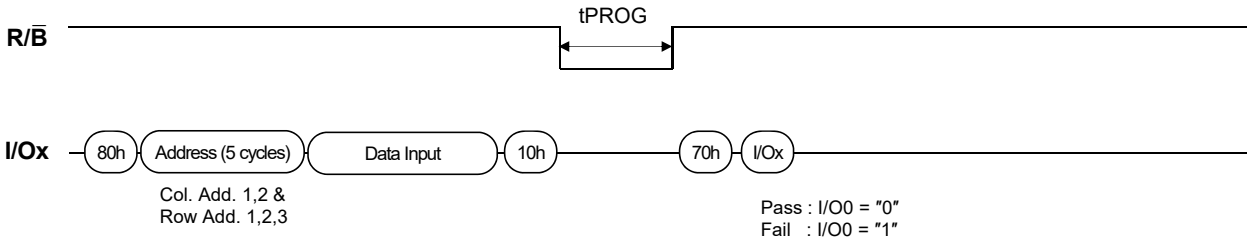


Figure 9. Page Program Sequence

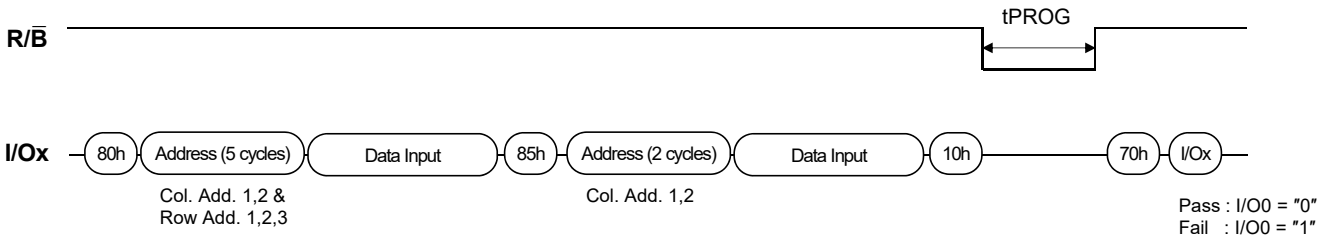
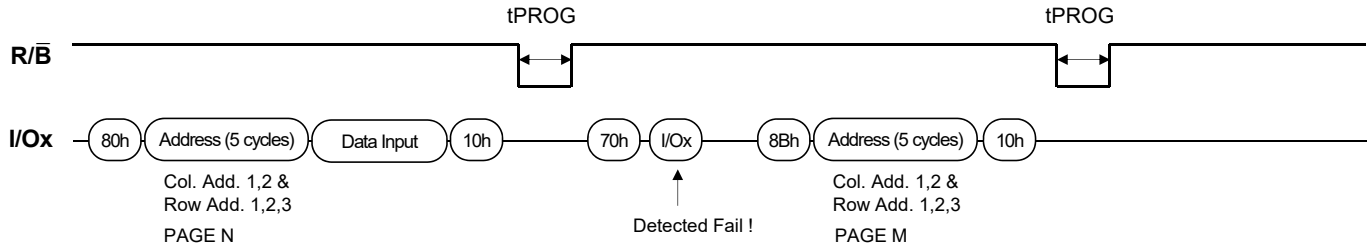


Figure 10. Program Operation with Random Data Input Sequence

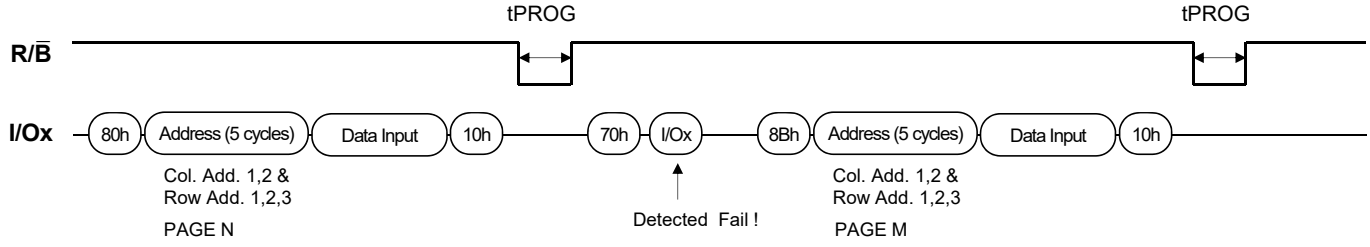
4.7 Page Re-program Operation

This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle. On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm "10h". During page re-program, address limitation applies as described in Figure 13,14 note 1 and 2 for copy-back function. Similarly, the multi-plane page re-program allows to re-program two pages in parallel, one per each plane. The first page must be in the first plane while the second page must be in the second plane; the multi-plane page re-program operation is performed after a previously failed multi-plane page program operation. As for single page re-program case, multi-plane page re-program can be issued without any data manipulation. During multiplane page re-program, address limitation applies as described in Figure 15 notes 1 and 2 for multiplane copy-back function.

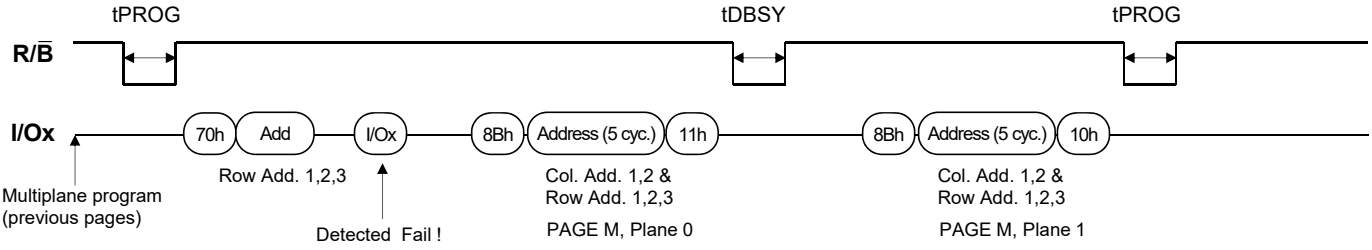
*** Page Re-program**



*** Page Re-program with data manipulation**



*** Multiplane Page Re-program**



*** Multiplane Page Re-program with data manipulation**

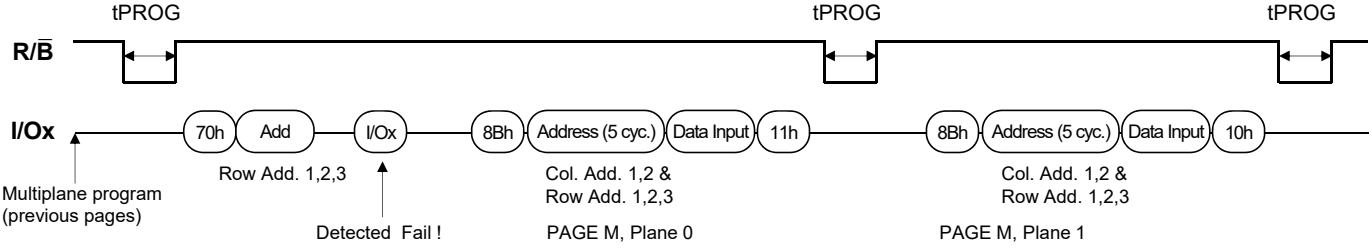


Figure 11. Page Re-program

4.8 Multiplane Program Operation

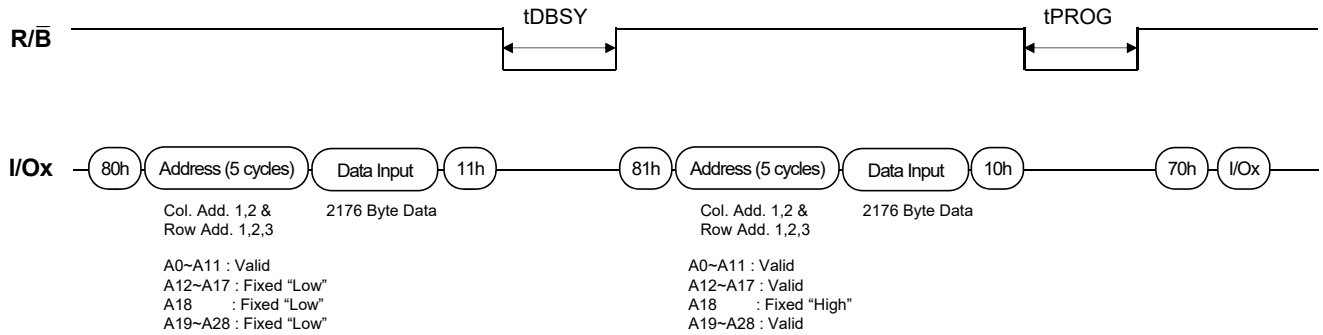
The device supports multiple plane program: it is possible to program 2 pages in parallel, one per each plane. A multiple plane program cycle consists of a double serial data loading period in which up to 4352 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. Address for this page must be in the 1st plane (A_{18}=0). The device supports random data input exactly same as in the case of page program operation. The Dummy Page program Confirm command (11h) stops 1st page data input and devices become busy for a short time (tDBSY). Once it has become ready again, either the "81h" or "80h" command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be in the 2nd plane (A_{18}=1). Program Confirm command (10h) makes parallel programming of both pages to start.

User can check operation status by monitoring R/$\overline{B}$ pin or reading status register commands (70h or 78h), as if it were a normal page program; read status register command is also available during Dummy Busy time (tDBSY).

In case of fail in any 1st and 2nd page program fail bit of status register will be set; however, in order to know which page failed, ONFI 1.0 “read status enhanced” command must be issued. Refer to section 4.14 for further information.

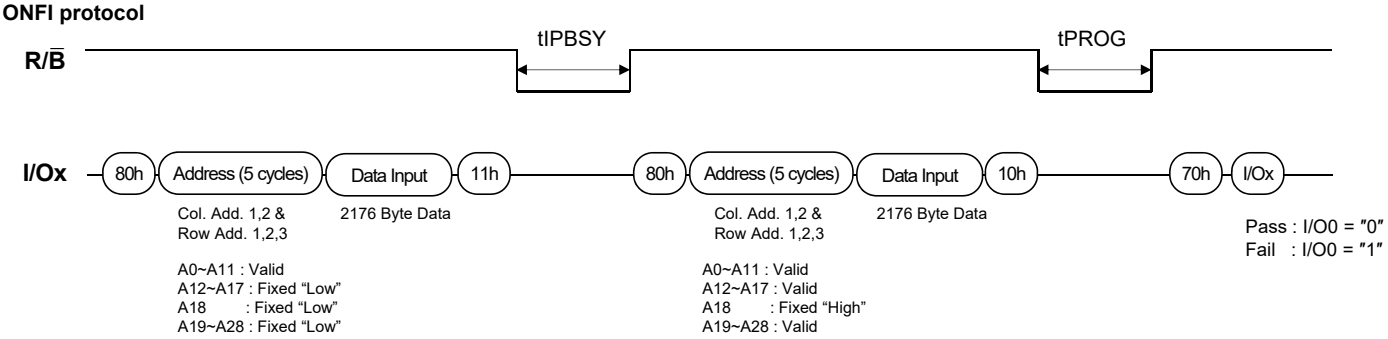
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/32byte).

*** Traditional protocol**



NOTE :
Any command between 11h and 81h is prohibited except 70h,78h,and FFh

*** ONFI protocol**



NOTE :
Any command between 11h and 80h is prohibited except 70h,78h,and FFh

Figure 12. Multiplane Program Sequence

4.9 Copy-Back Program Operation

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2176 bytes(x8 Device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling $\overline{RE}$, or copy-back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 13, 14. When there is a program-failure at copy-back operation, error is reported by pass/fail status. But, if copy-back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, four bit error correction is recommended for the use of copy-back operation. Figure 20 shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, $\overline{WP}$ value is don't care during Read for copy-back, while it must be set to Vcc When performing the program. During copy-back operation, address limitation applies as described in Figure 13, 14 notes 1 and 2.

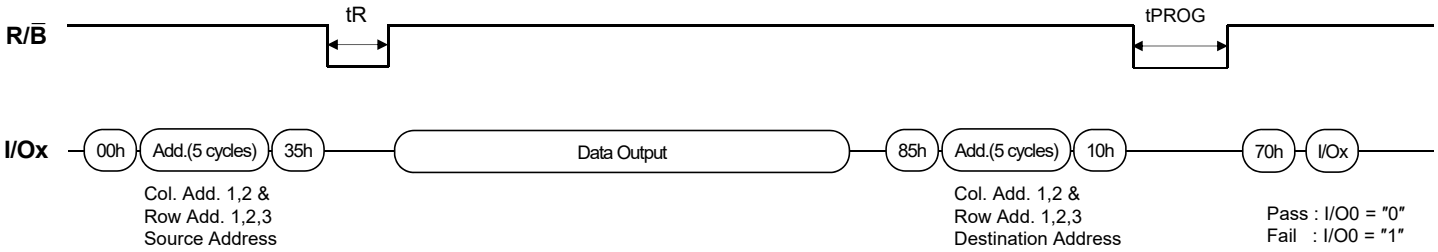


Figure 13. Copy-Back Read with Optional Data Readout

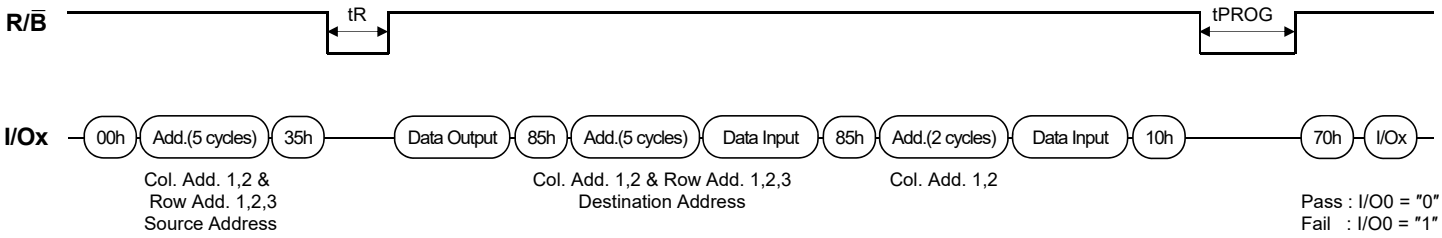


Figure 14. Copy-Back Program with Random Data Input Sequence

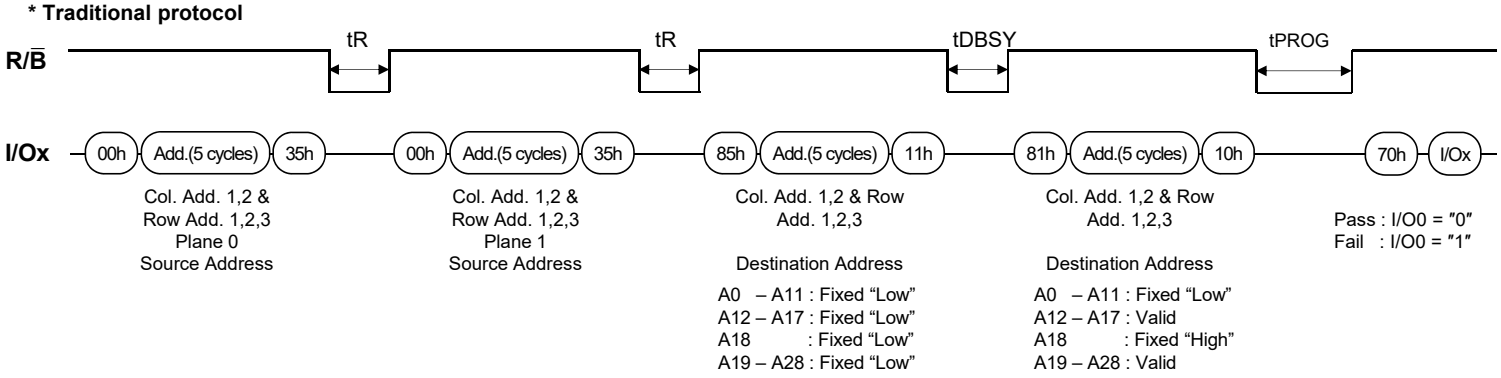
NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
2) On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page (target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.

4.10 Multiplane Copy-Back Program Operation

As for page program, device supports multiplane copy back program with exactly same sequence and limitations. Multiplane copy back program must be preceded by 2 single page read for copy back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane). Multiplane copy back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane.

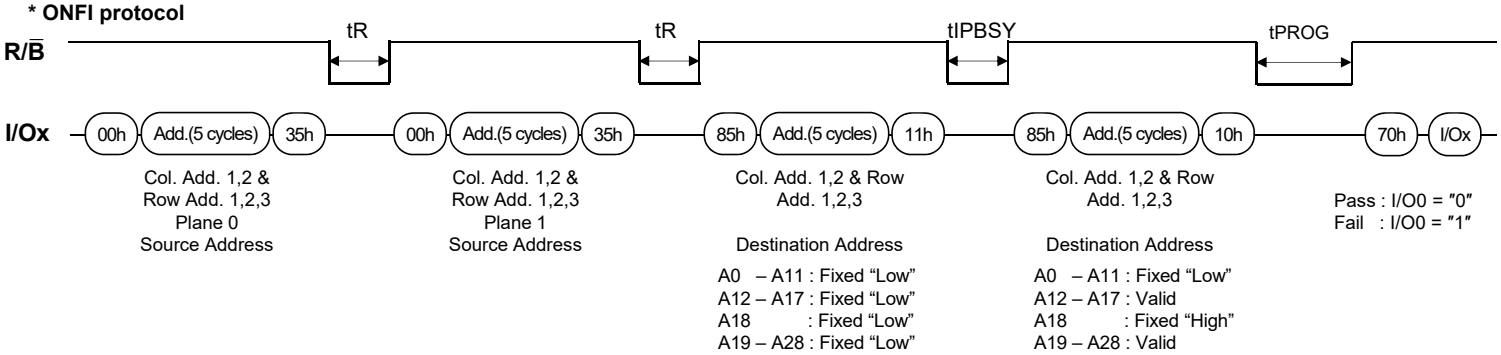
Also in this case, two different sequences are allowed : the traditional one (85h, first plane address 11h, 81h, second plane address, 10h) and ONFI 1.0 sequence (85h, first plane address 11h, 85h, second plane address, 10h). During multi-plane copy-back operation, address limitation applies as described in Figure 15 notes 1 and 2.

*** Traditional protocol**



NOTE : Any command between 11h and 81h is prohibited except 70h and 78h and FFh.

*** ONFI protocol**



NOTE : Any command between 11h and 85h is prohibited except 70h and 78h and FFh.

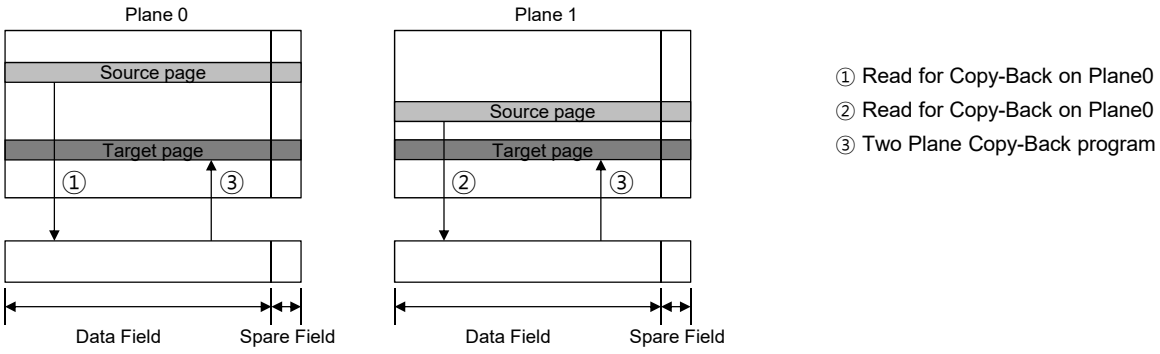


Figure 15. Multiplane Copy-Back Program

NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
2) On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page (target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.

4.11 Special read for Copy-back Operation

The device feature the "special read for copy-back".

If copy-back read (described in sections 4.9 and 4.10) is triggered with confirm command "36h" instead "35h", copy-back read from target page(s) will be executed with an increased internal (Vpass) voltage. This special feature is used in order to try to recover incorrigible ECC read errors due to over program or read disturb: it shall be used ONLY if ECC read errors have occurred in the source page using "standard read" or "standard read for copy-back" sequences.. Excluding the copy-back read confirm command, all other features described in sections 4.9 and 4.10 for standard copy-back remain valid (including the figures referred to in those sections).

4.12 Cache Program Operation (available only within a block)

Cache Program is an extension of the standard page program which is executed with two 2176 bytes registers, the data and the cache register. In short, the cache program allows data insertion for one page while program of another page is under execution. Cache program is available only within a block. After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register. Once the cache write command(15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).

The busy time following the first sequence 80h-15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model.

In case of any subsequent sequence 80h-15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (tCBSYW).

Read Status commands (70h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. More in detail:

a) The status bit SR[I/O 6] indicates when the cache register is ready to accept new data.
b) The status bit SR[I/O 5] indicates when the cell programming of the current data register is complete
c) The status bit SR[I/O 1] returns the pass/fail status for the previous page when the status bit SR[I/O 6] equals a “1” (ready state).
d) The status bit SR[I/O 0] returns the pass/fail status for the current page when the status bit SR[I/O 5] equals a “1” (ready state).
SR[I/O 1] may be read together with SR[I/O 0].

If the system monitors the progress of the operation only with R/$\overline{B}$, the last page of the target program sequence must be programmed with Page Program Confirm command(10h). If the Cache Program command(15h) is used instead, the status bit SR[I/O 5] must be polled to find out if the last programming is finished before starting any other operation.

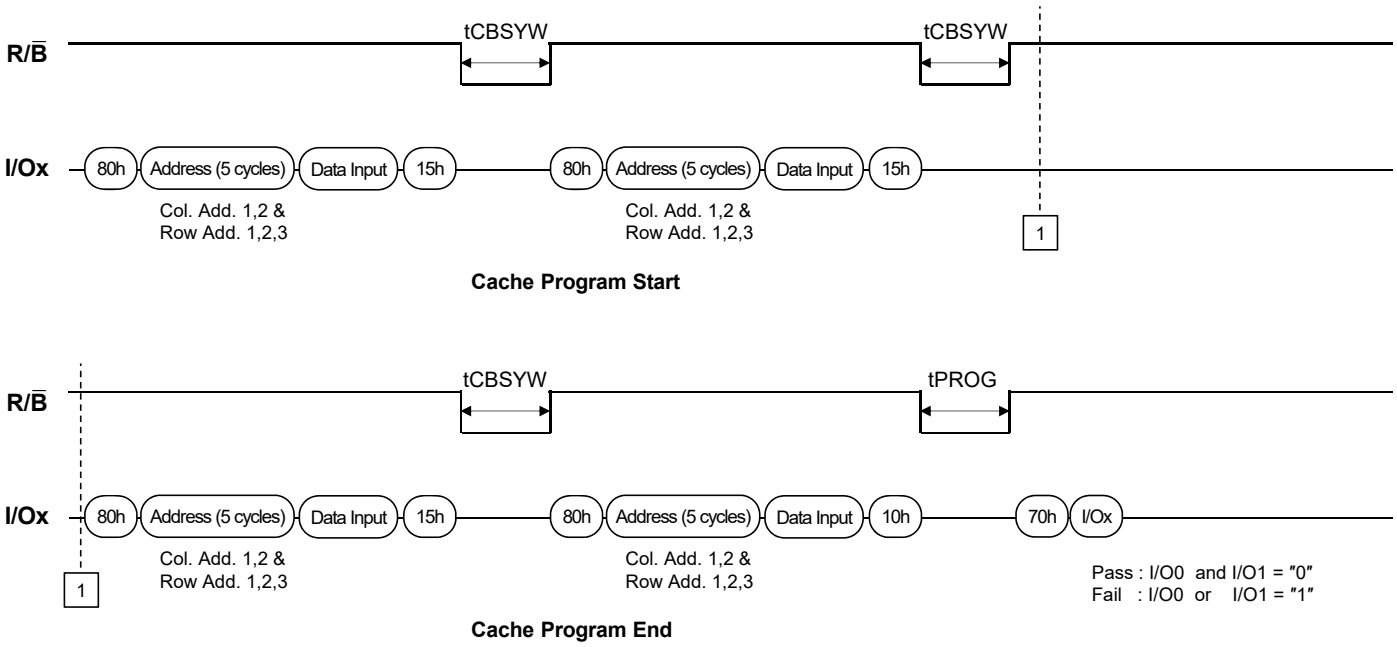


Figure 16. Cache Program Operation

4.13 Multiplane Cache Program Operation

The device supports multi-plane cache program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache. The device supports both the traditional and ONFI 1.0 command sets.

The command sequence can be summarized as follows :

a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A_{18}=0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.

b) The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

c) Once device returns to ready again, 81h (or 80h) command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A_{18}=1). The data of 2nd page other than those to be programmed do not need to be loaded.

d) Once Cache Program confirm command(15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence.

The sequence 80h–11h–81h(or 80h) –15h can be iterated, and any new time the device will be busy for a for the tCBSYW time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed. The sequence to end multi-plane cache program is 80h–11h–81h(or 80h)–10h. Multiplane Cache program is available only within two paired blocks belonging to the two planes.

User can check operation status by R/$\overline{B}$ pin or read status register commands (70h or 78h). Status register read(70h) will provide a “global” information about the operation in the two planes.

More in detail:

a) The status bit SR[I/O 6] indicates when both cache registers are ready to accept new data.

b) The status bit SR[I/O 5] indicates when the cell programming of the current data registers is complete

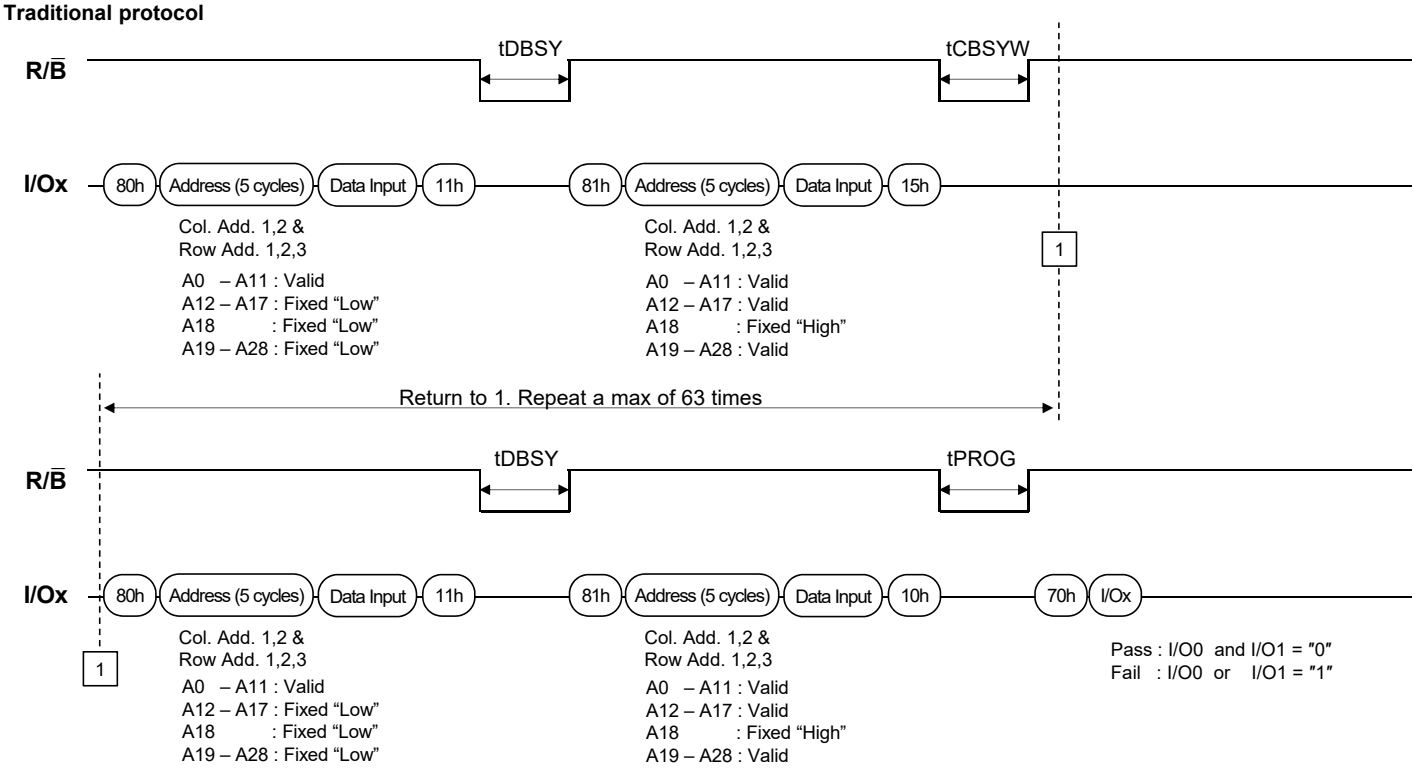
c) The status bit SR[I/O 1] identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon the status bit SR[I/O 6] changing to "1".

d) The status bit SR[I/O 0] identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon the status bit SR[I/O 5] changing to "1".

If the system monitors the progress of the operation only with R/$\overline{B}$, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit SR[I/O 5] must be polled to find out if the last programming is finished before starting any other operation.

4.13 Multiplane Cache Program Operation

*** Traditional protocol**



*** ONFI protocol**

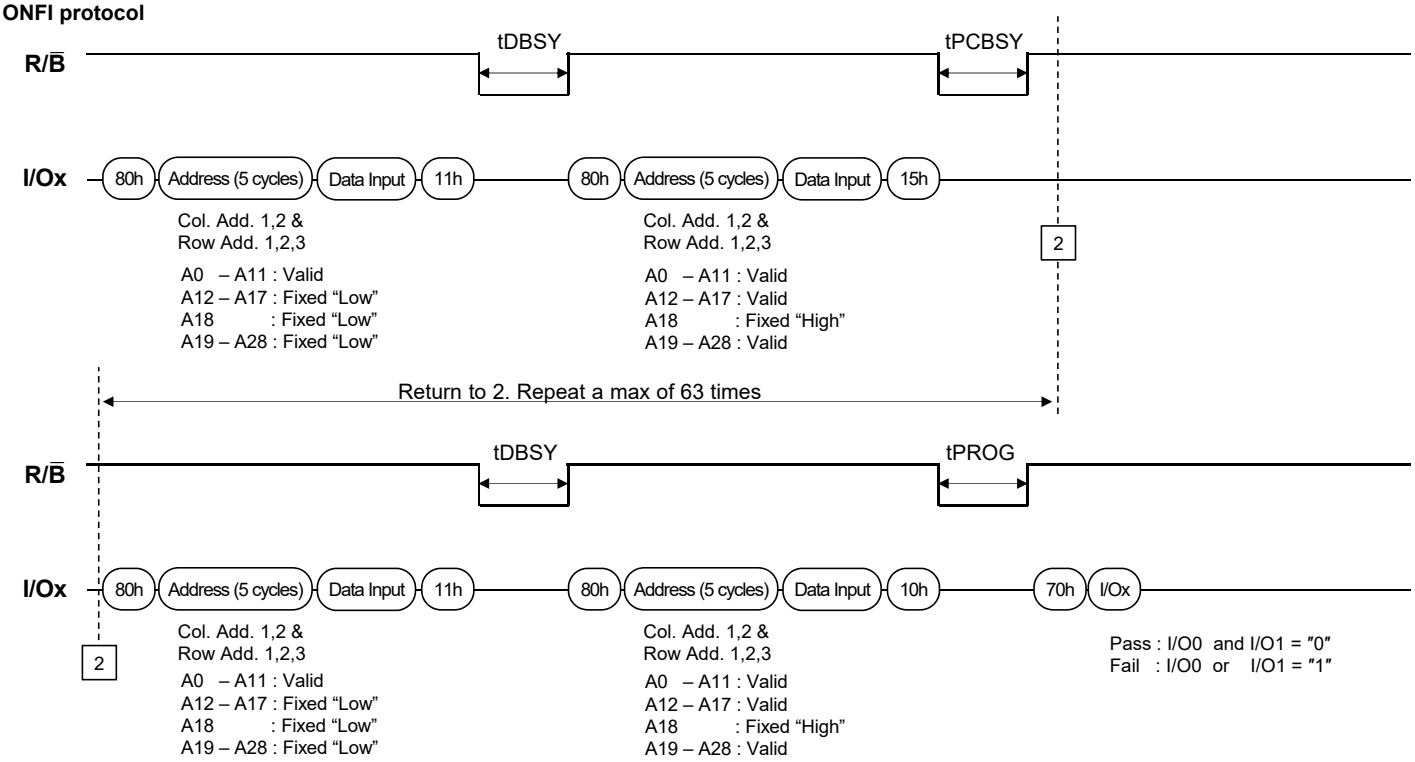


Figure 17. Multiplane Cache Program Operation

NOTE :
Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

4.14 Block Erase Operation

The Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command(60h). Only address A_{18} to A_{28} is valid while A_{12} to A_{17} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify.

Once the erase process starts, the Read Status Register commands (70h or 78h) may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/$\overline{B}$ output, or the status bit SR[I/O 6] of the Status Register. Only the Read Status Register commands (70h or 78h) and Reset command are valid while erasing is in progress.

When the erase operation is completed, the Write Status Bit SR[I/O 0] may be checked.

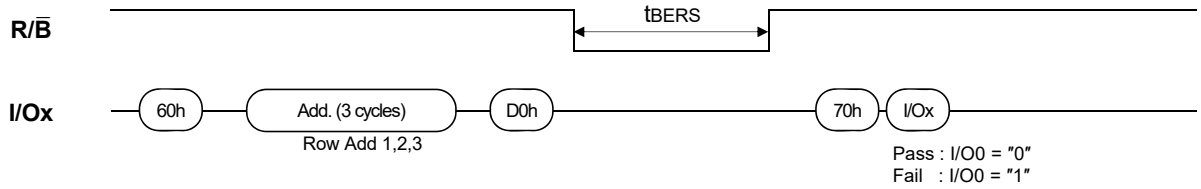


Figure 18. Block Erase Sequence

4.15 Multiplane Block Erase Operation

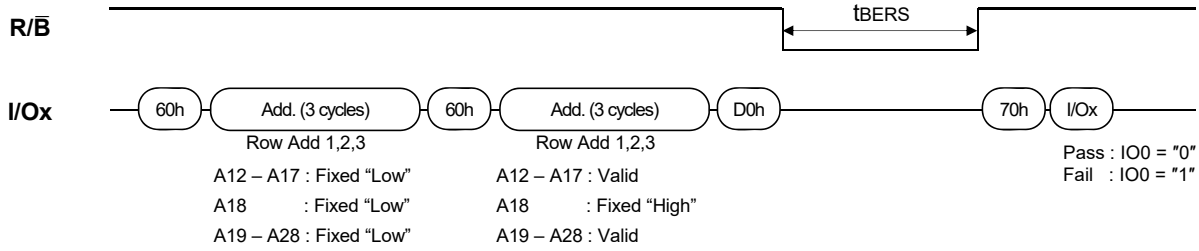
Multiplane erase allows parallel erase of two blocks in parallel, one per each memory plane. Two different command sequences are allowed in these case, traditional and ONFI 1.0. In case of traditional, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation to start. In this case, multiplane erase does not need any Dummy Busy Time between 1st and 2nd block insertion.

As an alternative, the ONFI 1.0 multiplane command protocol can be used, with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multiplane confirm). Between the two block-related sequences, a short busy time tIEBSY will occur.

Address limitation required for multiple plane program applies also to multiple plane erase. Also operation progress can be checked like in the multiple plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced.

As for multiplane page program, the address of the first second page must be within the first plane (A_{18}=0) and second plane (A_{18}=1), respectively.

*** Traditional protocol**



*** ONFI protocol**

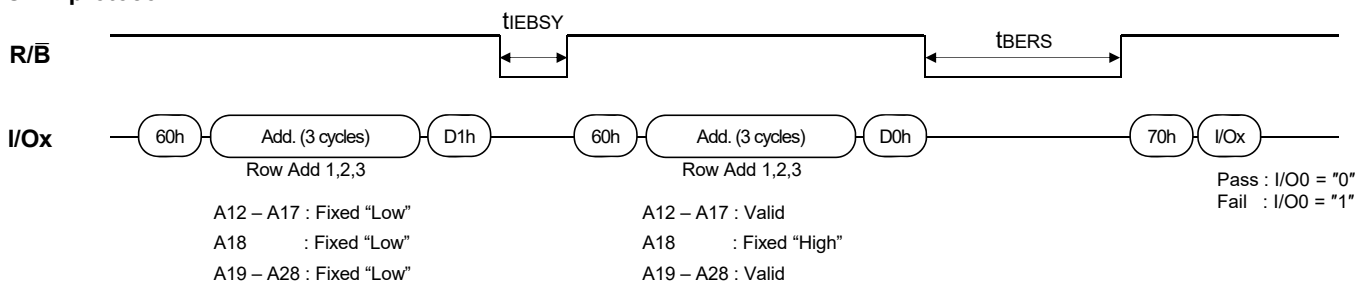


Figure 19. Multiplane Block Erase Sequence

4.16 Read Status Register

The device contains a Status Register which may be read to find out whether read program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/ O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 13 for specific Status Register definitions. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

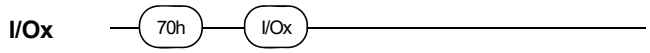


Figure 20. Read Status Register Sequence

4.17 Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the following cases :

- on a specific plane in case of multi-plane operations.

The plane address must be specified in the command sequence in order to retrieve the status of the plane of interest. Refer to Table 13 for specific Status Register definition. The command register remains in Status Read mode until further commands are issued.

Status register is dynamic in other words, user is not required to toggle $\overline{RE}$ / $\overline{CE}$ to update it

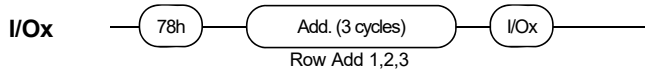


Figure 21. Read Status Register Sequence

[Table 13] Status Register Definition

SR bit	Page Program	Block Erase	Read	Cache Read	Cache Program Cache Reprogram	Definition
I/O 0	Pass / Fail	Pass / Fail	Not use	Not use	Pass / Fail	N page, Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Not use	Not use	Pass / Fail	N-1 page, Pass : "0" Fail : "1"
I/O 2	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O 3	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready / Busy Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data Cache Ready/Busy Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Not Use	Write Protect	Protected : "0" Not Protected : "1"

NOTE :

1) I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to one.
2) I/O1: This bit is only valid for Cache Program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache Program sequence. When Cache Program is not supported, this bit is not used.
3) I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.
4) I/O6: If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the last command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the last operation is complete.

4.18 Read ID

4.18.1 00h Address ID Definition

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ADh), and the device code and 3rd, 4th and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 22 shows the operation sequence.

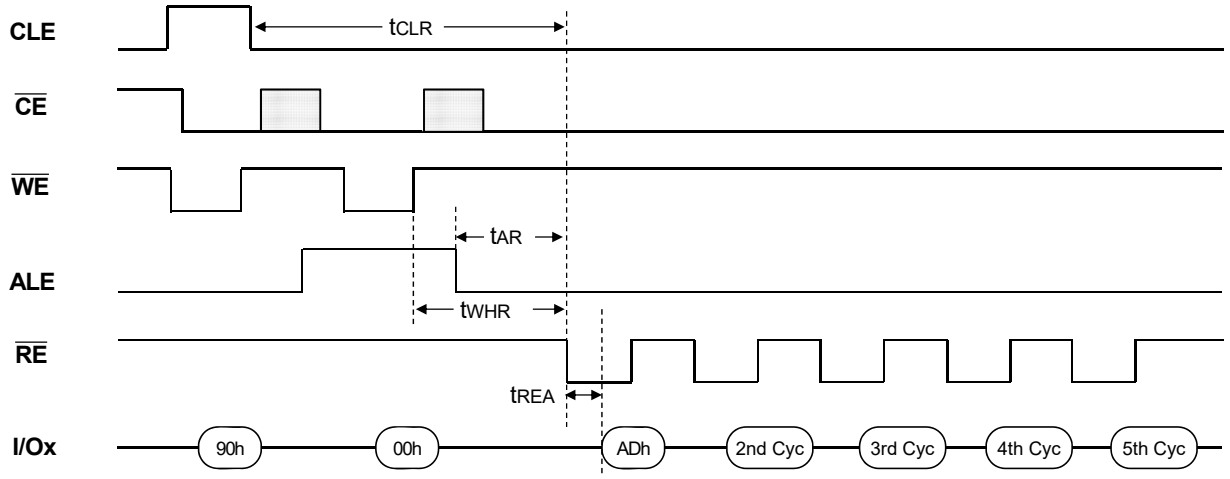


Figure 22. Read ID Sequence

4.18.2 00h Address ID Cycle

[Table 14] 00h Address ID cycle

Device		1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle
S8F2G08U0A	3.3V	ADh	DAh	90h	95h	46h
S8F2G08S0A	1.8V	ADh	AAh	90h	15h	46h

[Table 15] 00 Address ID Definition Table

Device Identifier Byte	Description
1st Byte	Manufacturer Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache
4th Byte	Page Size, Block Size, Spare Size, Organization, Serial Access Minimum
5th Byte	ECC, Multiplane information

[Table 16] 3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Program Between multiple chips	Not Support		0						
	Support		1						
Cache Program	Not Support	0							
	Support	1							

[Table 17] 4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (without spare area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (without spare area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Spare Area Size (byte/512bytes)	16						0		
	32						1		
Organization	X8		0						
	X16		1						
Serial Access time (Minimum)	45ns	0				0			
	25ns	1				0			
	Reserved	0				1			
	Reserved	1				1			

[Table 18] 5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	1bit/512Byte							0	0
	2bit/512Byte							0	1
	4bit/512Byte							1	0
	8bit/512Byte							1	1
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size (without spare area)	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Reserved	Reserved	0							

NOTE : To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Section 5.15 shows the operation sequence .

4.19 Reset Operation

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin changes to low for tRST after the Reset command is written. Refer to Figure 23 below

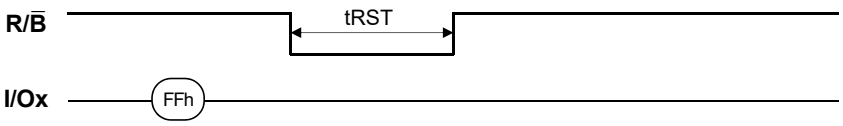


Figure 23. Reset Sequence

4.20 Read Parameter Page Operation

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. The whole data structure is repeated at least three times.
The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.
The Read Status may be used to check the status of Read Parameter Page during execution. After completion of the Read Status command, 00h shall be issued by the host on the command line to continue with the data output flow for the Read Parameter Page command. Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

4.20.1 Parameter Page Data Structure Definition

Table 19 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page.
For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

[Table 19] Parameter page data

Byte	O/M	Description
	Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Cache Read commands 0 1 = supports Page Cache Program command
10-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles

Byte	O/M	Description
	Memory organization block	
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
	Electrical parameters block	
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	t_{PROG} Maximum page program time (µs)
135-136	M	t_{BERS} Maximum block erase time (µs)
137-138	M	t_R Maximum page read time (µs)
139-163		Reserved (0)
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	M	Additional redundant parameter pages

Note : “O” stands for Optional, “M” for Mandatory

4.21 Ready/$\overline{\text{Busy}}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy), an appropriate value can be obtained with the following reference chart(Figure 24). Its value can be determined by the following guidance.

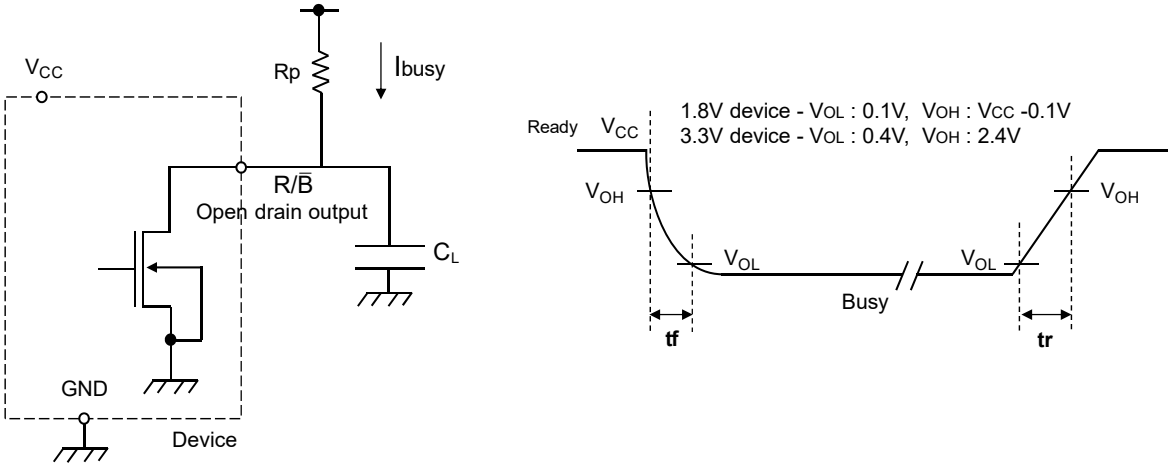
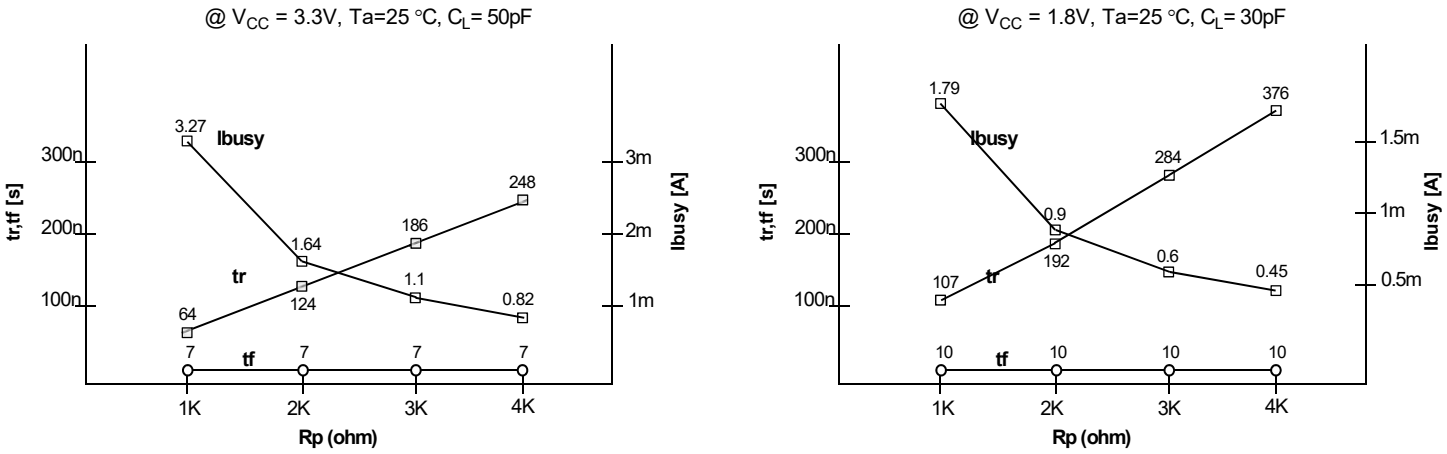


Figure 24. Rp vs tr, tf & Rp vs Ibusy



Rp value guidance

$$Rp(\text{min, 3.3V device}) = \frac{V_{CC}(\text{Max.}) - V_{OL}(\text{Max.})}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

$$Rp(\text{min, 1.8V device}) = \frac{V_{CC}(\text{Max.}) - V_{OL}(\text{Max.})}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

4.22 Write protect ($\overline{WP}$) handling

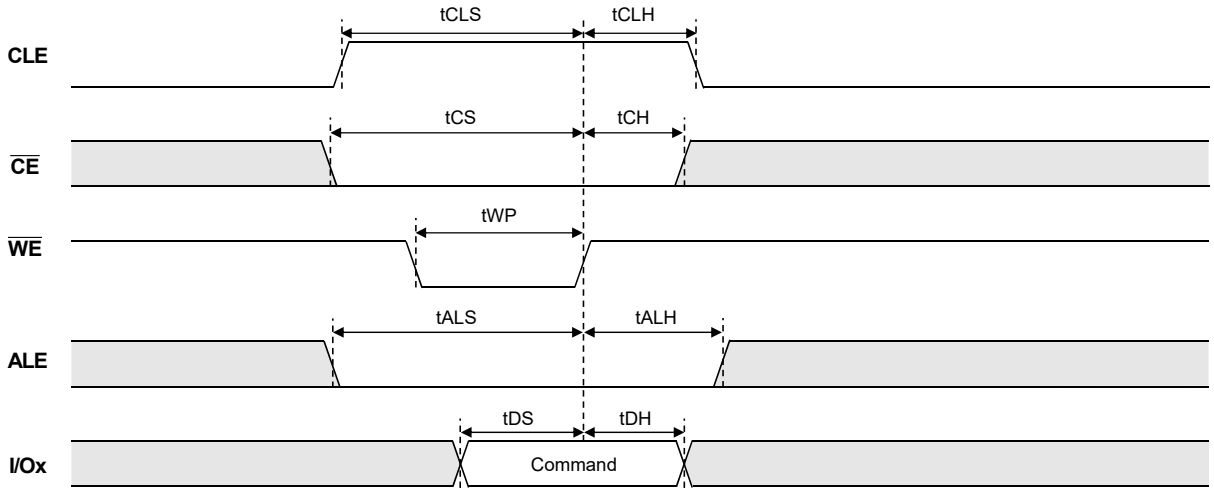
Erase and program operations are a aborted if $\overline{WP}$ is driven low during busy time, and kept low for about 100nsec. Switching $\overline{WP}$ low during this time is equivalent to issuing a Reset command (FFh).

The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/$\overline{B}$ pin will stay low for tRST(described in sections 5.17). At the end of this time, the command register is ready to process the next command, and the status bit SR[I/O 6] will be cleared to "1", while the status bit SR[I/O 7] value will be related to the $\overline{WP}$ value. Refer to Table 13 for more information on device status. Erase and program operations are enabled or disabled by setting $\overline{WP}$ to high or low respectively prior to issuing the setup commands (80h or 60h). The level of $\overline{WP}$ shall be set tWW prior to raising the $\overline{WE}$ pin for the set up command.

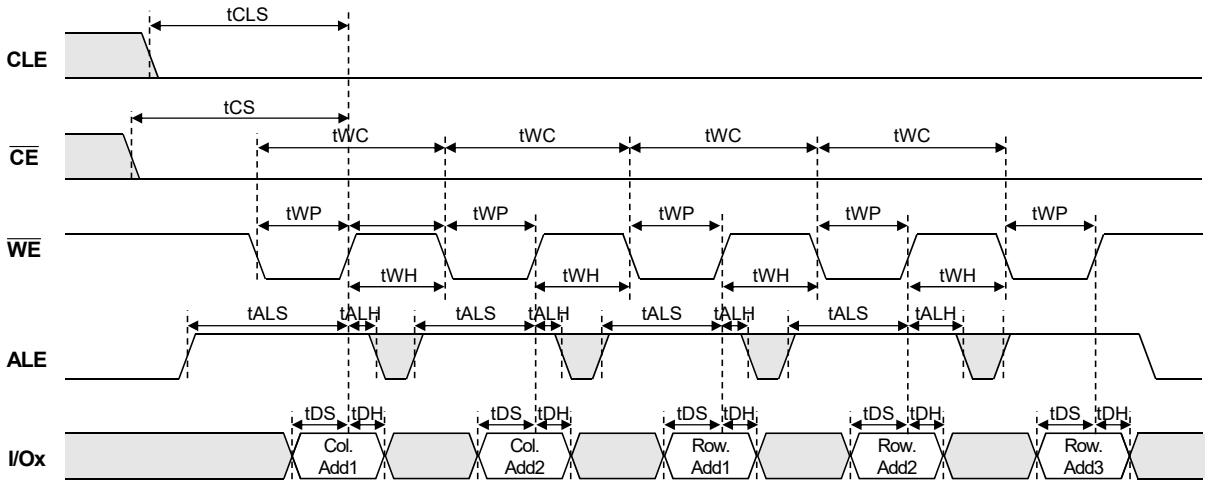
5.0 TIMING DIAGRAM

5.1 General Timing

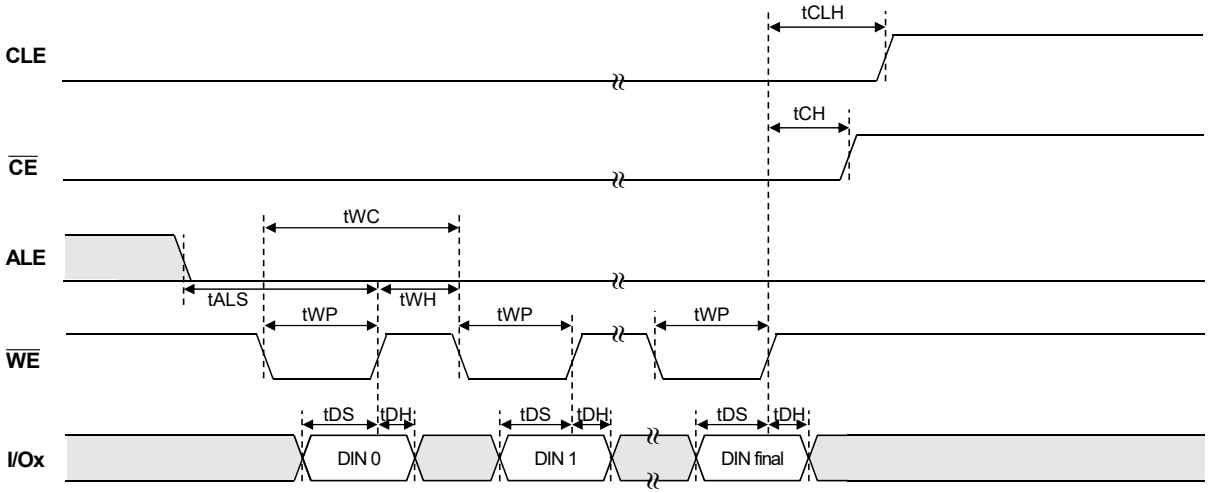
5.1.1 Command Latch Cycle



5.1.2 Address Latch Cycle

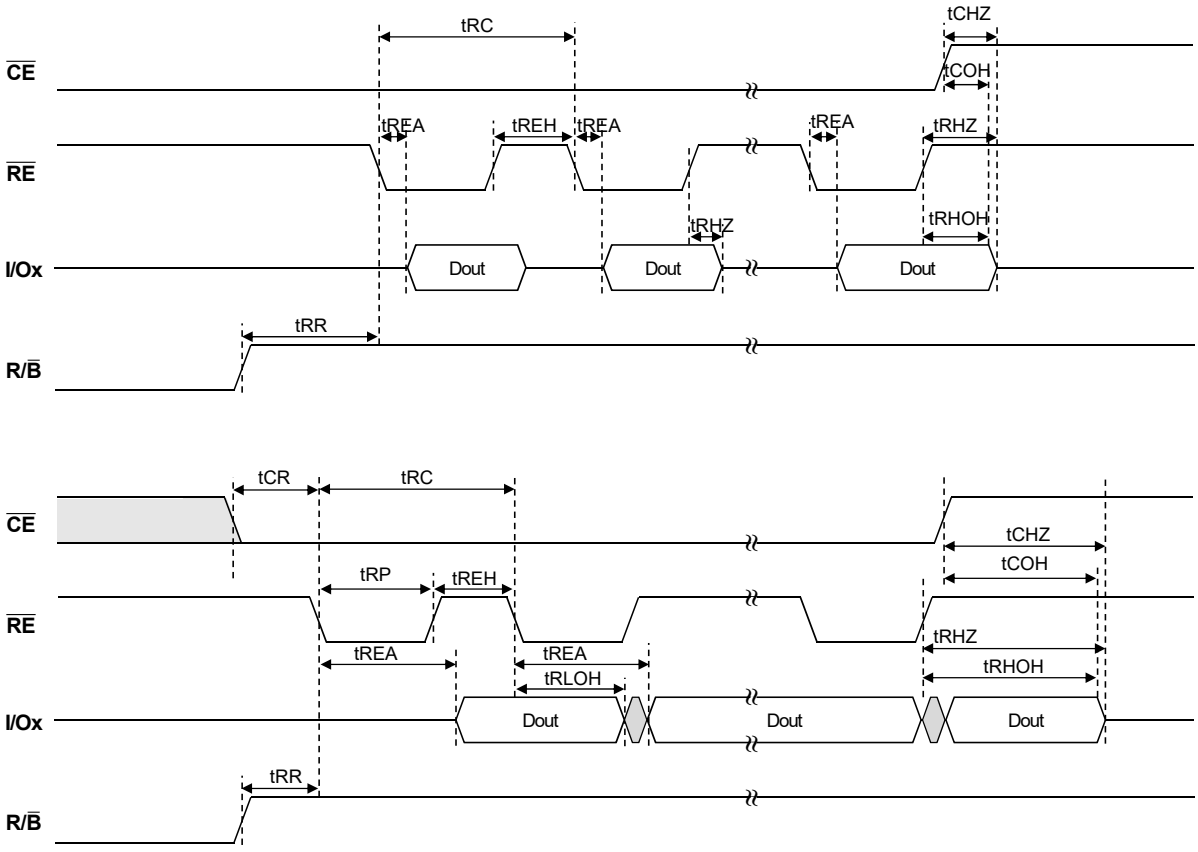


5.1.3 Input Data Latch Cycle



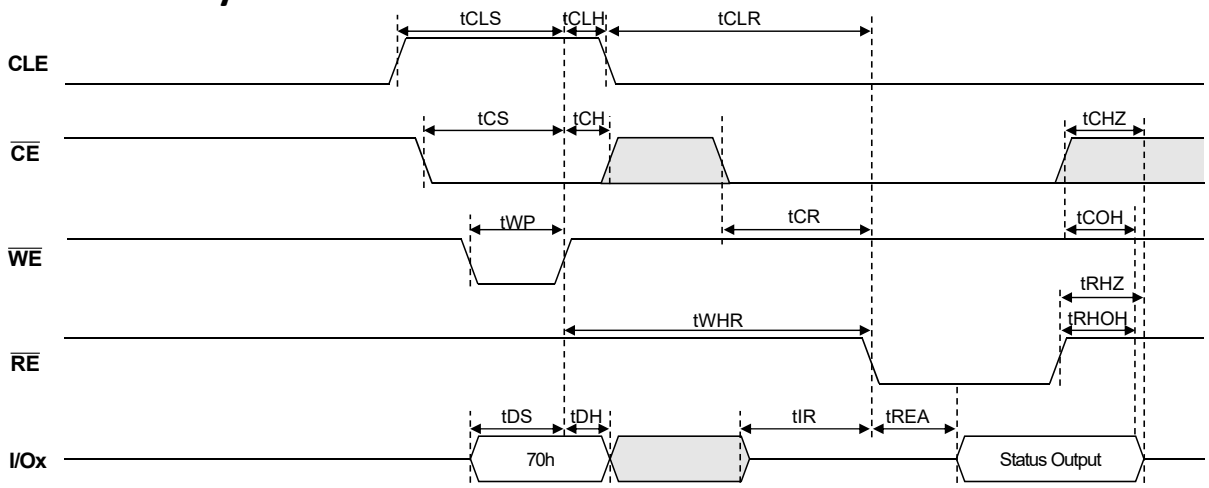
NOTE : Data Input cycle is accepted to data register on the rising edge of $\overline{WE}$, when CLE and $\overline{CE}$ and ALE are low, and device is not Busy state.

5.1.4 Serial Access Cycle after Read

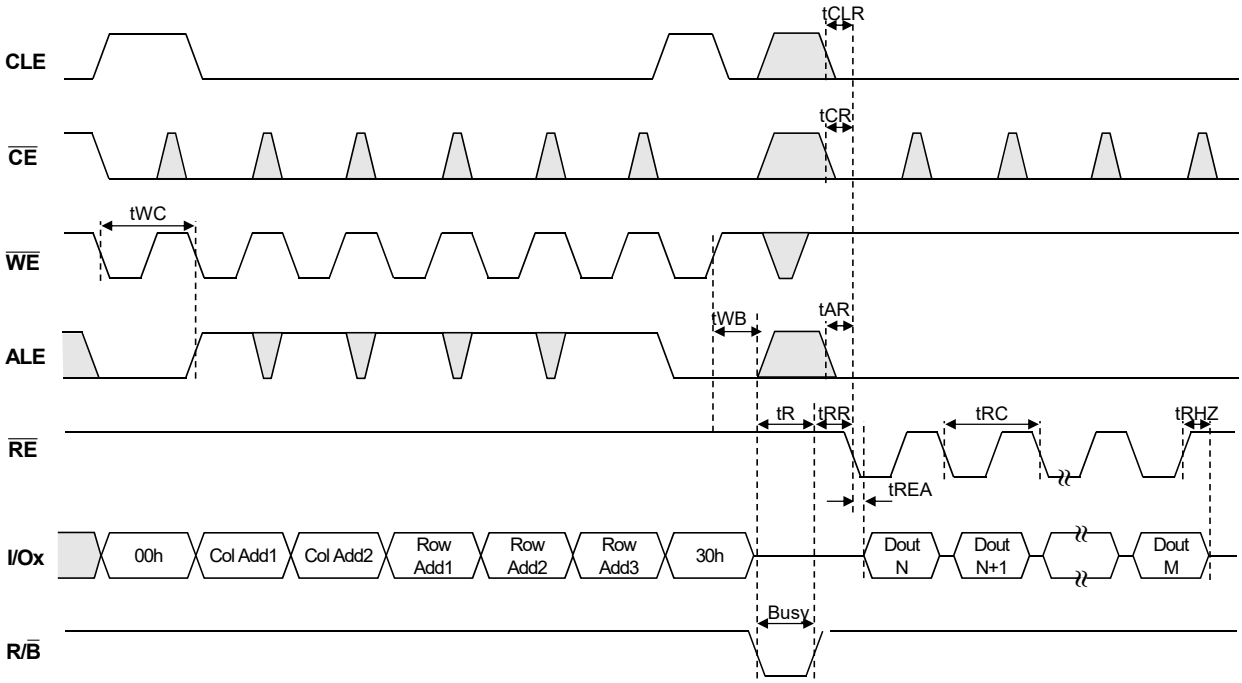


NOTE :
1)Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2) tRHOH starts to be valid when frequency is lower than 33Mhz.
3) tRLOH is valid when frequency is higher than 33MHz

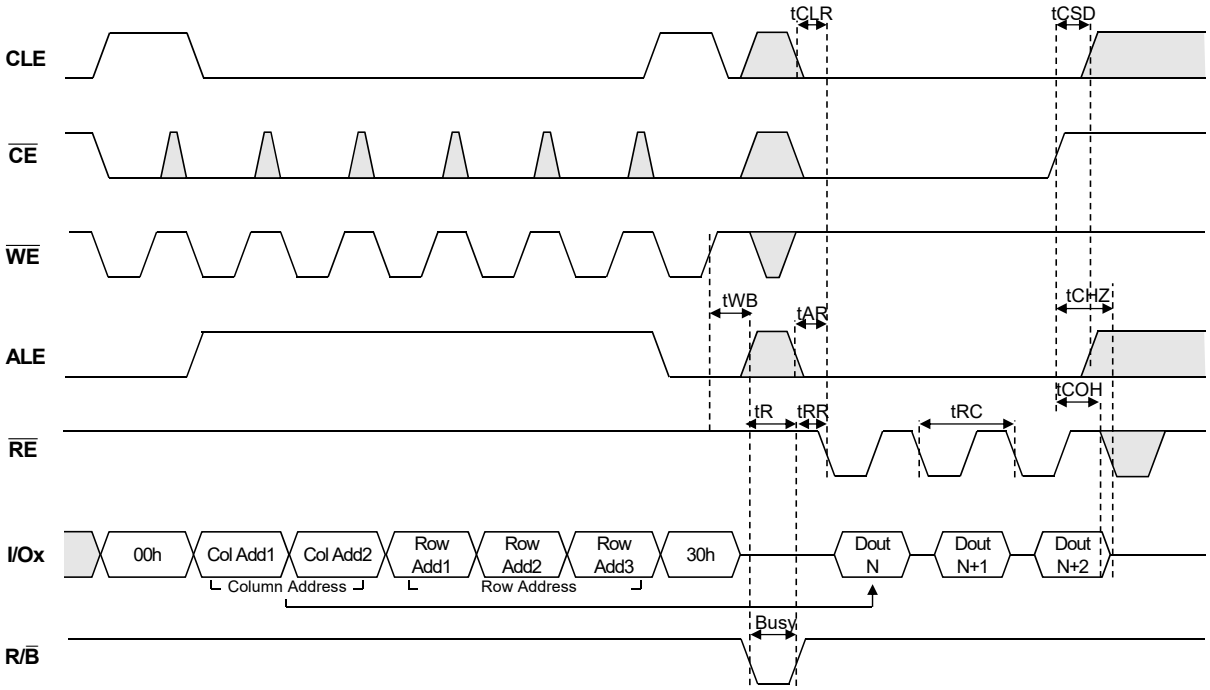
5.2 Read Status Cycle



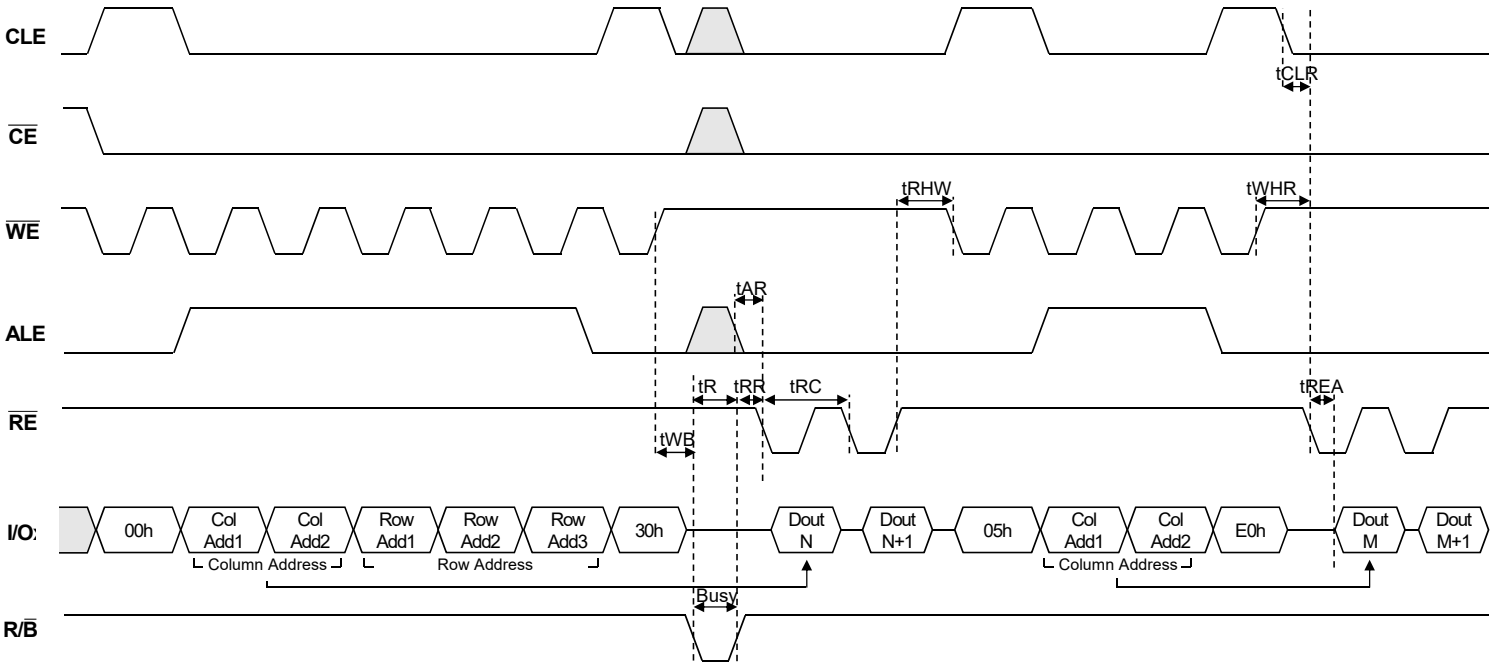
5.3 Read Operation (with $\overline{CE}$ don't care)



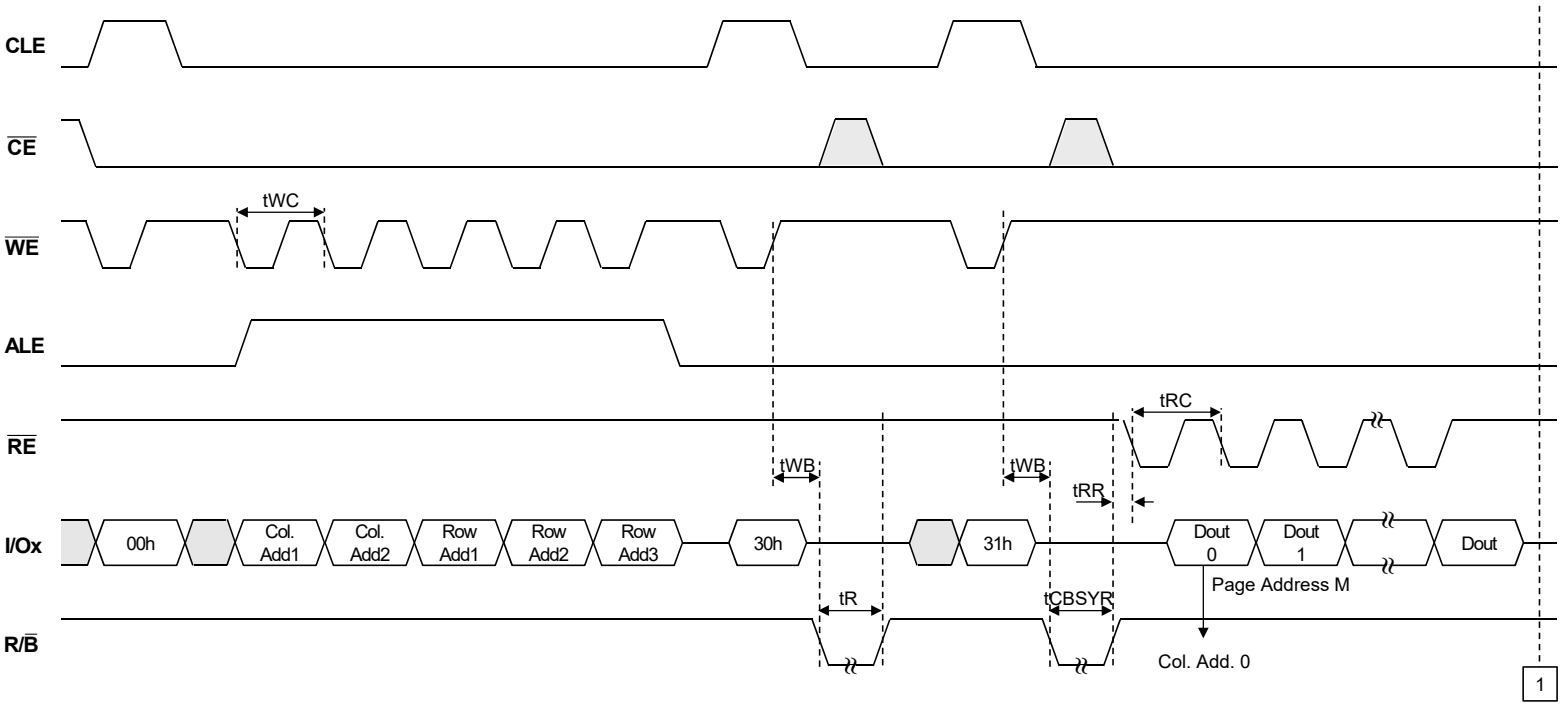
5.4 Read Operation (Intercepted by $\overline{CE}$)



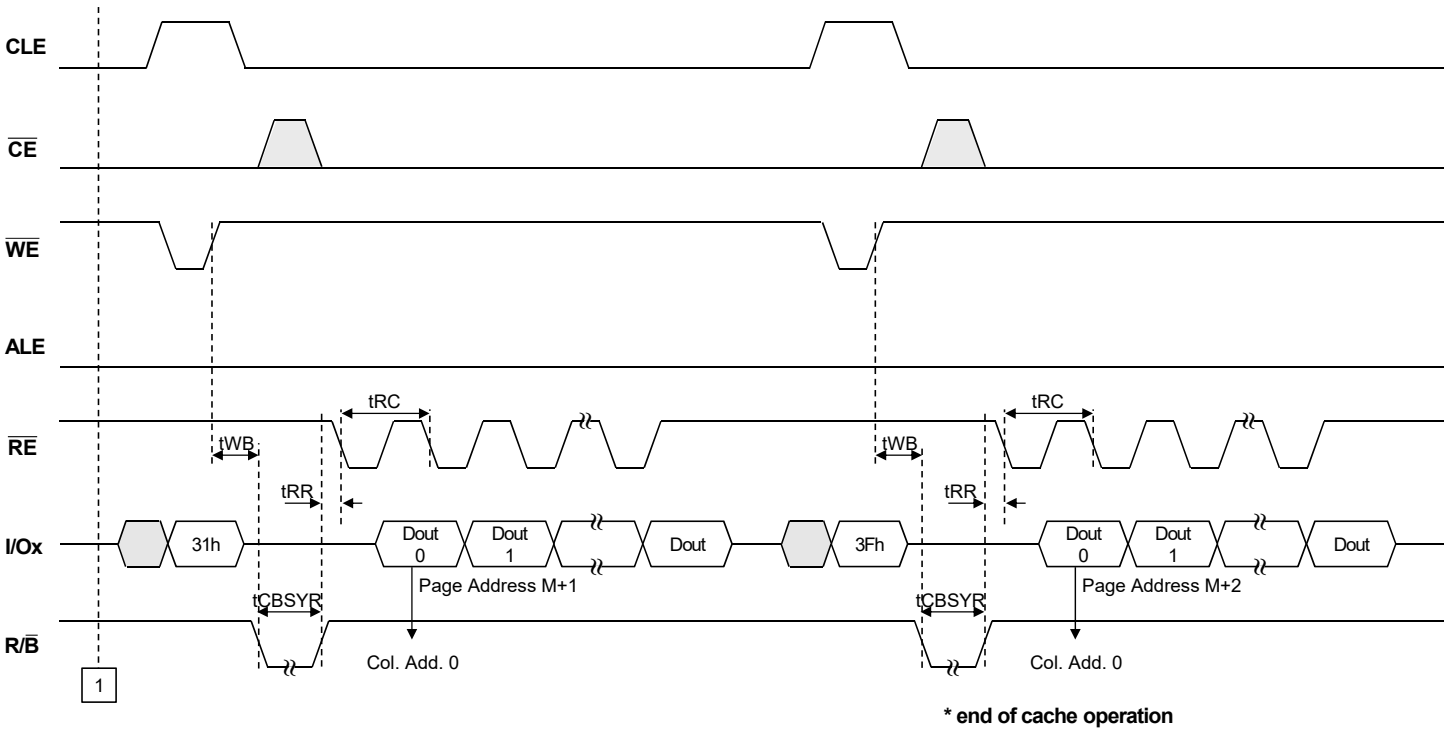
5.5 Random Data Output In a Page Operation



5.6 Cache Read Operation

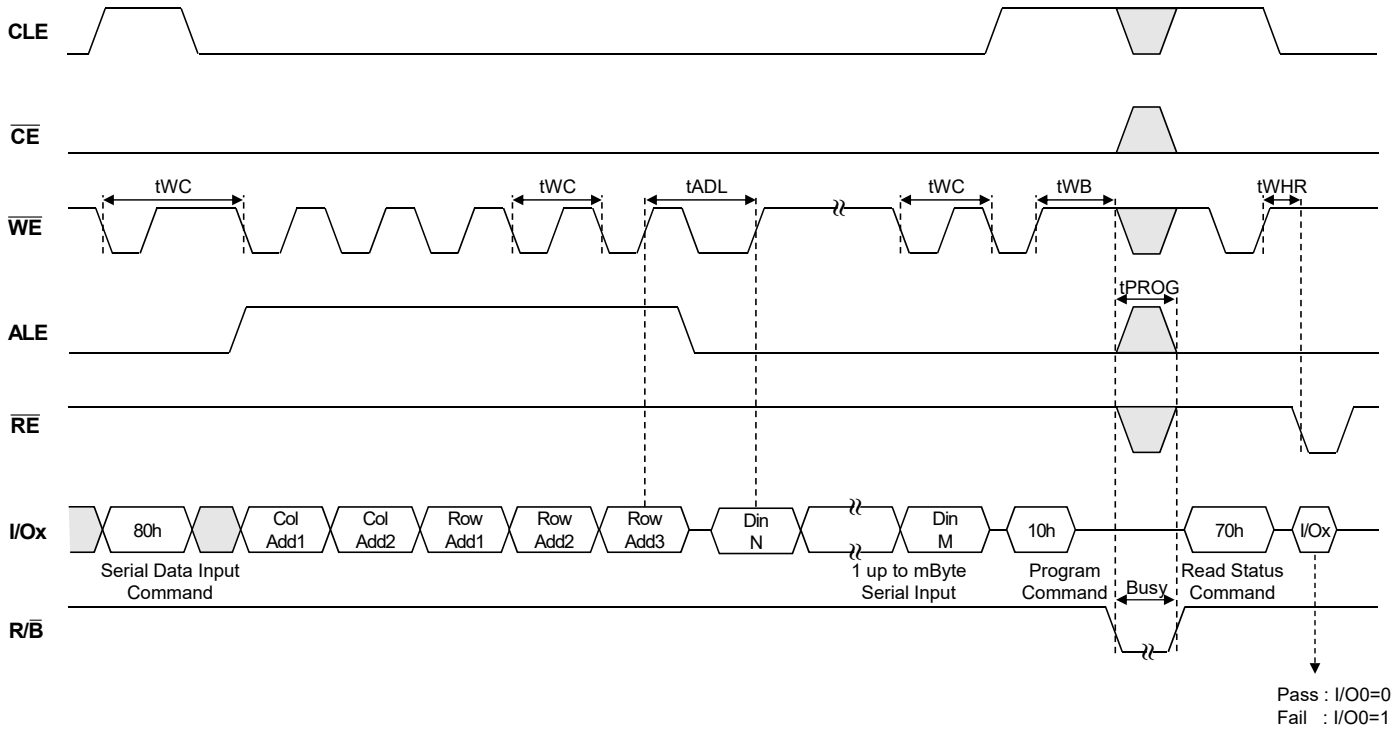


* start of cache operation



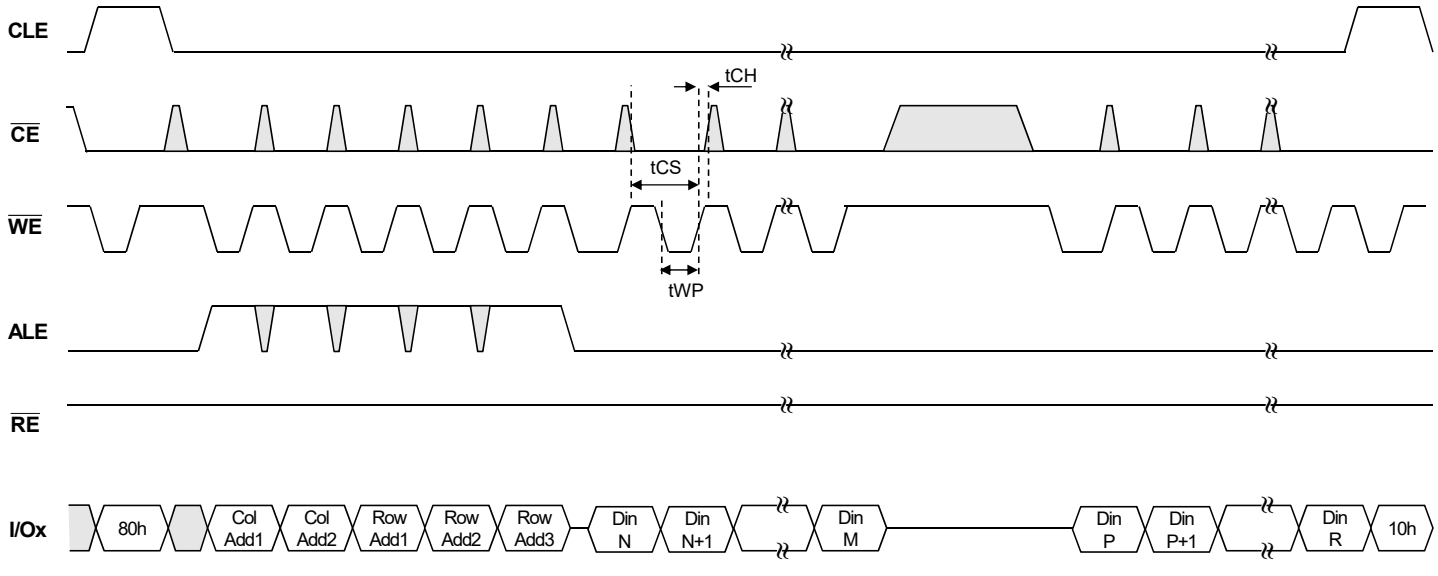
* end of cache operation

5.7 Page Program Operation



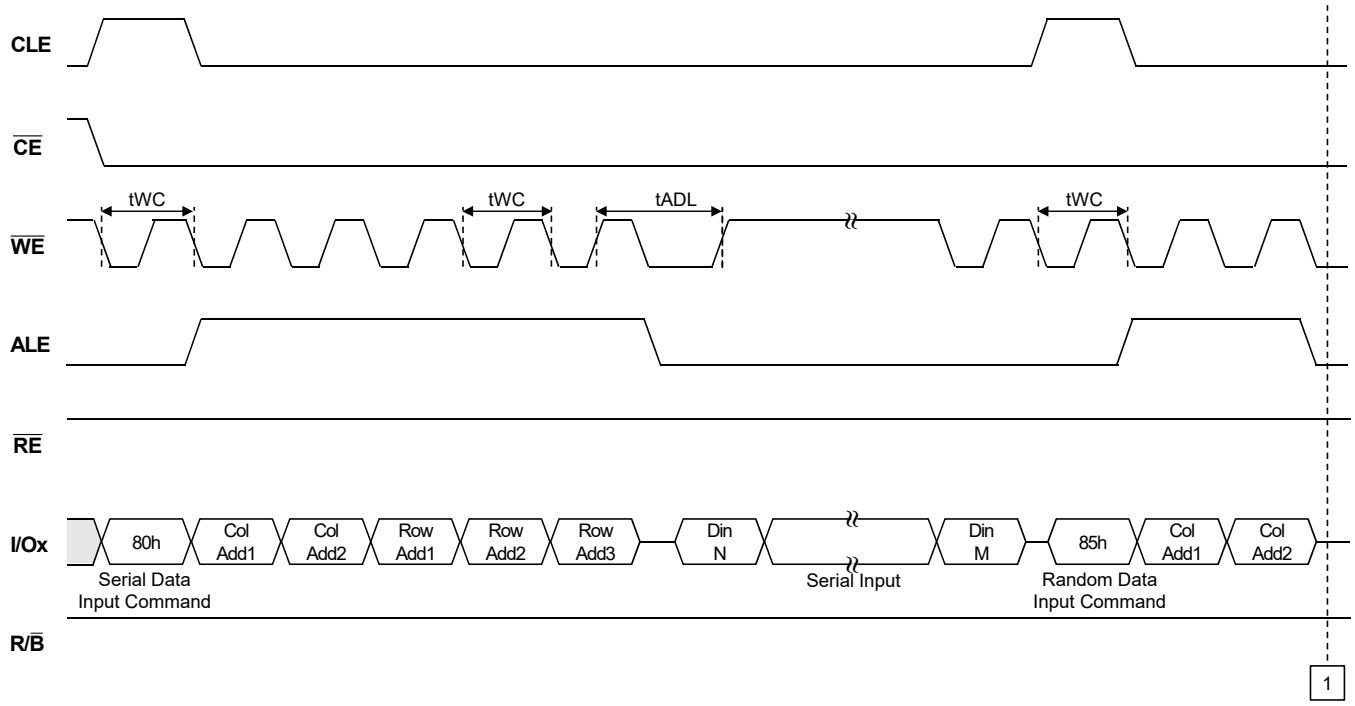
NOTE :
tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

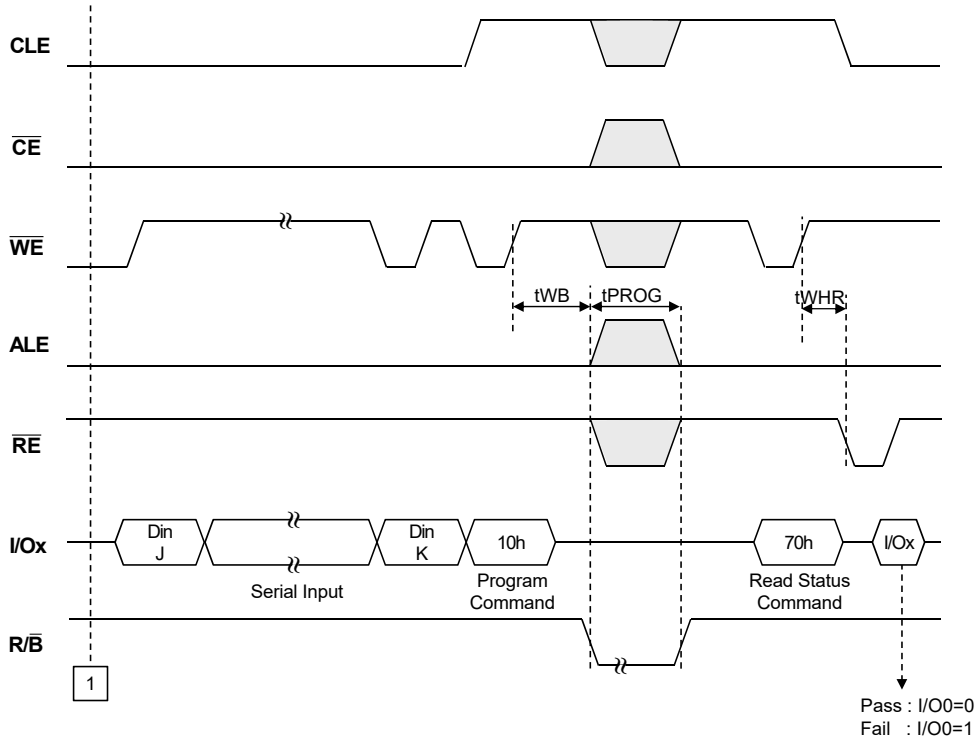
5.8 Page Program Operation (with $\overline{CE}$ don't care)



NOTE :
tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

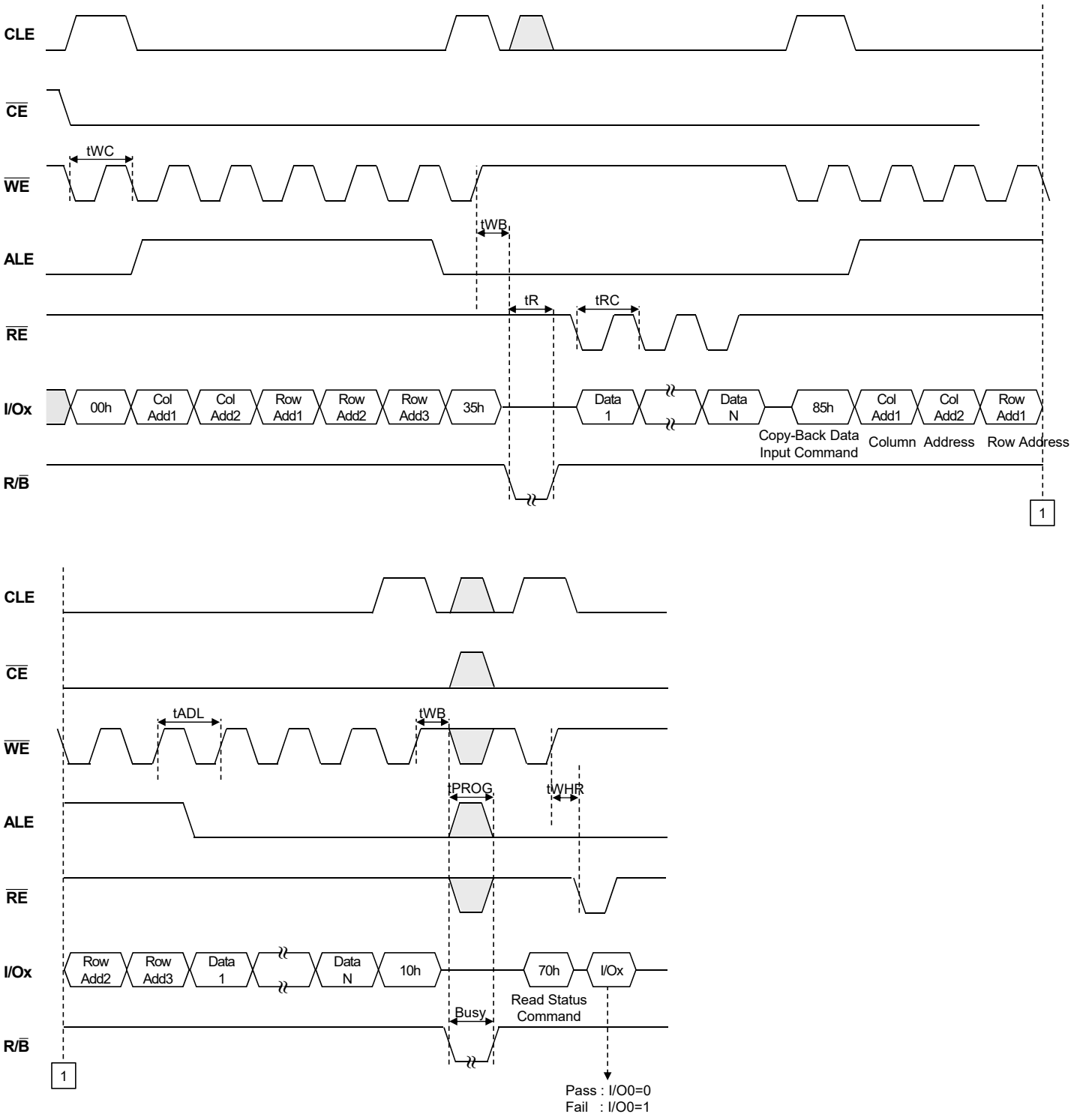
5.9 Page Program Operation with Random Data Input Operation





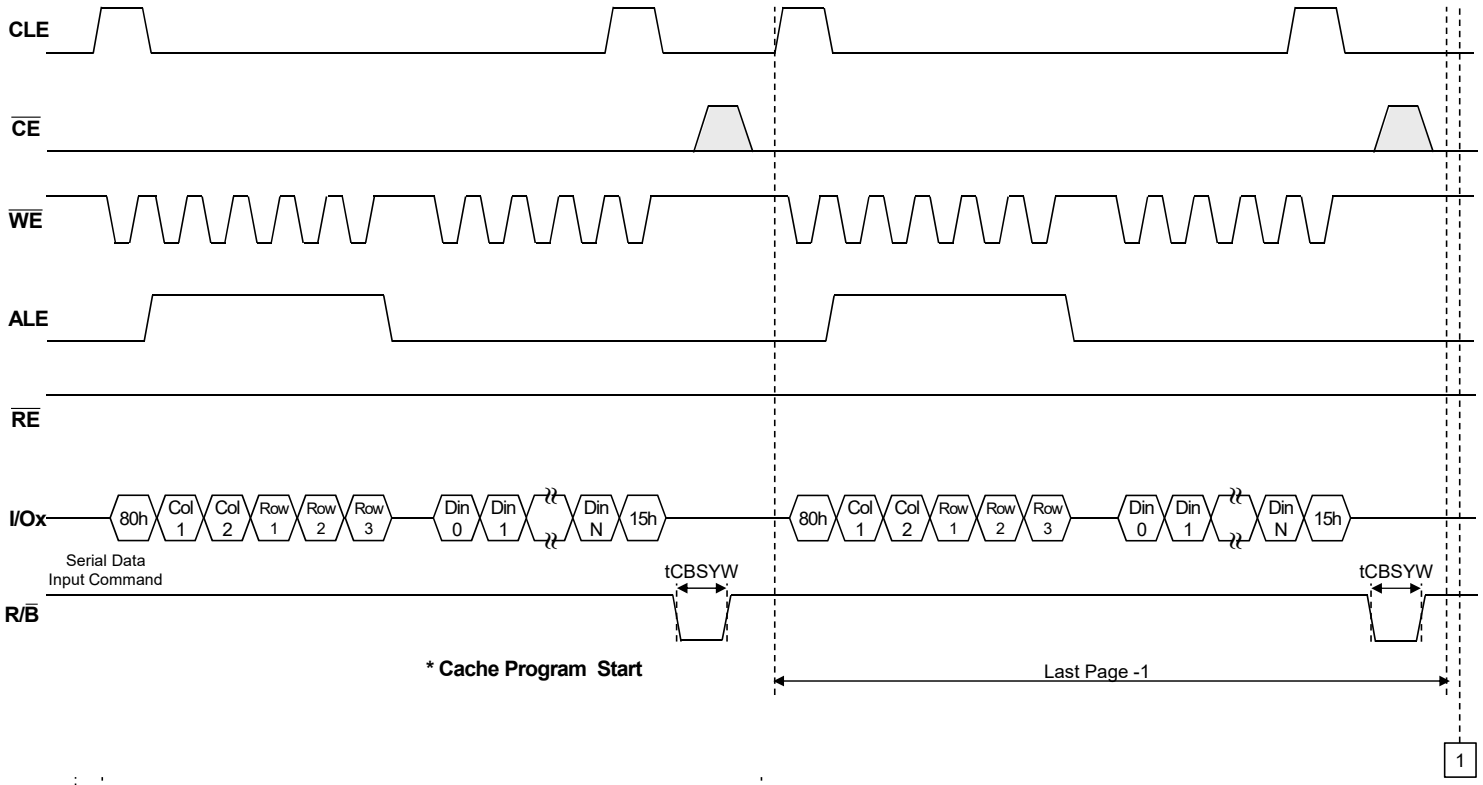
NOTE :
1) tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.
2) Random data input can be performed in a page.

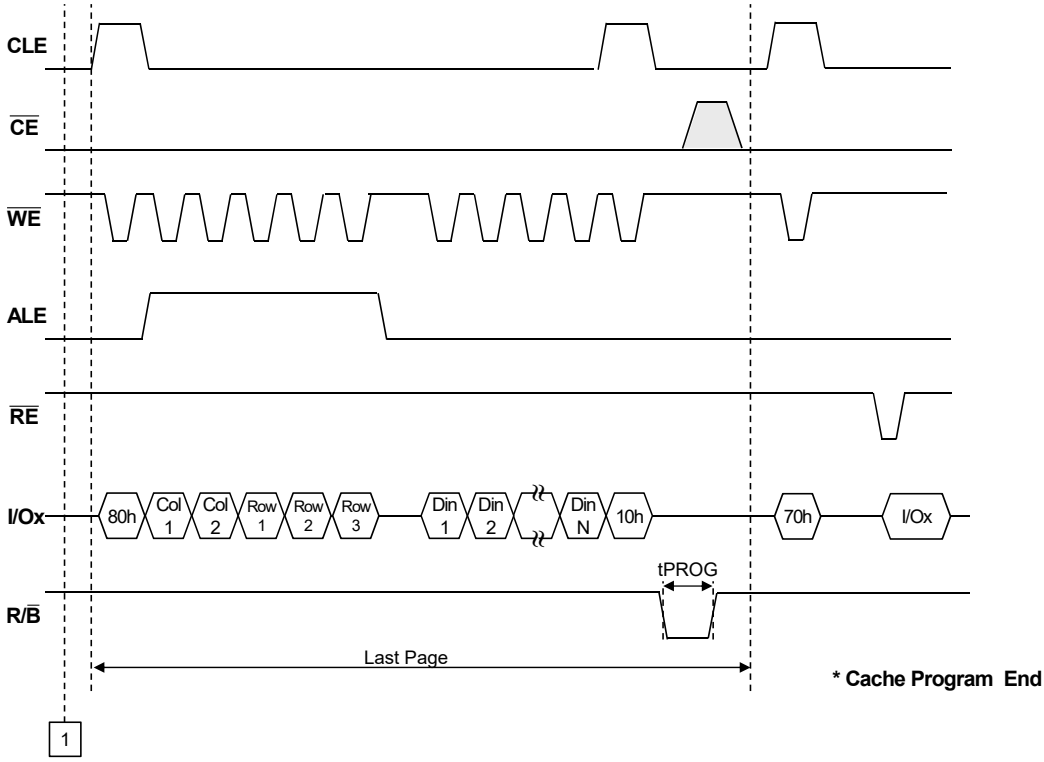
5.10 Copy-Back Program Operation with Random Data Input Operation



NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
2) On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

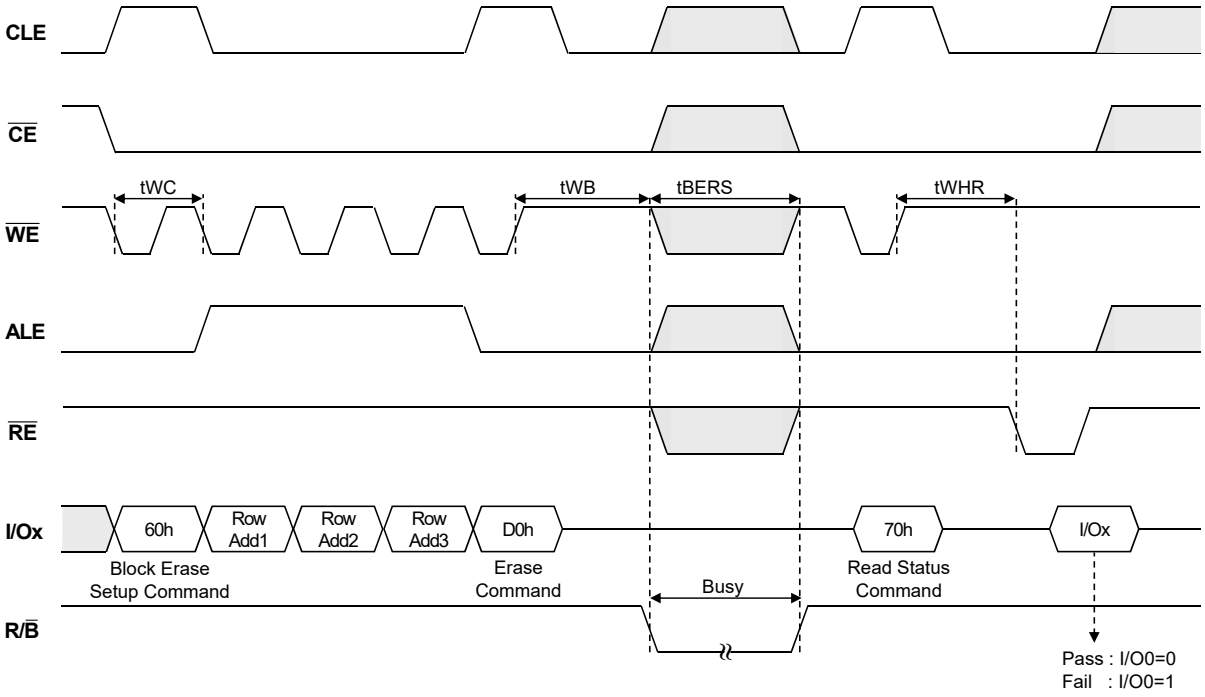
5.11 Cache Program Operation



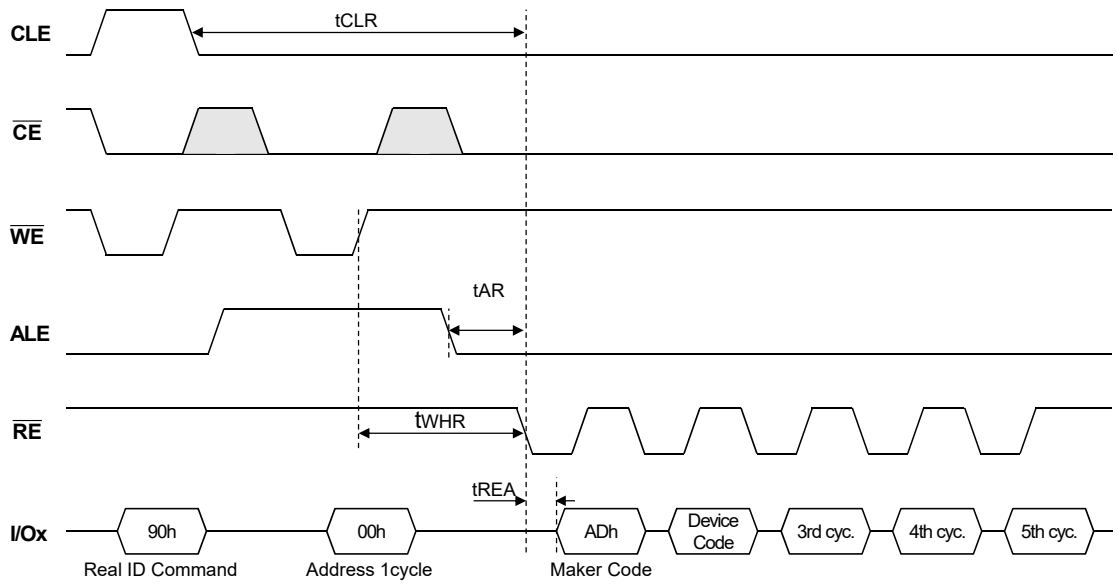


NOTE :
tPROG = Program time for the last page + Program time for the (last -1)th page - (command input cycle time + address input cycle time + Last page data loading time)

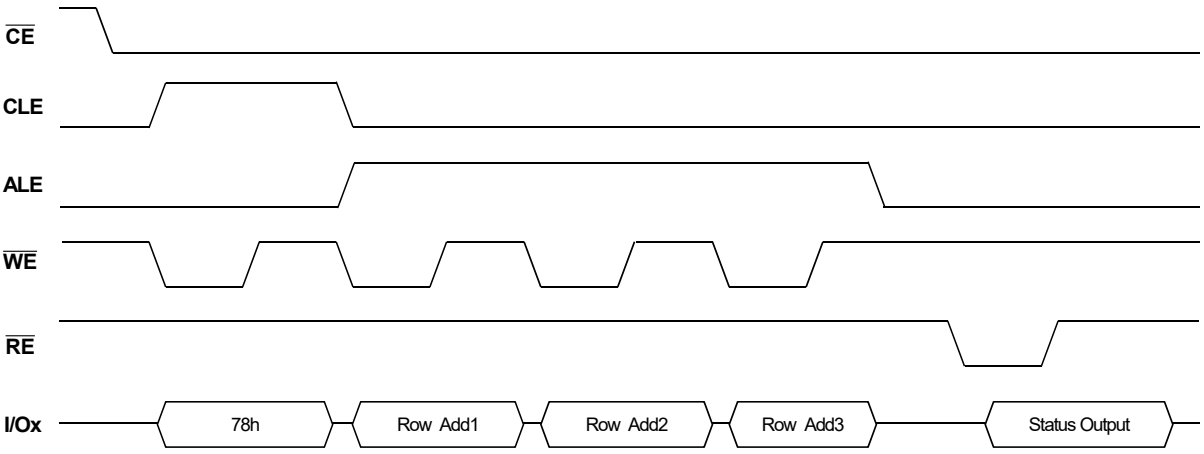
5.12 Block Erase Operation



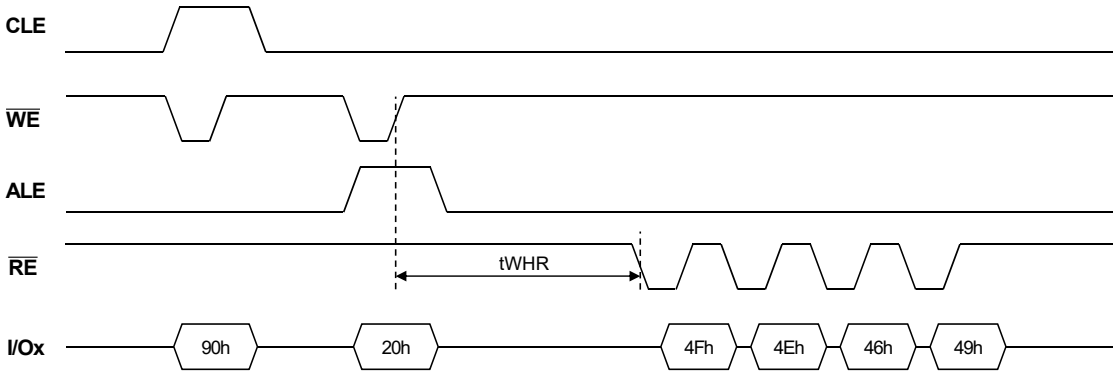
5.13 Read ID Operation



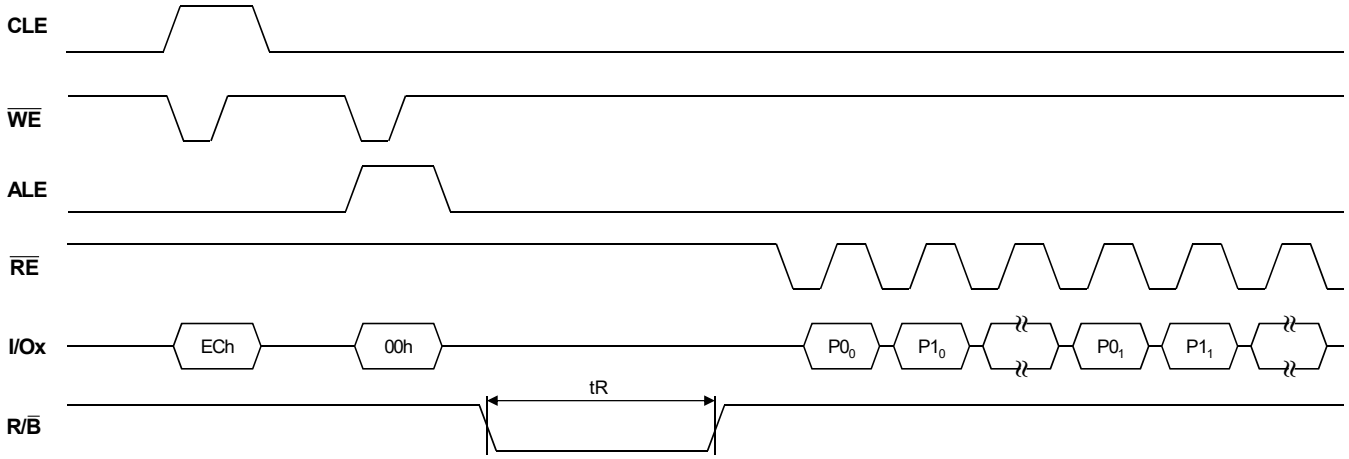
5.14 Read Status Enhanced



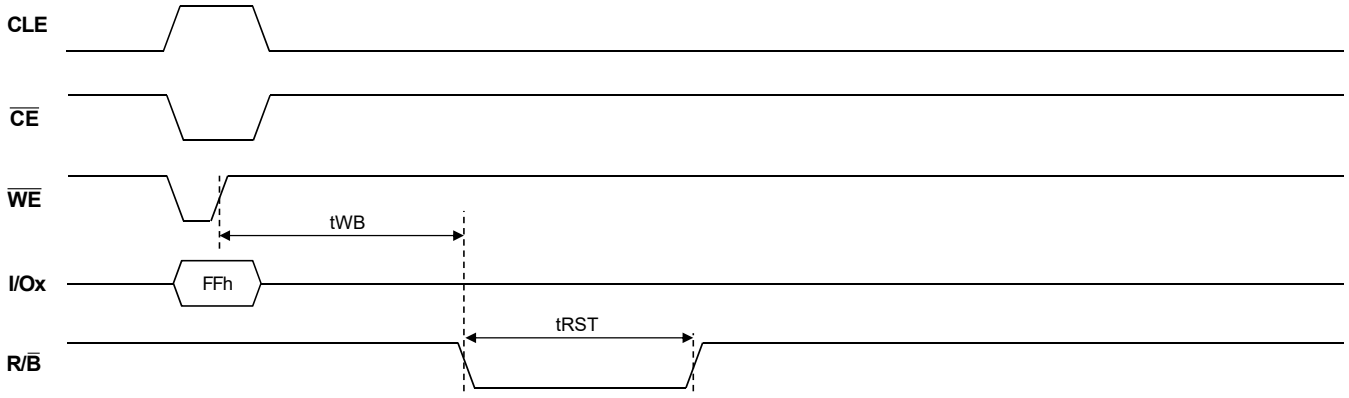
5.15 ONFI Signature Operation



5.16 Read Parameter Page Operation



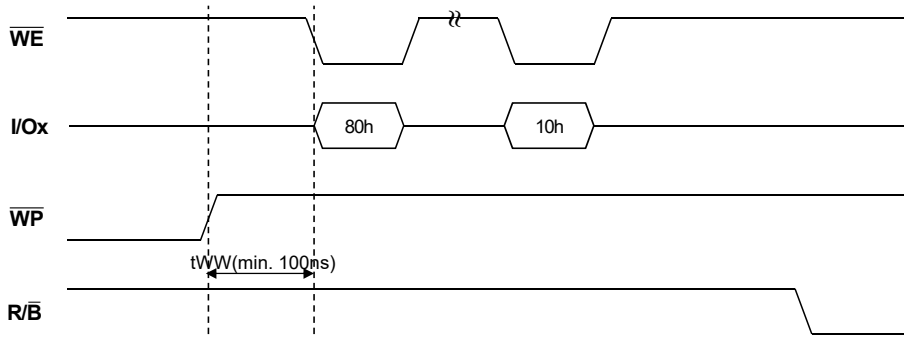
5.17 Reset Operation



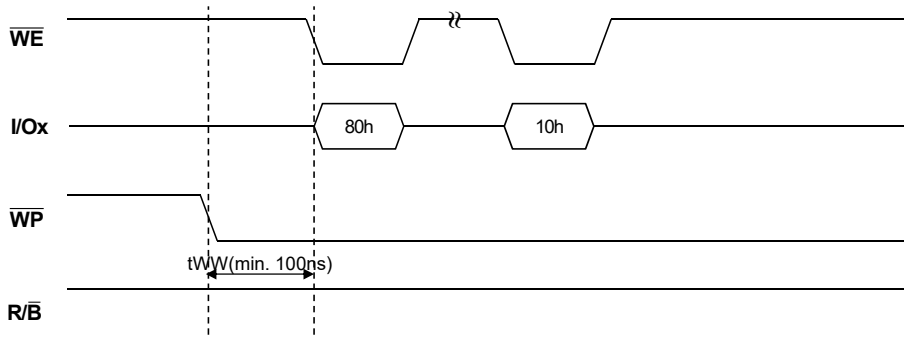
5.18 Write Protection Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min).
The operations are enabled and disabled as follows.

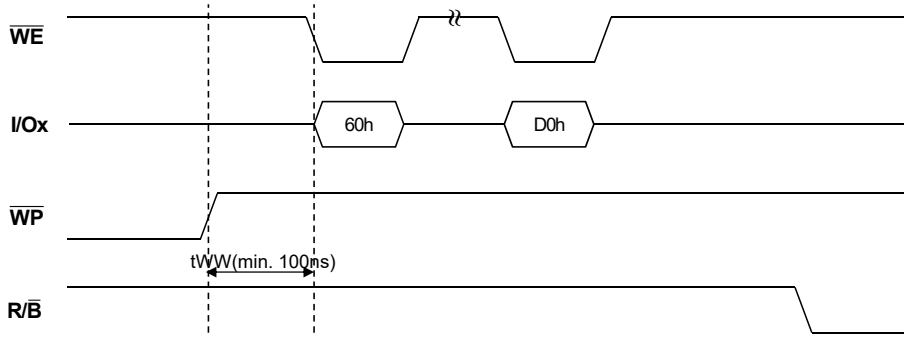
- **Program Enable Mode**



- **Program Disable Mode**



- **Erase Enable Mode**



- **Erase Disable Mode**