1Gb B-die (1.8V) NAND Flash

Single-Level-Cell (1bit/Cell)

datasheet

Revision History

Revision No.	History	Draft Date	Remark
1.0	Final version release	Dec. 2018	Final

Table Of Contents

1.0 INTRODUCTION

1.1 General Description

S8F1G08S0B is a 1G-bit NAND Flash Memory with spare 32M-bit. The device is offered in 1.8V V_{CC}. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 300μs on the (2K+64)Byte page and an erase operation can be performed in typical 3ms on a (128K+4K)Byte block. Data in the data register can be read out at 45ns cycle time per Byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The write operations can be locked using $\overline{WP}$ input pin. The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal. The device supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND flash memory device by a microcontroller, since the CE# transitions do not stop the read operation. The devices have a Read Cache feature that improves the read throughput for large files. During cache reading, the devices load the data in a cache register while the previous data is transferred to the I/O buffers to be read. The device also supports ONFI 1.0 specification.

1.2 Features

- Voltage Supply
  - V_{CC} : 1.8V (1.7V ~ 1.95V)

- NAND Interface
  - Command/Address/Data Multiplexed I/O Port
  - X8 I/O Bus

- Organization
  - Memory Cell Array : (128M + 4M) x 8bit
  - Page Size : (2K + 64)Byte
  - Data Register : (2K + 64)Byte

- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (128K + 4K)Byte

- Page Read Operation
  - Random Read : 25μs(Max.)
  - Serial Access : 45ns(Min.)

- Fast Write Cycle Time
  - Page Program time : 300μs(Typ.)
  - Block Erase Time : 3ms(Typ.)

- Copy Back Program
  - Fast data copy without external buffering

- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions

- Data Retention
  - 50K Program / Erase Cycles (With 4bit/528byte ECC)
  - Data Retention : 10 years

- Chip Enable Don't Care Option
  - Simple interface with microcontrollers

- Command Set
  - ONFI 1.0 Compliant command set
  - Read unique ID

- Security
  - OTP area
  - Serial number (Unique ID)
  - Read ID2 extension
  - Non-volatile protection

- Package :
  - S8F1G08S0B-Bx[1]B0 : Pb-Free Package
    : 63Ball FBGA (9.0 x 11.0 x 1.0 mm)
  - S8F1G08S0B-Xx[1]B0 : Pb-Free Package
    : 48Ball FBGA (6.5 x 8.0 x 1.0 mm)

NOTE :
C : Commercial
I : Industrial

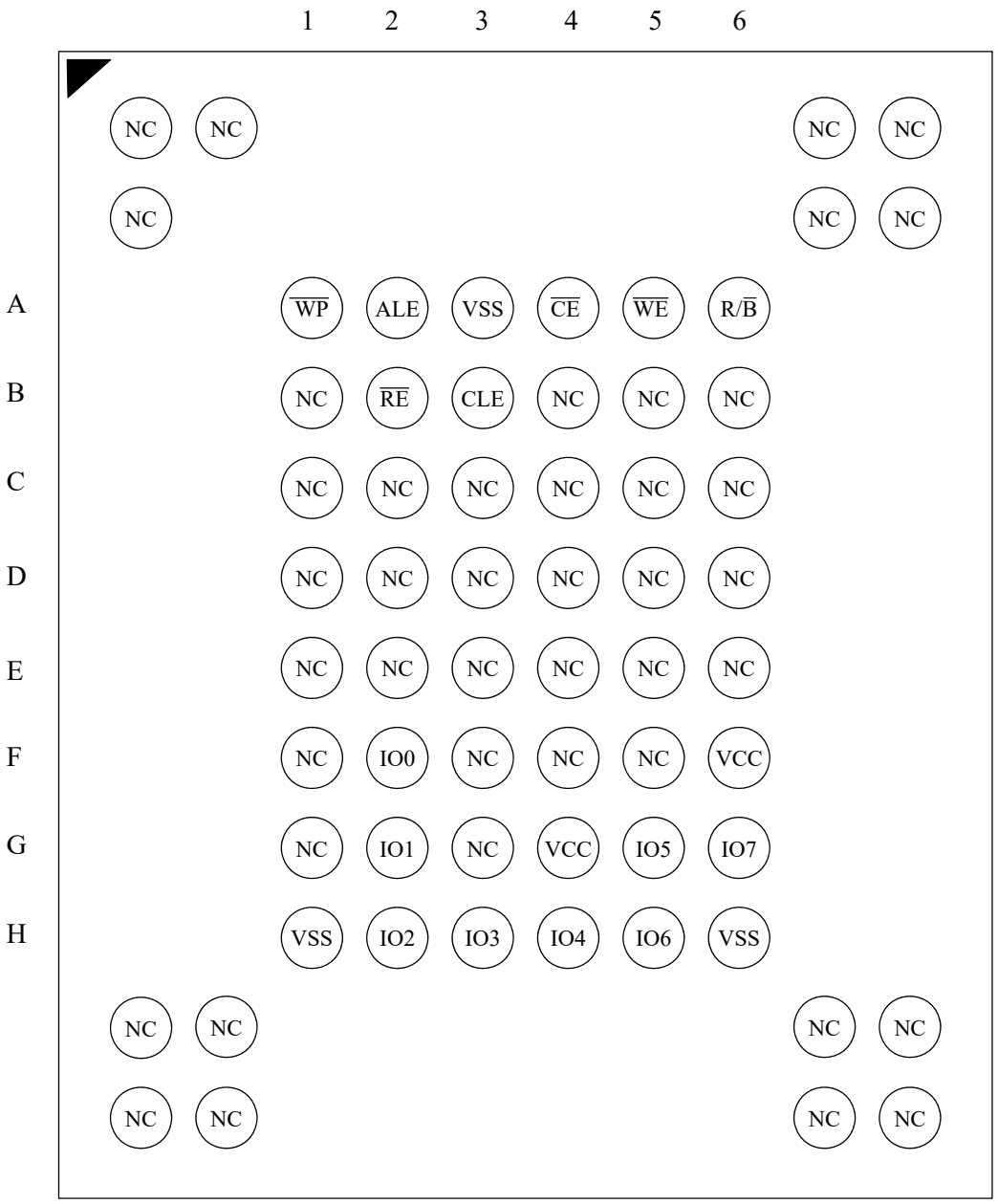
1.3 Product List

Part Number	Density	Organization	V_{CC} Range	PKG Type
S8F1G08S0B-B	1Gb	x8	1.7V ~ 1.95V	63FBGA
S8F1G08S0B-X	1Gb	x8	1.7V ~ 1.95V	48FBGA

1.4 Package

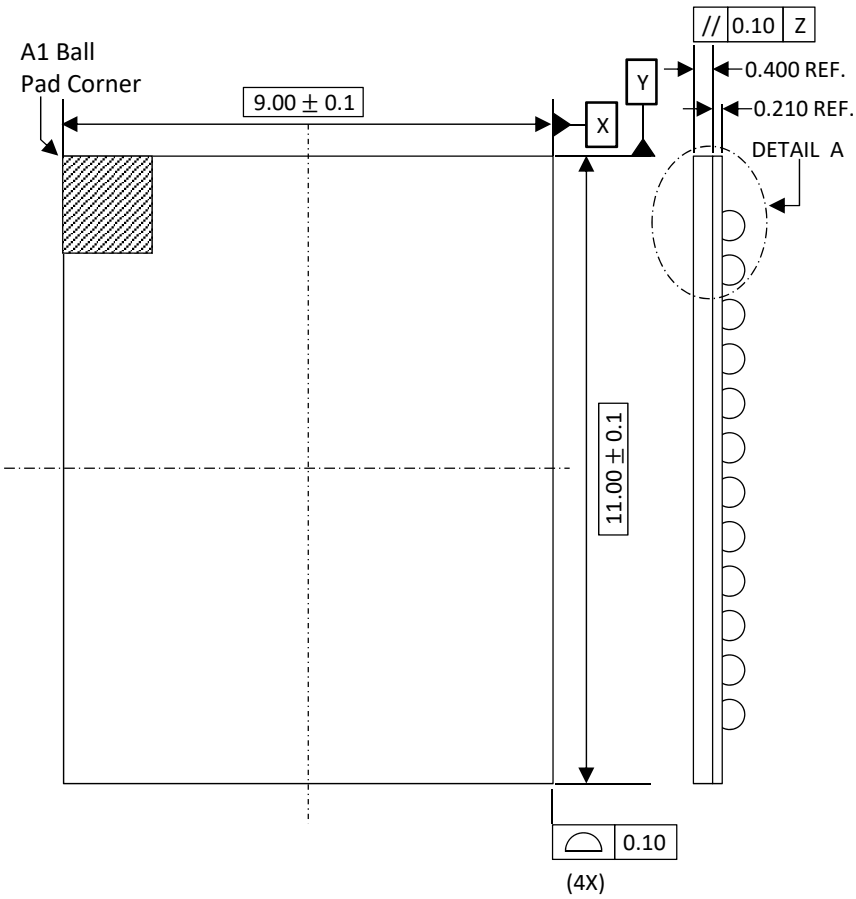
1.4.1 Pin Configuration (63 FBGA 9x11mm)

S8F1G08S0B-BxB0

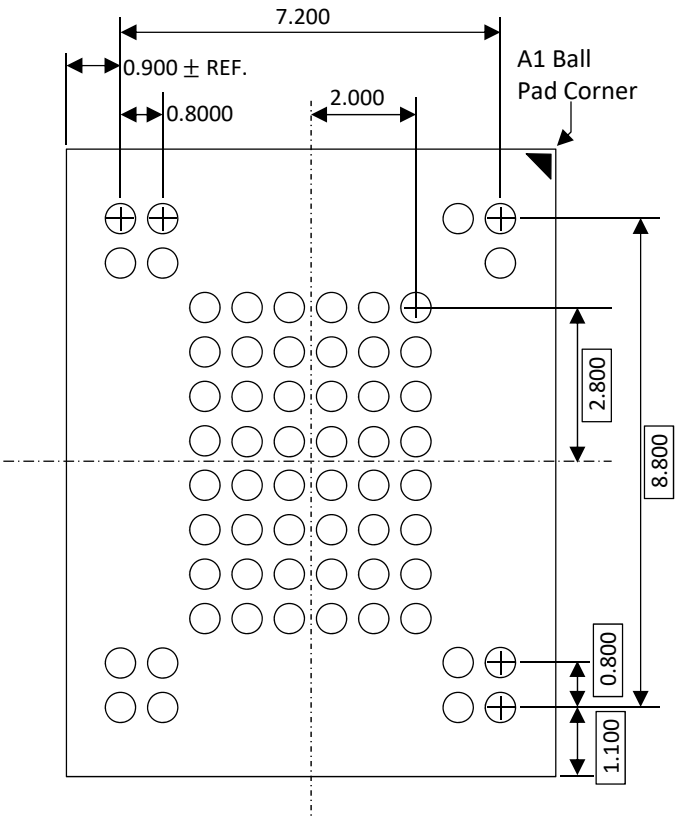


Top View

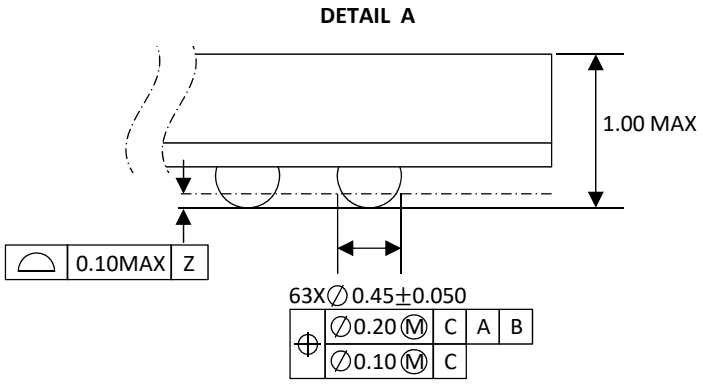
1.4.2 Package Dimensions (63 FBGA 9x11mm)



Top View



Bottom View

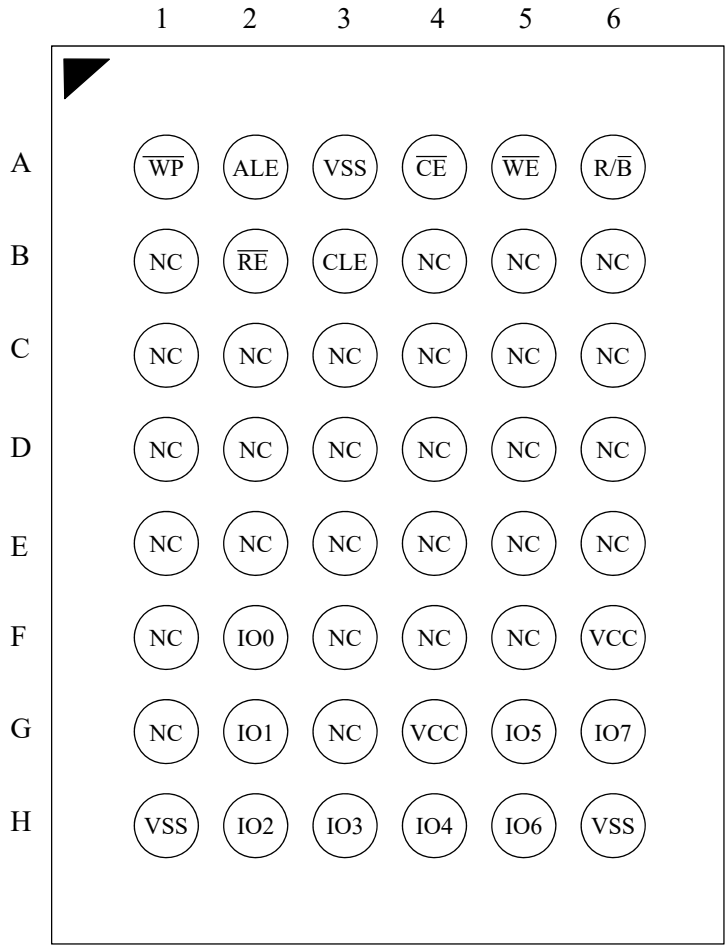


1. All Dimensions are in millimeters.
2. Post Reflow Solder Ball Diameter.
(Pre Reflow Diameter :∅0.40±0.02)

1.4 Package

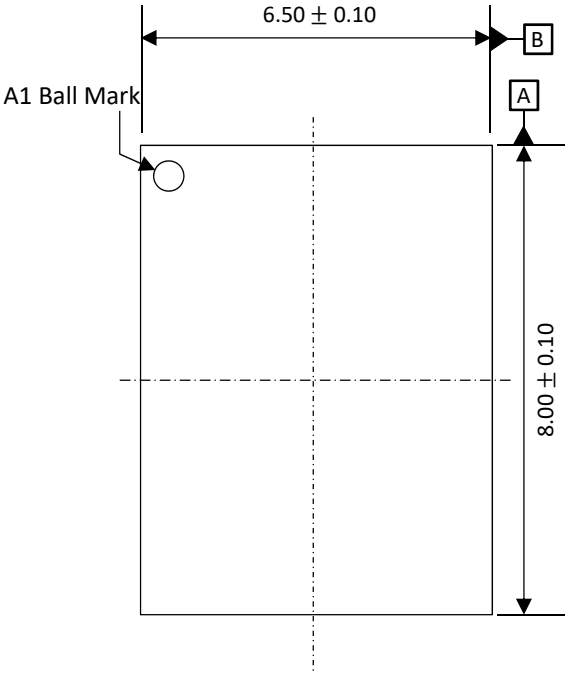
1.4.3 Pin Configuration (48 FBGA 6.5x8mm)

S8F1G08S0B-XxB0

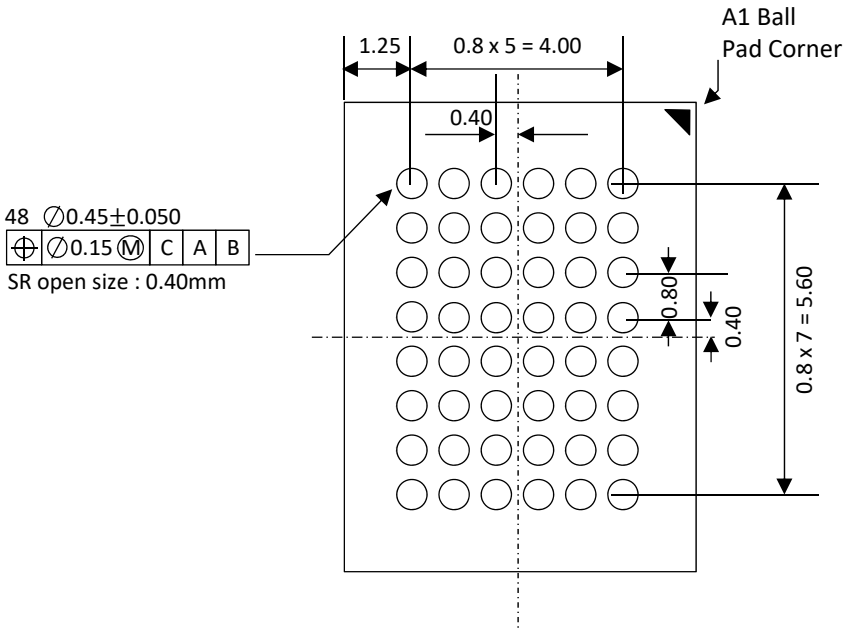


Top View

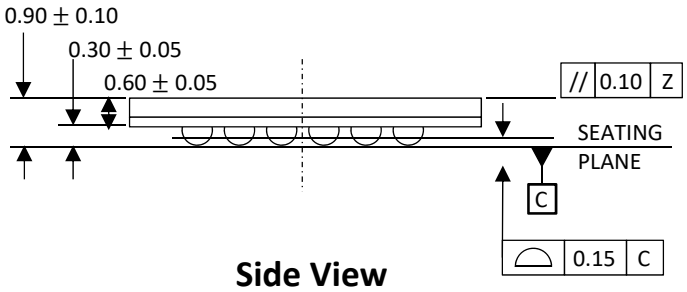
1.4.4 Package Dimensions (48 FBGA 6.5x8mm)



Top View



Bottom View



Side View

1. All Dimensions are in millimeters.
2. Post Reflow Solder Ball Diameter.
(Pre Reflow Diameter :∅0.40±0.02)

1.5 Pin Descriptions

[Table 1] Pin Descriptions

Pin Name	Pin Function
I/O0 ~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{CE}$ control during read operation, refer to 'Page Read' section of device operation.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** V_{CC} is the power supply for device.
VSS	**GROUND**
N/C	**NO CONNECTION**

NOTE :

1) A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2) Connect all Vcc and Vss pins of each device to common power supply outputs. Do not leave Vcc or Vss disconnected.

1.6 Block Diagram

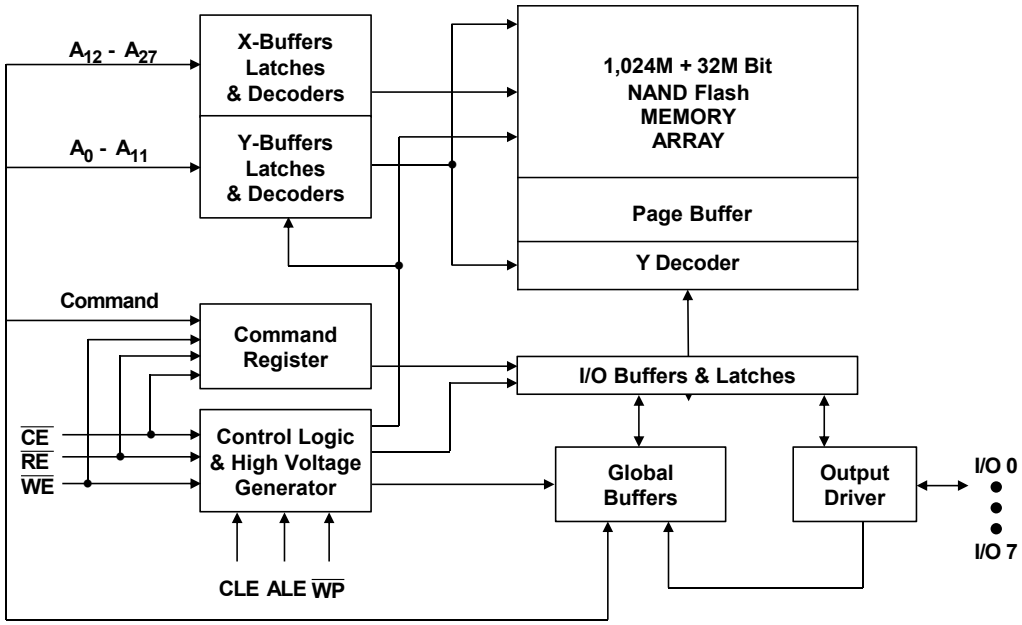


Figure 1. S8F1G08S0B Functional Block Diagram

1.7 Memory Array Organization

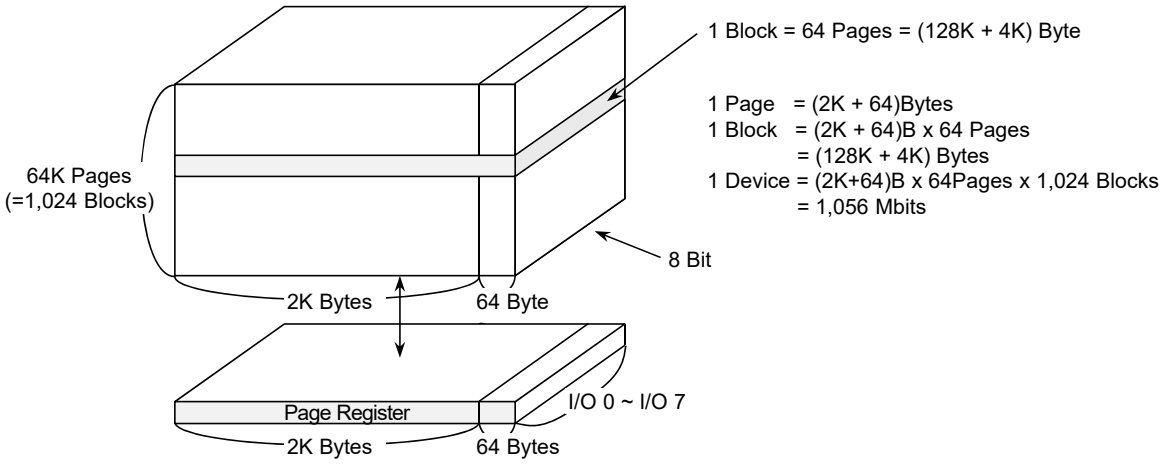


Figure 2. S8F1G08S0B Array Organization

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	

NOTE :

1. *L must be set to "Low"
2. A0 – A11 : Column Address in the page
3. A12 – A17 : Page Address in the block
   A18 – A27 : Block Address
4. The device ignores any additional input of address cycles than required.

2.0 PRODUCT INTRODUCTION

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc. require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 2 defines the specific commands of the S8F1G08S0B.

[Table 2] Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Page Read	00h	30h	
Read for Copy Back	00h	35h	
Cache Read (Start)	31h	-	
Cache Read (End)	3Fh	-	
Read ID	90h	-	
Reset	FFh	-	
Page Program (Start) Cache Program (End)	80h	10h	
Cache Program (Start)	80h	15h	
Cache Read Random	00h	31h	
Page Re-Program	8Bh	10h	
Copy Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input	85h	-	
Random Data Output	05h	E0h	
Read Status Register	70h	-	O

Caution :
Any undefined command inputs are prohibited except for above command set of Table 2.

2.1 Valid Block

[Table 3] The Number of Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1,004	-	1,024	Blocks

NOTE :
1) The device may include invalid blocks when first shipped. Additional invalid blocks may develop while being used.
The number of valid blocks is presented with both cases of invalid blocks considered.
Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks.
Refer to the attached technical notes for a appropriate management of invalid blocks.
2) The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.
3) Minimum 1,004 valid blocks are guaranteed for each contiguous 128Mb memory space.

2.2 Absolute Maximum DC Ratings

[Table 4] Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C
Voltage on any pin relative to V_{SS}		V_{CC}	-0.6 to + 4.6	V
		V_{IN}	-0.6 to + 4.6	
		$V_{I/O}$	-0.6 to VCC + 0.3 (<4.6V)	
Temperature Under Bias		T_{BIAS}	-50 to +125	°C
Storage Temperature		T_{STG}	-65 to +150	°C
Short Circuit Current		I_{OS}	5	mA

NOTE :
1) Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.3 Recommended Operating Conditions

[Table 5] Recommended Operating Conditions

Parameter	Symbol	S8F1G08S0B			Unit
		Min	Typ.	Max	
Power Supply Voltage	V_{CC}	1.7	1.8	1.95	V
Ground Supply Voltage	V_{SS}	0	0	0	V

NOTE :
Voltage reference to GND.

2.4 DC Operating Characteristics

[Table 6] DC & Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Access Operation Current	I_{CC1}	tRC=45ns, $\overline{CE}$ =V_{IL}, I_{OUT}=0mA	-	15	30	mA
Program Operation Current	I_{CC2}	-				
Erase Operation Current	I_{CC3}	-				
Stand-by Current (TTL)	I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	
Stand-by Current (CMOS)	I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}(max)	-	-	±10	
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}(max)	-	-	±10	
Input High Voltage	V_{IH}1)	-	0.8xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage, All inputs	V_{IL}1)	-	-0.3	-	0.2xV_{CC}	
Output High Voltage Level	V_{OH}	I_{OH}=100µA	V_{CC} - 0.1	-	-	
Output Low Voltage Level	V_{OL}	I_{OL}=100µA	-	-	0.1	
Output Low Current (R/$\overline{B}$)	I_{OL}(R/$\overline{B}$)	V_{OL}=0.1V	3	4	-	mA
V_{CC} Supply Voltage (Erase and Program Lockout)	V_{LKO}	-	-	1.1	-	V

NOTE :
1) Typical value is measured at V_{CC}=1.8V, T_A=25°C. Not 100% tested.

2.5 Input / Output Capacitance (T_A=25°C, V_{CC}=1.8V, f=1.0Mhz)

[Table 7] Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE :
Capacitance is sampled and not 100% tested.

2.6 AC Test Condition

[Table 8] AC Test Condition

Parameter	S8F1G08S0B
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC}/2
Output Load	1 TTL GATE and C_L=30pF

2.7 Read / Program / Erase Characteristics

[Table 9] NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	tR	-	-	25	µs
Program Time	tPROG	-	300	700	µs
Cache Read busy time	tCBSYR	-	3	tR	µs
Cache Program short busy time	tCBSYW	-	5	tPROG	µs
Number of Partial Program Cycles	Nop	-	-	4	cycle
Block Erase Time	tBERS	-	3	10	ms

NOTE :
1) Typical Program time is defined as the time within which more than 50% of the whole pages are programmed at Vcc of 1.8V and 25°C.
2) Typical value is measured at V_{CC}=1.8V, T_A=25°C. Not 100% tested.

2.8 AC Timing Parameters Table

[Table 10] AC Timing Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t_{CLS}	25	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{CE}$ Setup Time	t_{CS}	35	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}[1)]	25	-	ns
ALE Setup Time	t_{ALS}	25	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns
Address to Data Loading Time	t_{ADL}	100	-	ns
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	25	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	45	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	30	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	50	ns
$\overline{CE}$ High to ALE or CLE Don't Care	t_{CSD}	10	-	ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15	-	ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	-	-	ns
$\overline{CE}$ High to Output Hold	t_{COH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low for Random Data Out	t_{WHR2}	200	-	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	t_{CR}	10	-	ns
Write Protection Time	t_{WW}	100	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	5/10/500[3)]	μs

NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
2) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5μs.

3.0 NAND FLASH TECHNICAL NOTES

3.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Netsol. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

3.2 Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Netsol makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the first byte of spare area on the 1st or 2nd page. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). The first block, whose address is 00h, is guaranteed to be a valid block at the time of shipment.

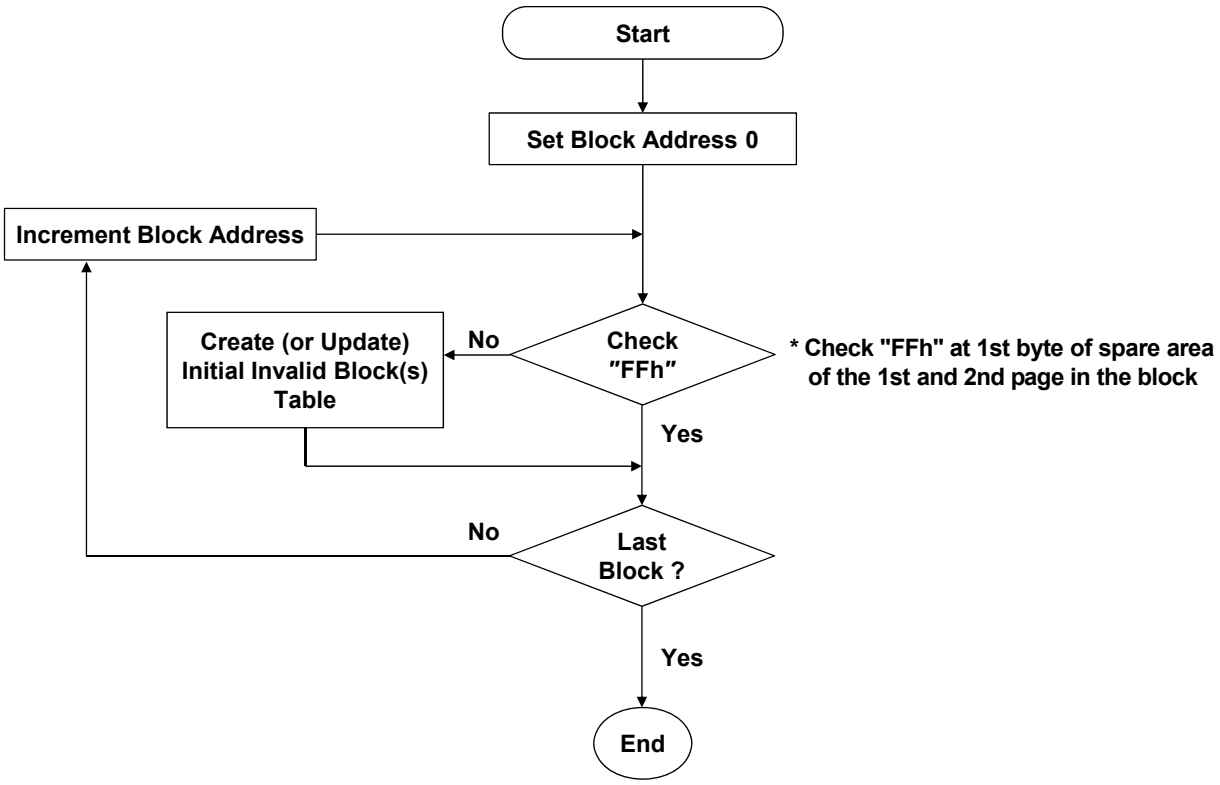


Figure 3. Flow Chart to Create Initial Invalid Block Table

3.3 Error in Write or Read Operation

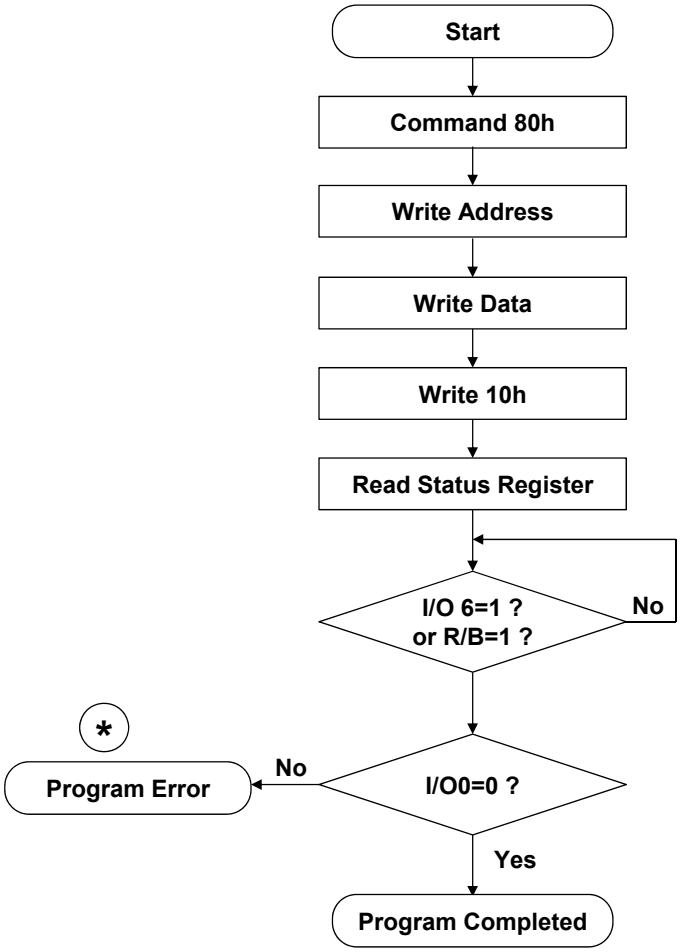
Within its life time, additional invalid blocks may develop with NAND Flash memory. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.

[Table 11] Failure Cases

Failure Mode		Detection and Countermeasure Sequence
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

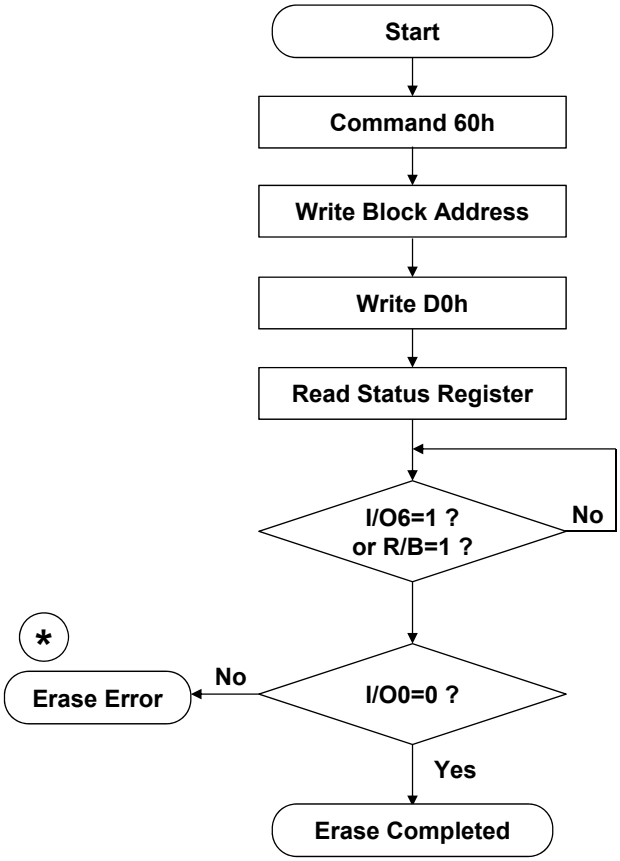
NOTE :
1) Error Correcting Code → Hamming Code etc. (Example : 1bit Correction & 2bits detection)

Program Flow Chart



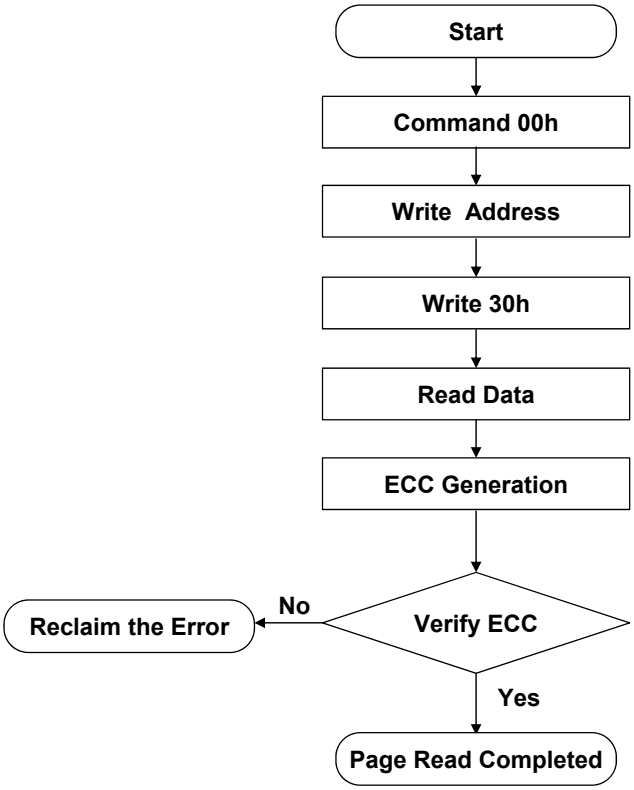
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

Erase Flow Chart

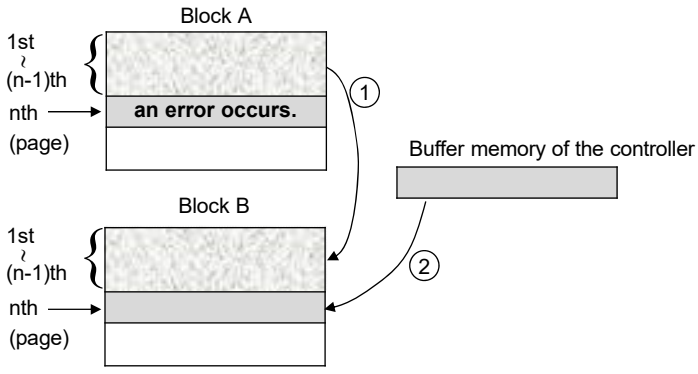


(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Read Flow Chart



Block Replacement



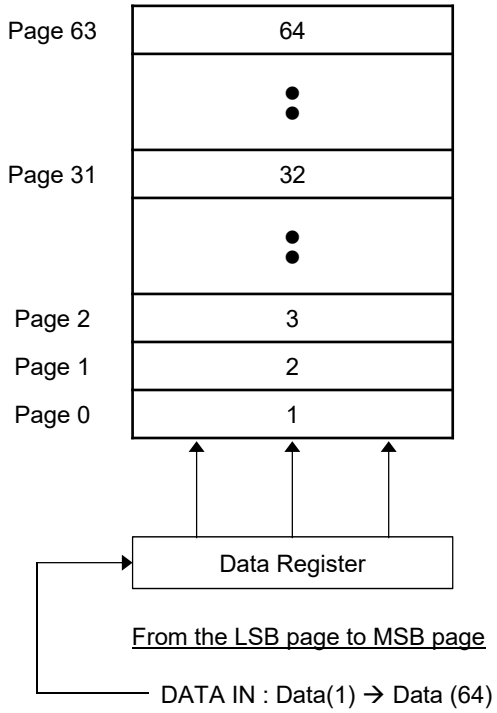
1. When an error happens in the nth page of the Block 'A' during erase or program operation.
2. Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
3. Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
4. Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

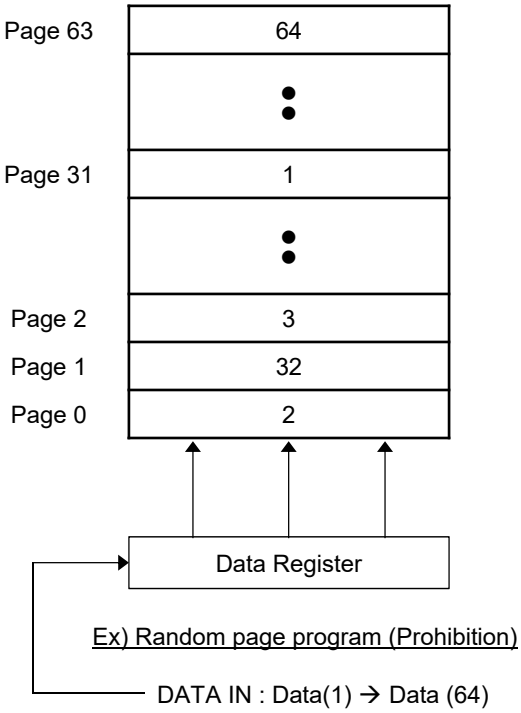
Figure 4. Flow Chart

3.4 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB(least significant bit) page of the block to the MSB(most significant bit) pages of the block. Random page address programming is prohibited.

In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.





3.5 System Interface Using $\overline{CE}$ don't-care

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

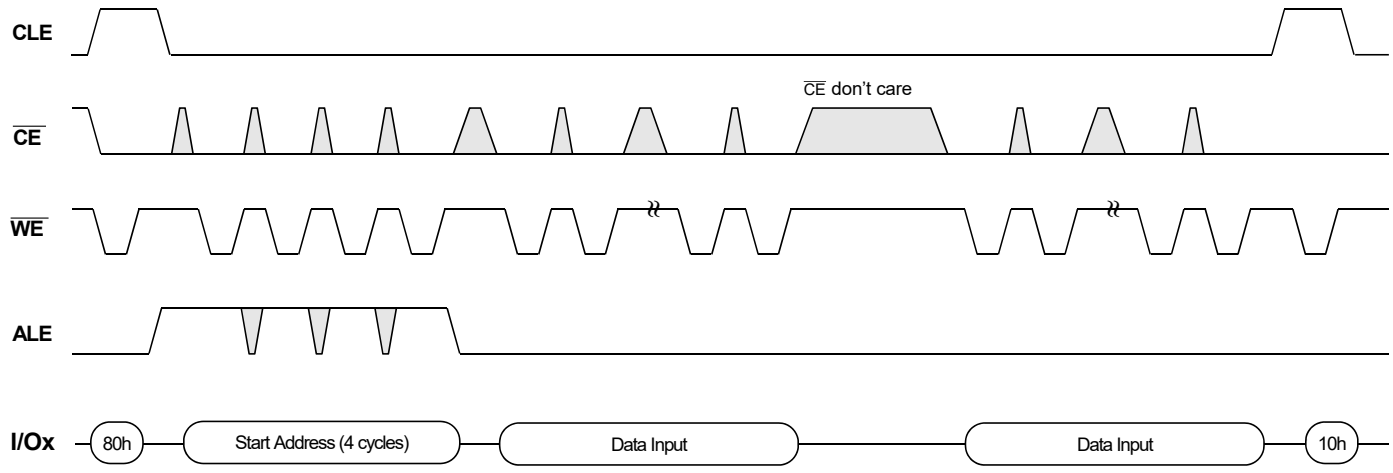


Figure 5. Program Operation with $\overline{CE}$ don't care.

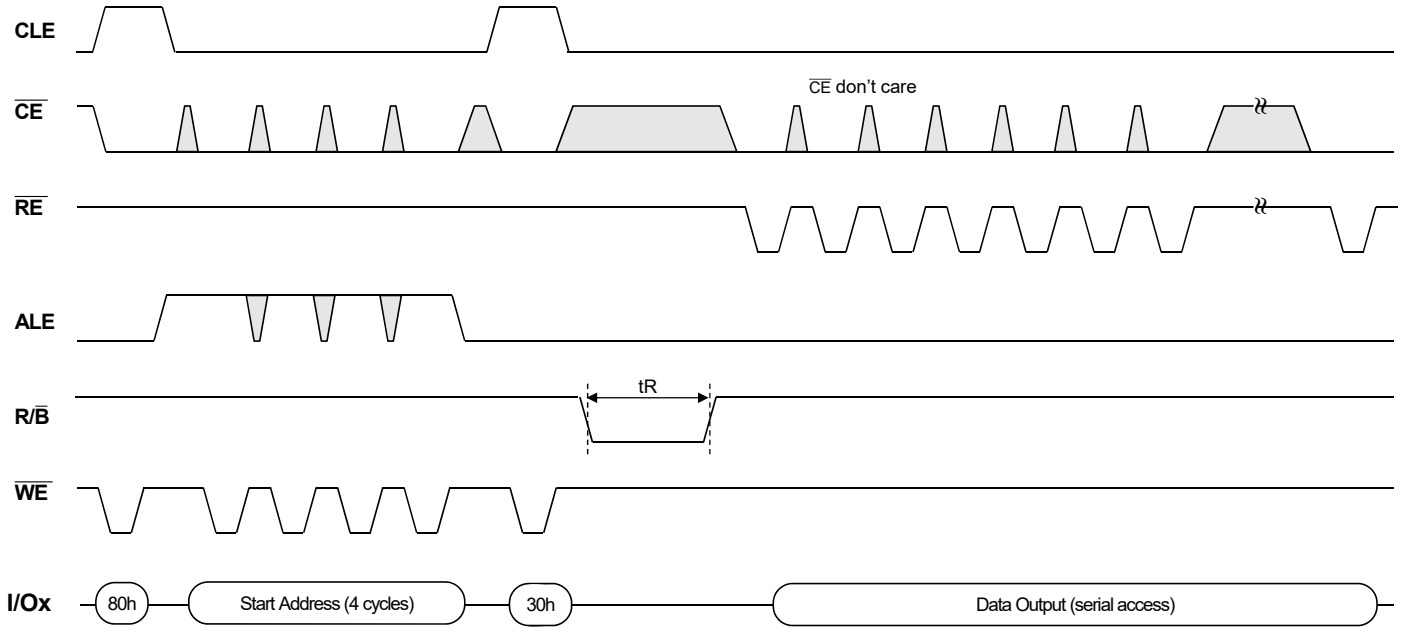


Figure 6. Read Operation with $\overline{CE}$ don't care.

4.0 DEVICE OPERATION

4.1 Power Up Sequence and Data Protection

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power down.
A recovery time of minimum 100us is required before internal circuit gets ready for any command sequences as shown in Figure 7. The two command sequence for program / erase provides additional software protection.

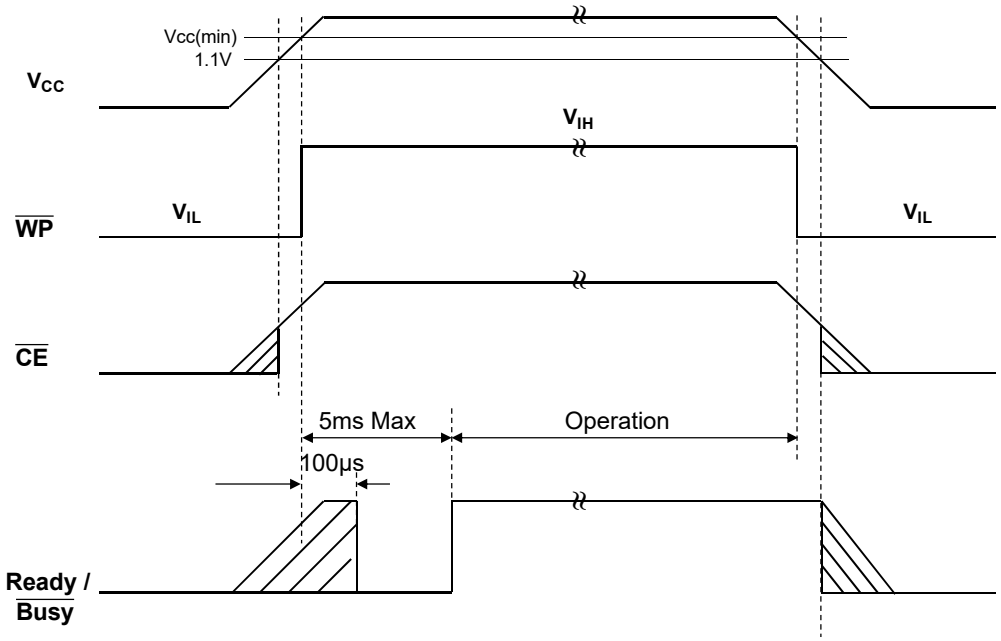


Figure 7. AC Waveforms for Power Transition

4.2 Mode Selection

[Table 12] Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(4cycles)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(4cycles)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output (on going)	
L	L	L	H[3)]	H[3)]	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X[1)]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}[2)]	Stand-by	

NOTE :
1) X can be V_{IL} or V_{IH}.
2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
3) $\overline{WE}$ and $\overline{RE}$ during Read Busy must be kept on high to prevent unplanned command/address/data input or to prevent unintended data out.
In this time, only Reset, Read Status and multi Plane Read Status can be input to the device.

4.3 Page Read Operation

Page read is initiated by writing 00h-30h to the command register along with four address cycles. After initial power up, 00h command is latched. Therefore only four address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 25μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 45ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

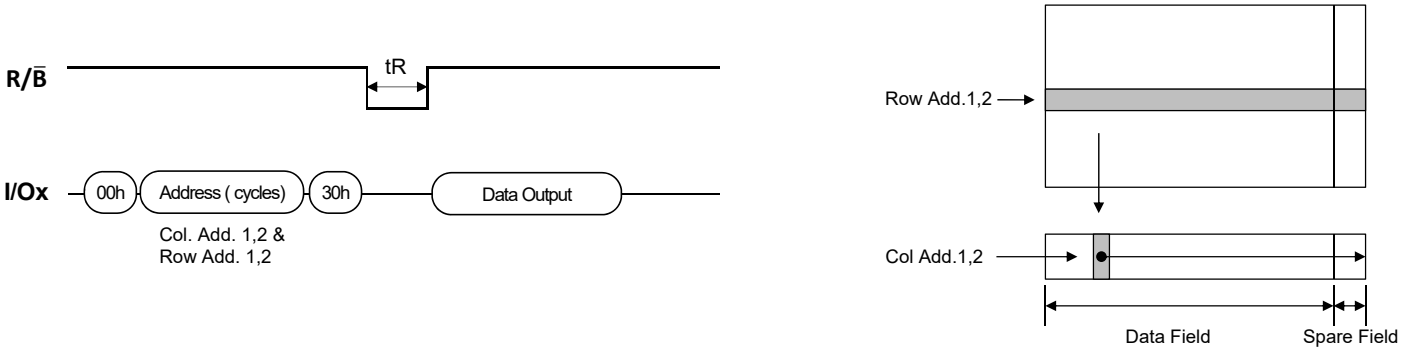


Figure 8. Page Read Sequence

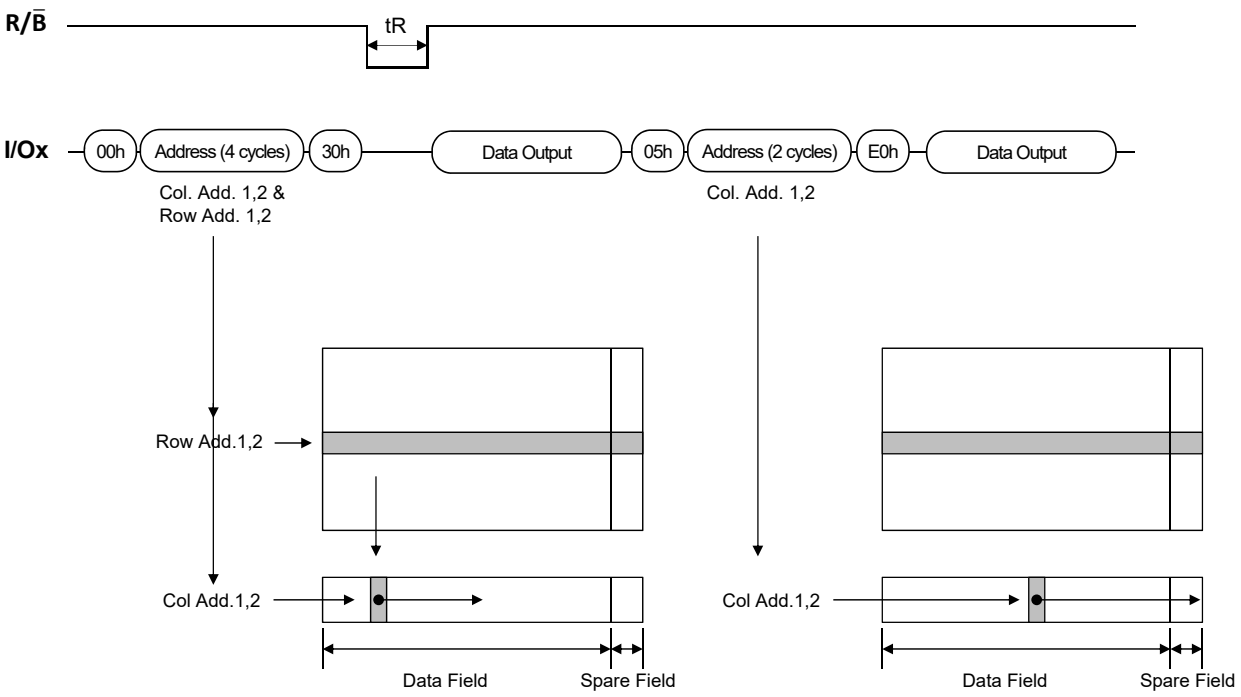


Figure 9. Page Read with Random Data Output Sequence

4.4 Cache Read (available only within a block)

Page command, as defined in 4.3, shall be issued prior to the initial sequential or random Cache Read command in a Cache Read sequence. A Cache Read Sequential or Cache Read Random command shall be issued prior to a Cache Read End (3Fh) command being issued.

The Cache Read function may be issued after the Read function is complete (the status bit SR[I/O 6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Cache Read function is issued, SR[I/O 6] is cleared to zero (busy). After the operation is begun SR[I/O 6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache Read function. Issuing an additional Cache Read function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[I/O 6] is set to one (ready). When the 31h and 3Fh commands are issued, SR[I/O 6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a sequential Cache Read (31h) command after the last page of the device is read. SR[I/O 6] conveys whether the next selected page can be read from the page register. During Cache Read operation the only acceptable commands are Read Status, Random Data Output and Reset.

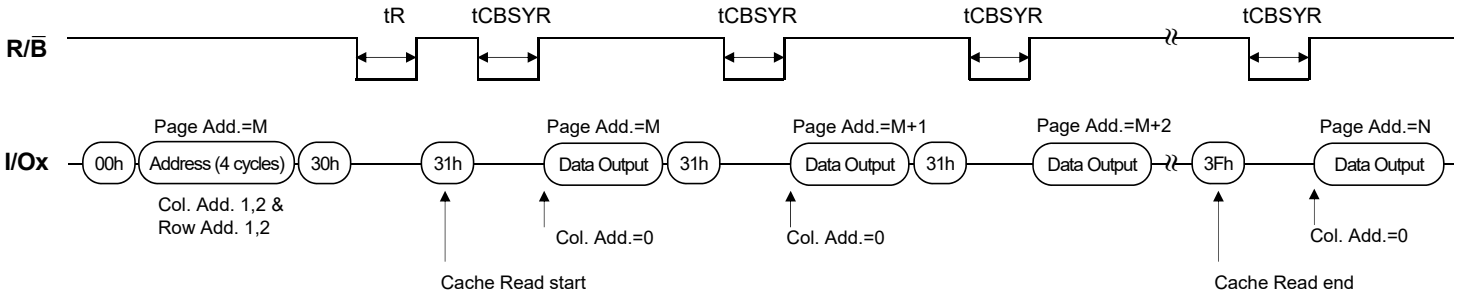


Figure 10. Sequential Cache Read Sequence

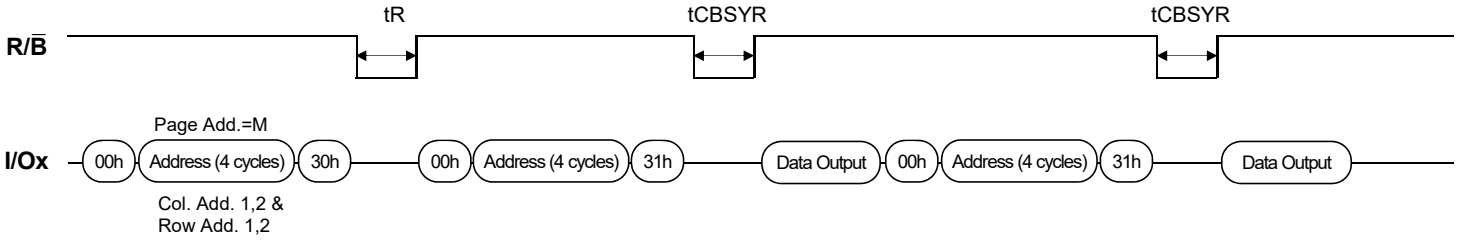


Figure 11. Random Cache Read Sequence

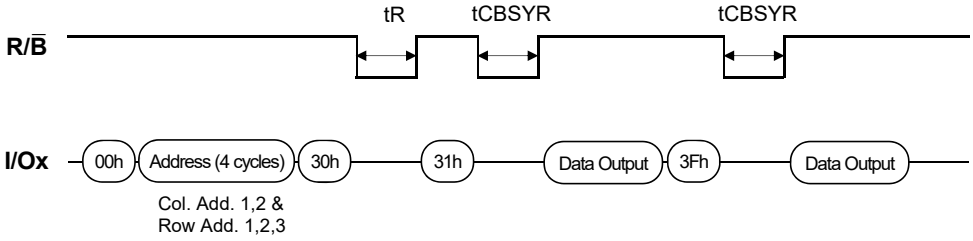


Figure 12. End of Cache Read Sequence

4.5 Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased. , but it does allow multiple partial page programming of a byte or consecutive bytes up to 2,112 byte, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 for a single page. The addressing may be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the four cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the status bit SR[I/O 6]. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit SR[I/O 0] may be checked(Figure 13 and 14). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

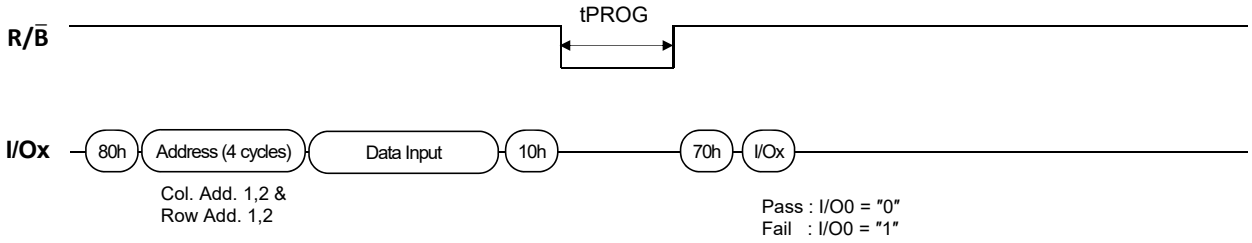


Figure 13. Page Program Sequence

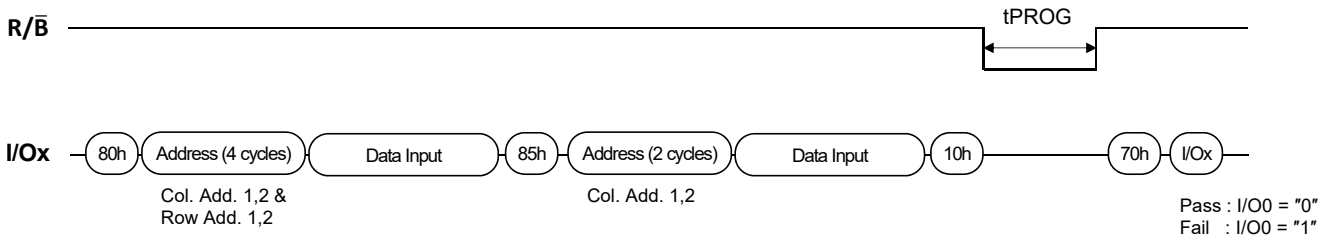


Figure 14. Program Operation with Random Data Input Sequence

4.6 Page Re-Program Operation

Page program may result in a fail, which can be detected by Read Status Register. In this event, the device implements the innovative feature of “page re-program”. This command allows reprogramming of the same pattern of the (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the four cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the page, the program confirm can be issued (10h) without any data input cycle.

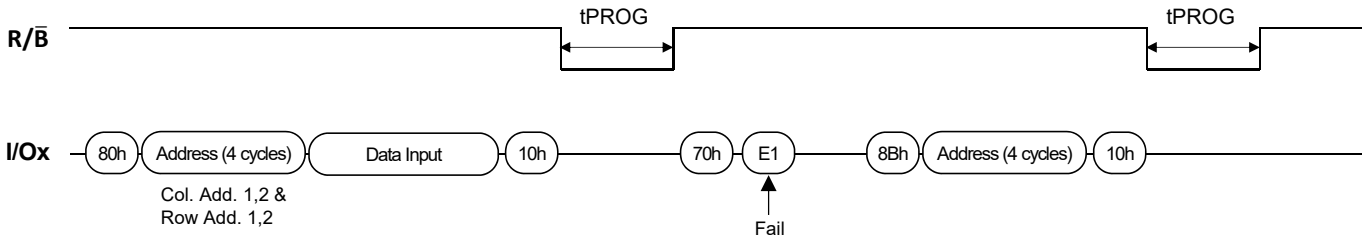


Figure 15. Page Re-Program Sequence

Meanwhile, if the pattern bound for target page is different from that of previous page, data in cycles can be issued before program confirm “10h”

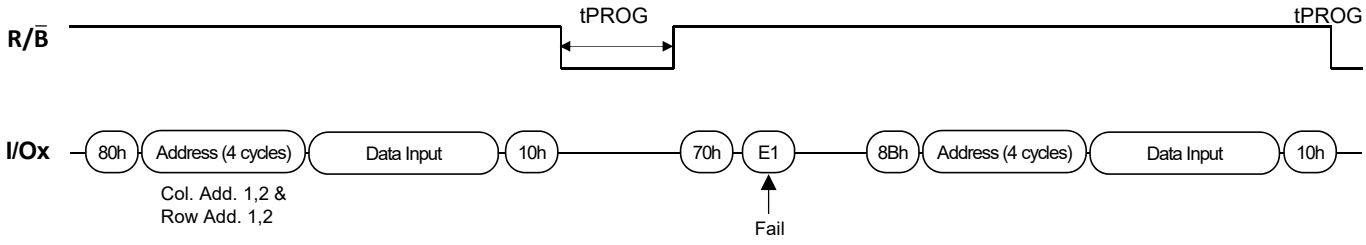


Figure 16. Page Re-Program with data manipulation Sequence

4.7 Cache Program Operation (available only within a block)

The cache program allows data insertion for one page while program of another page is under execution. Cache program is available only within a block. After the serial data input command (80h) is loaded to the command register, followed by 4 cycles of address, a full or partial page of data is latched into the cache register. Once the cache write command(15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).

The busy time following the first sequence 80h-15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model.

In case of any subsequent sequence 80h-15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (tCBSYW).

Read Status commands (70h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. More in detail:

a) The status bit SR[I/O 6] indicates when the cache register is ready to accept new data.
b) The status bit SR[I/O 5] indicates when the cell programming of the current data register is complete
c) The status bit SR[I/O 1] returns the pass/fail status for the previous page when the status bit SR[I/O 6] equals a “1” (ready state).
d) The status bit SR[I/O 0] returns the pass/fail status for the current page when the status bit SR[I/O 5] equals a “1” (ready state).
SR[I/O 1] may be read together with SR[I/O 0].

If the system monitors the progress of the operation only with R/$\overline{B}$, the last page of the target program sequence must be programmed with Page Program Confirm command(10h). If the Cache Program command(15h) is used instead, the status bit SR[I/O 5] must be polled to find out if the last programming is finished before starting any other operation.

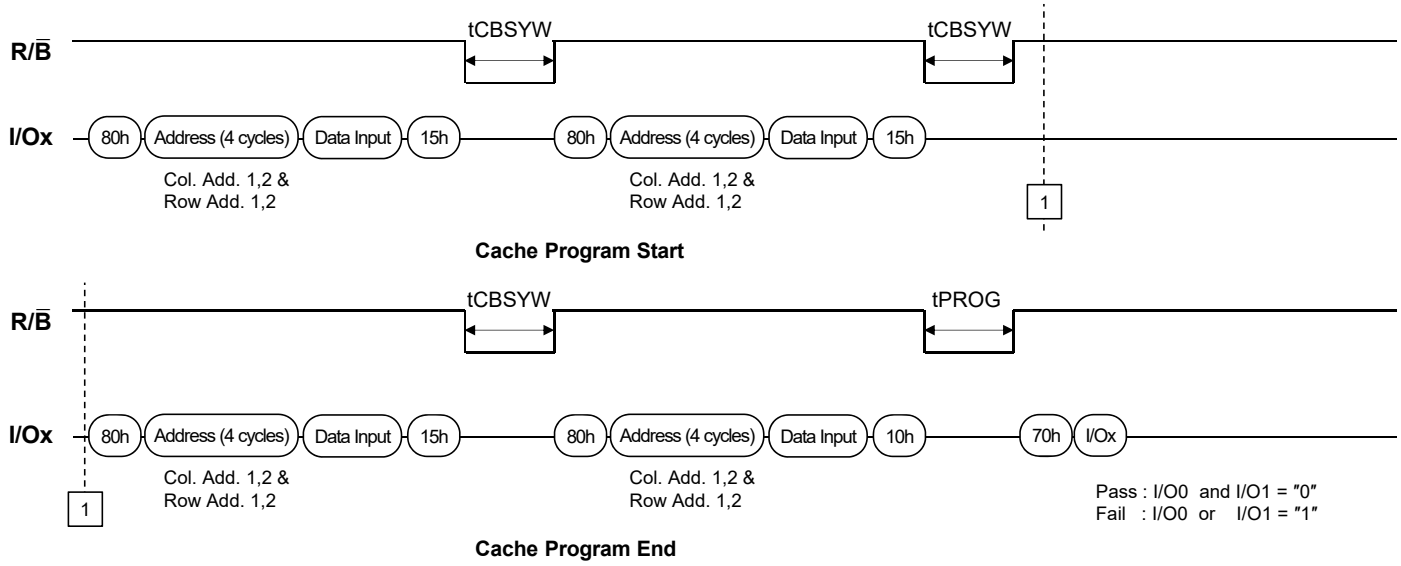


Figure 17. Cache Program Operation

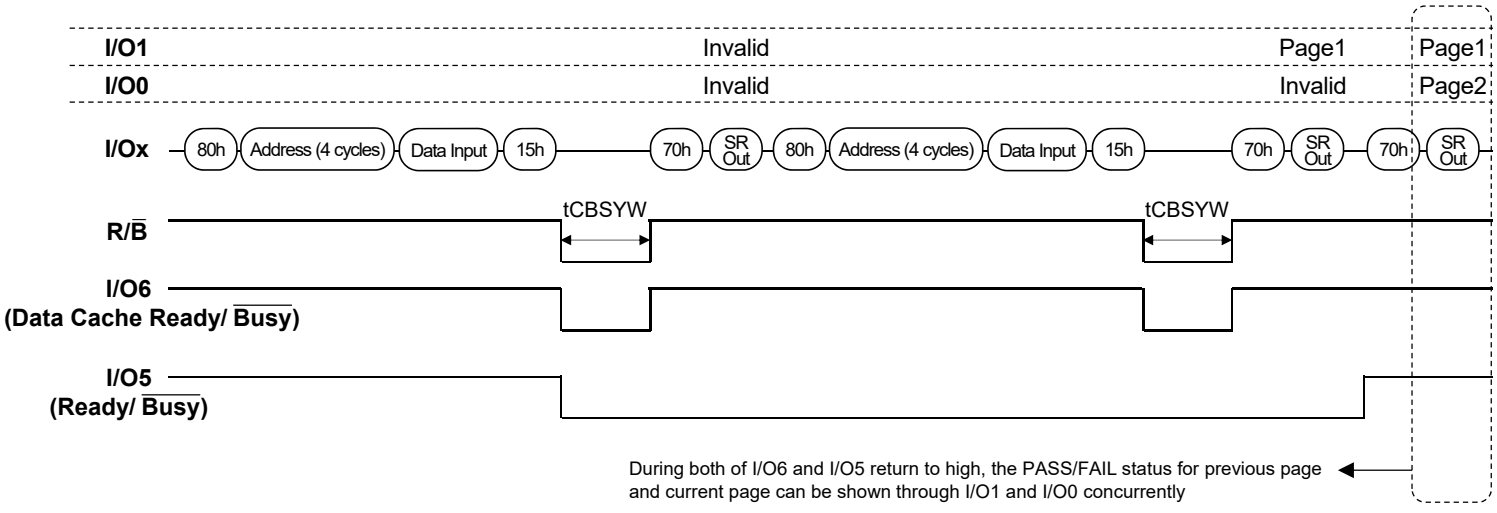


Figure 18. Cache Program PASS/FAIL Status Check

4.8 Copy-Back Program Operation

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or SR[I/O 6]. When the Copy-Back Program is complete, the Write Status Bit SR[I/O 0] may be checked(Figure 19 and 2-). The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h).

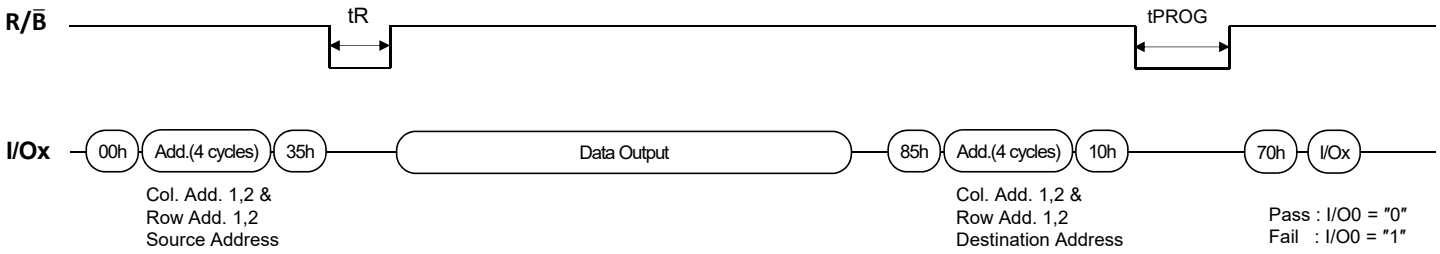


Figure 19. Copy-Back Read with Optional Data Readout

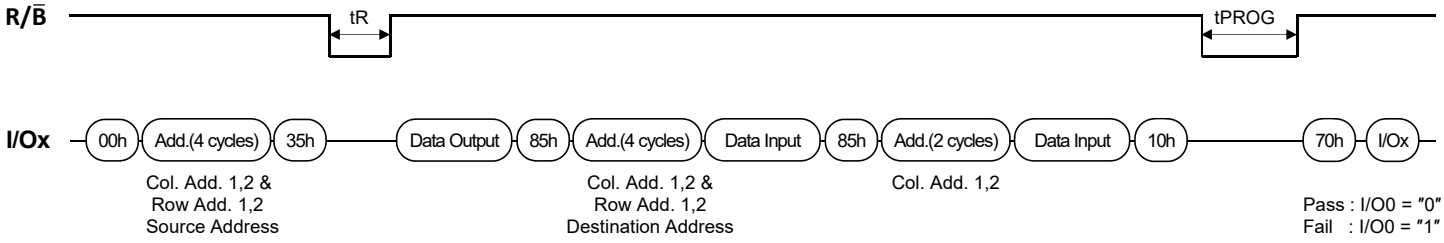


Figure 20. Copy-Back Program with Random Data Input Sequence

4.9 Block Erase Operation

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A_{18} to A_{27} is valid while A_{12} to A_{17} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify.

When the erase operation is completed, the Write Status Bit SR[I/O 0] may be checked.

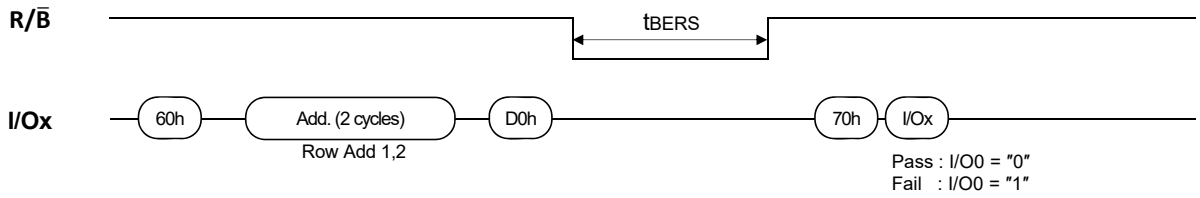


Figure 21. Block Erase Sequence

4.10 Read Status Register

The device contains a Status Register which may be read to find out whether read program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/ O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple mem- ory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 13 for specific Status Register definitions. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

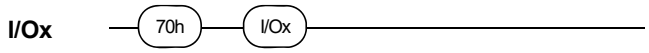


Figure 22. Read Status Register Sequence

[Table 13] Status Register Definition for 70h Command

SR bit	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
I/O 0	Pass / Fail	Pass / Fail	N/A	N/A	Pass / Fail (N)	N page, Pass : "0" Fail : "1"
I/O 1	N/A	N/A	N/A	N/A	Pass / Fail (N-1)	N-1 page, Pass : "0" Fail : "1"
I/O 2	N/A	N/A	N/A	N/A	N/A	Don't -cared
I/O 3	N/A	N/A	N/A	N/A	N/A	Don't -cared
I/O 4	N/A	N/A	N/A	N/A	N/A	Don't -cared
I/O 5	Ready/Busy	Ready/Busy	Ready/Busy	P/E/R controller bit	Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data Cache Ready/Busy Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	N/A	Write Protect	Protected : "0" Not Protected : "1"

Notes:
1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to one.
2. I/O1: This bit is only valid for cache program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache program sequence. When Cache program is not supported, this bit is not used.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.
4. I/O6: If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the operation is complete.

4.11 Read ID

4.11.1 00h Address ID Definition

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code(ADh), and the device code and 3rd, 4th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 23 shows the operation sequence.

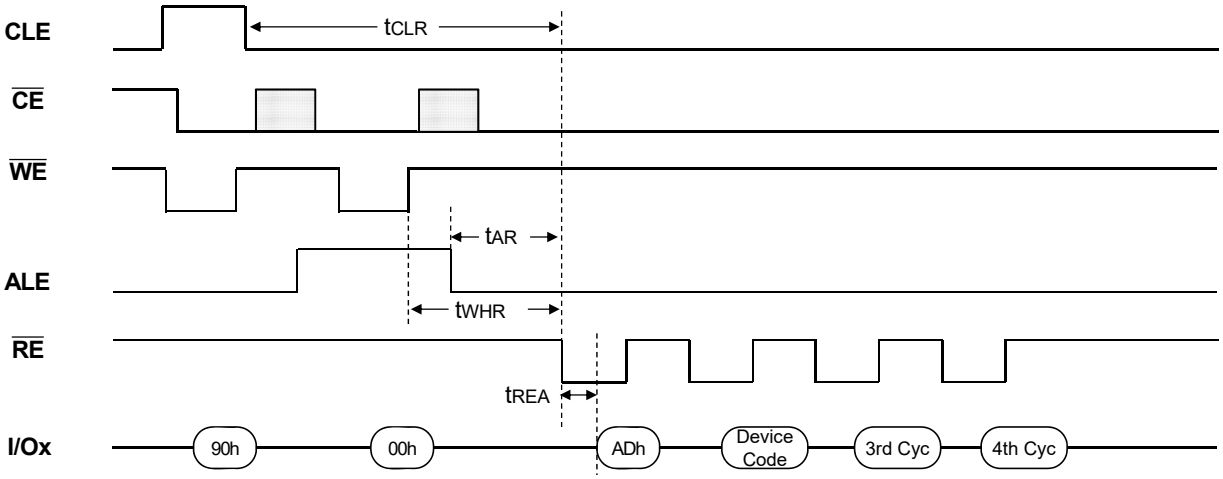


Figure 23. Read ID Sequence

4.11.2 Read Parameter Page

The device supports the ONFI Read Parameter Page operation, which enables the host processor to recognize the NAND Flash chip's organization, features, timings and other behavioral parameters automatically. Read Parameter Page operation is initiated by writing ECh to the command register, followed by an address input of 00h. The host may monitor the R/$\overline{B}$ pin or wait for the maximum data transfer time (tR) before reading the Parameter Page data. The command register remains in Parameter Page mode until further commands are issued to it. If the Status Register is read to determine when the data is ready, the Read Command (00h) must be issued before starting read cycles. Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

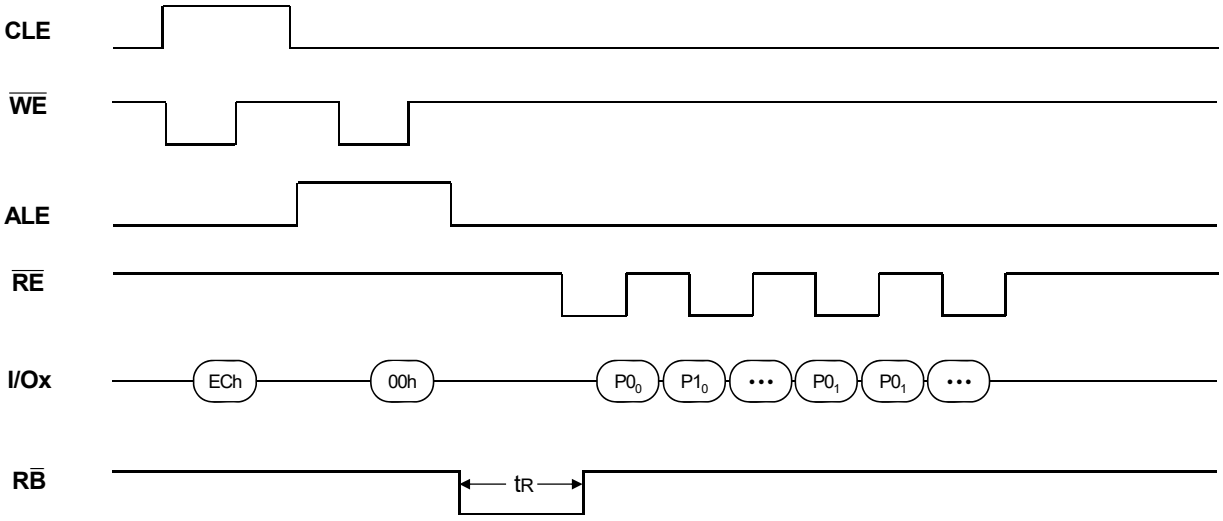


Figure 24. Read Parameter Page Sequence

4.11.3 Parameter Page Data Structure Definition

Table 19 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page.
For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

[Table 14] Parameter page data

Byte	O/M	Description	Values
	Revision information and features block		
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	14h, 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Cache Read commands 0 1 = supports Page Cache Program command	33h, 00h
10-31		Reserved (0)	00h
	Manufacturer information block		
32-43	M	Device manufacturer (12 ASCII characters)	48h, 59h, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	48h, 32h, 37h, 53h, 31h, 47h, 38h, 46h, 32h, 43h, 46h,52h, 2Dh, 42h, 43h, 20h, 20h, 20h, 20h, 20h
64	M	JEDEC manufacturer ID	ADh
65-66	O	Date code	00h
67-79		Reserved (0)	00h
	Memory organization block		
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	40h, 00h
86-89	M	Number of data bytes per partial page	00h, 00h, 00h, 00h
90-91	M	Number of spare bytes per partial page	00h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	00h, 04h, 00h, 00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	22h

Byte	O/M	Description	Values
	Memory organization block		
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	20h, 00h
105-106	M	Block endurance	05h, 04h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	05h, 04h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	04h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	00h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00h
115-127		Reserved (0)	00h
	Electrical parameters block		
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	03h, 00h
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0	03h, 00h
133-134	M	t_{PROG} Maximum page program time (µs)	BCh, 02h
135-136	M	t_{BERS} Maximum block erase time (µs)	10h, 27h
137-138	M	t_R Maximum page read time (µs)	19h, 00h
139-140	M	t_{CCS} Minimum change column set up time (µs)	3Ch, 00h
141-163		Reserved (0)	00h
	Vendor block		
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
254-255			
	Redundant Parameter Pages		
256-511	M	Value of bytes 0-255	Repeat values of byte 0~255
512-767	M	Value of bytes 0-255	Repeat values of byte 0~255
768+	O	Additional redundant parameter pages	FFh

Note : “O” stands for Optional, “M” for Mandatory

4.11.4 00h Address ID Cycle

[Table 15] 00h Address ID cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle
S8F1G08S0B	ADh	A1h	80h	15h

[Table 16] 00 Address ID Definition Table

	Description
1st Byte	Manufacturer Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc
4th Byte	Page Size, Spare Size, Block Size, Organization, Serial Access Minimum

[Table 17] 3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Program Between multiple chips	Not Support		0						
	Support		1						
Cache Program	Not Support	0							
	Support	1							

[Table 18] 4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (without spare area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Spare Area Size (byte/512bytes)	8						0		
	16						1		
Block Size (without spare area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Organization	X8		0						
	X16		1						
Serial Access Minimum	45ns	0				0			
	25ns	0				1			
	Reserved	1				0			
	Reserved	1				1			

4.12 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 24 shows the operation sequence

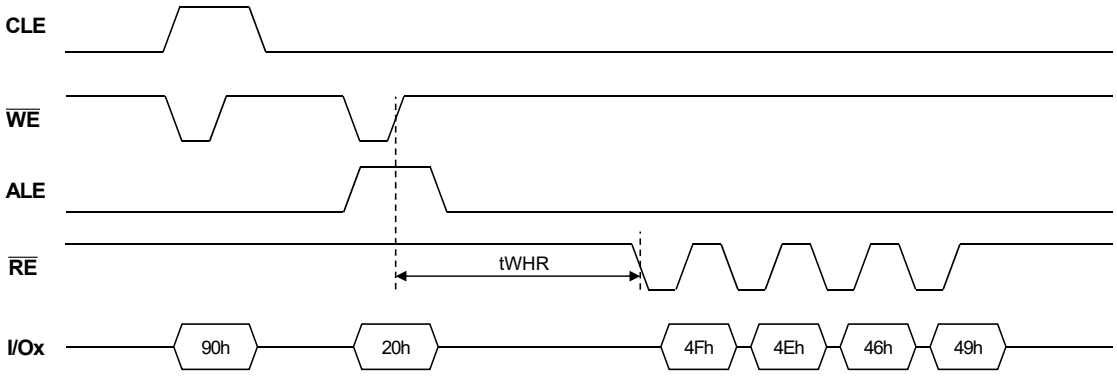


Figure 25. Read ONFI Signature Timing

4.13 Reset Operation

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin changes to low for tRST after the Reset command is written. Refer to Figure 26 below

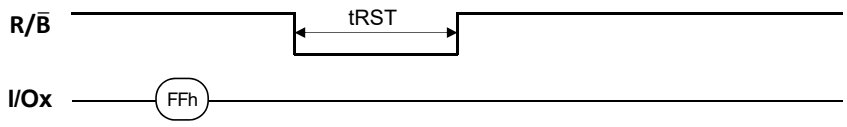


Figure 26. Reset Sequence

[Table 19] Device Status

	After Power-up	After Reset
Operation mode	00h Command is latched	Waiting for next command

4.14 Ready/$\overline{\text{Busy}}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy), an appropriate value can be obtained with the following reference chart(.Figure 27). Its value can be determined by the following guidance.

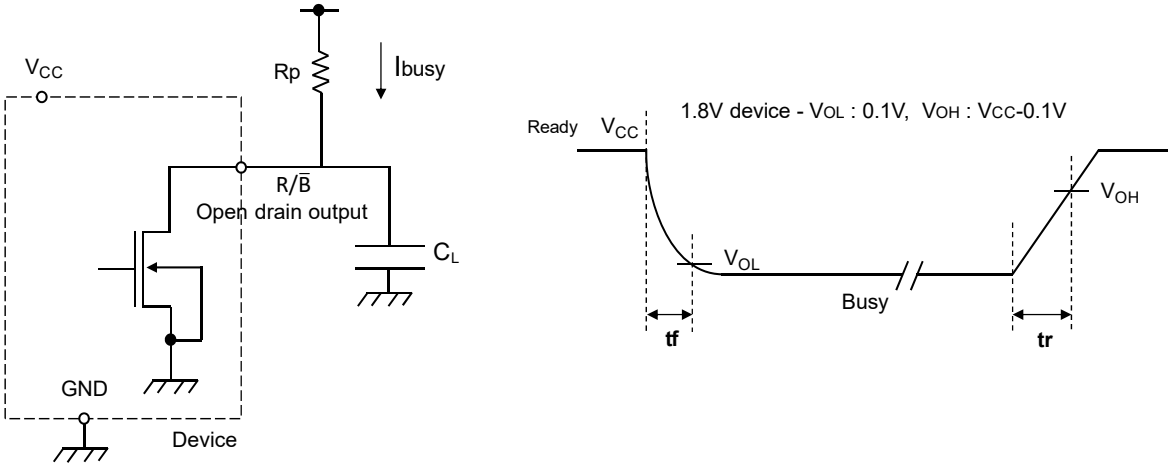
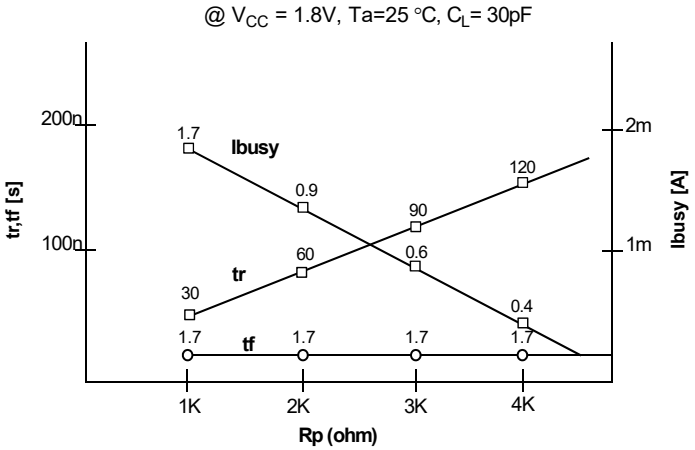


Figure 27. Rp vs tr, tf & Rp vs Ibusy



Rp value guidance

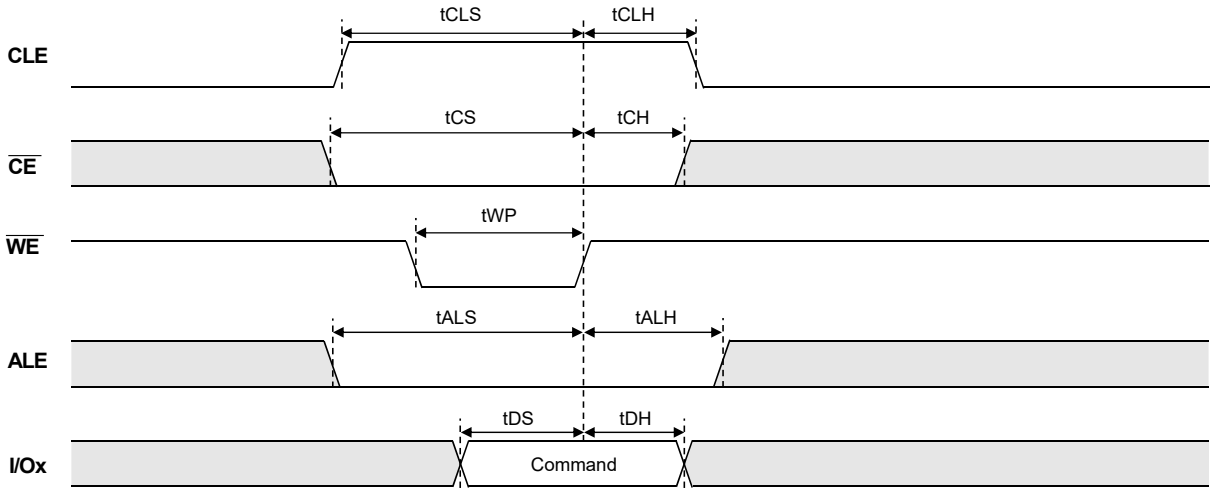
$$Rp(min, 1.8V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

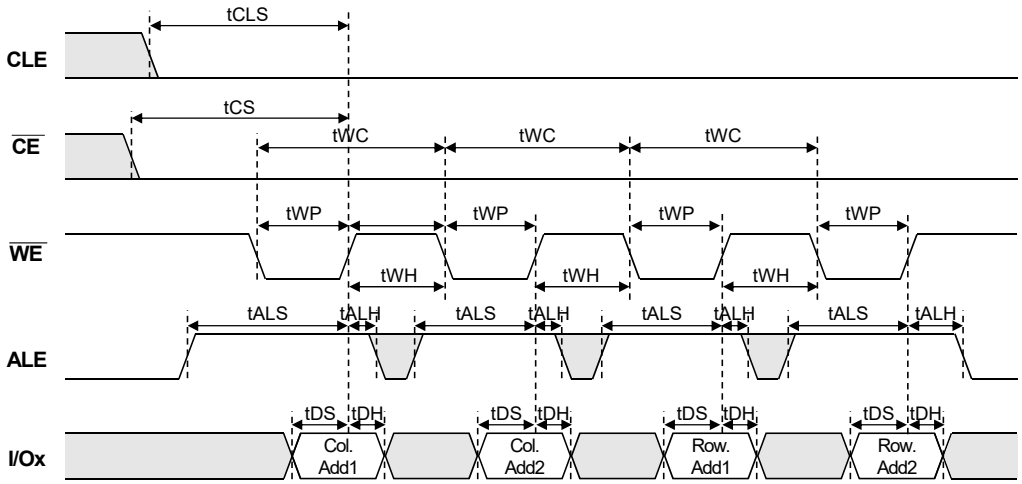
5.0 TIMING DIAGRAM

5.1 General Timing

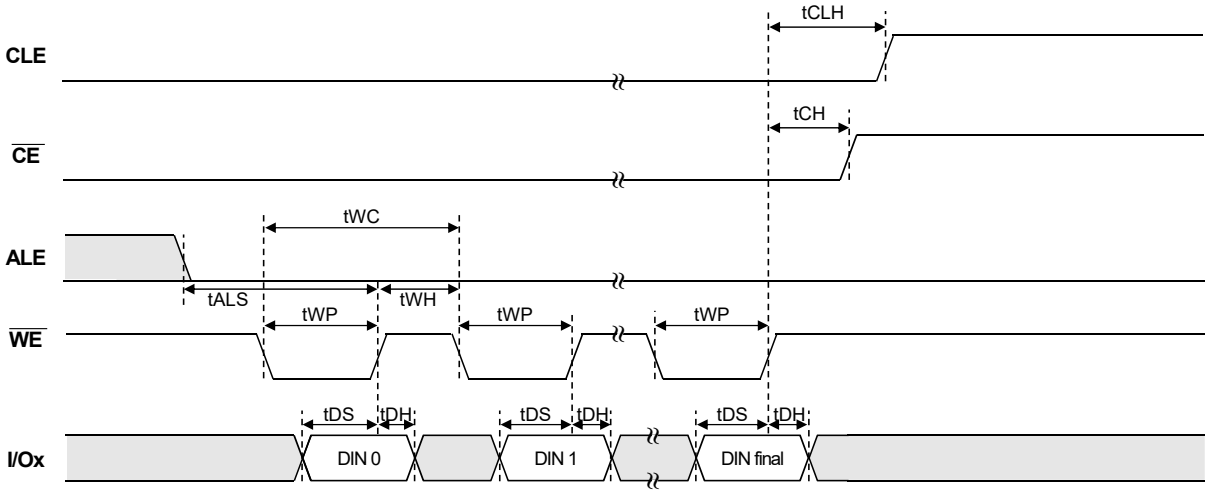
5.1.1 Command Latch Cycle



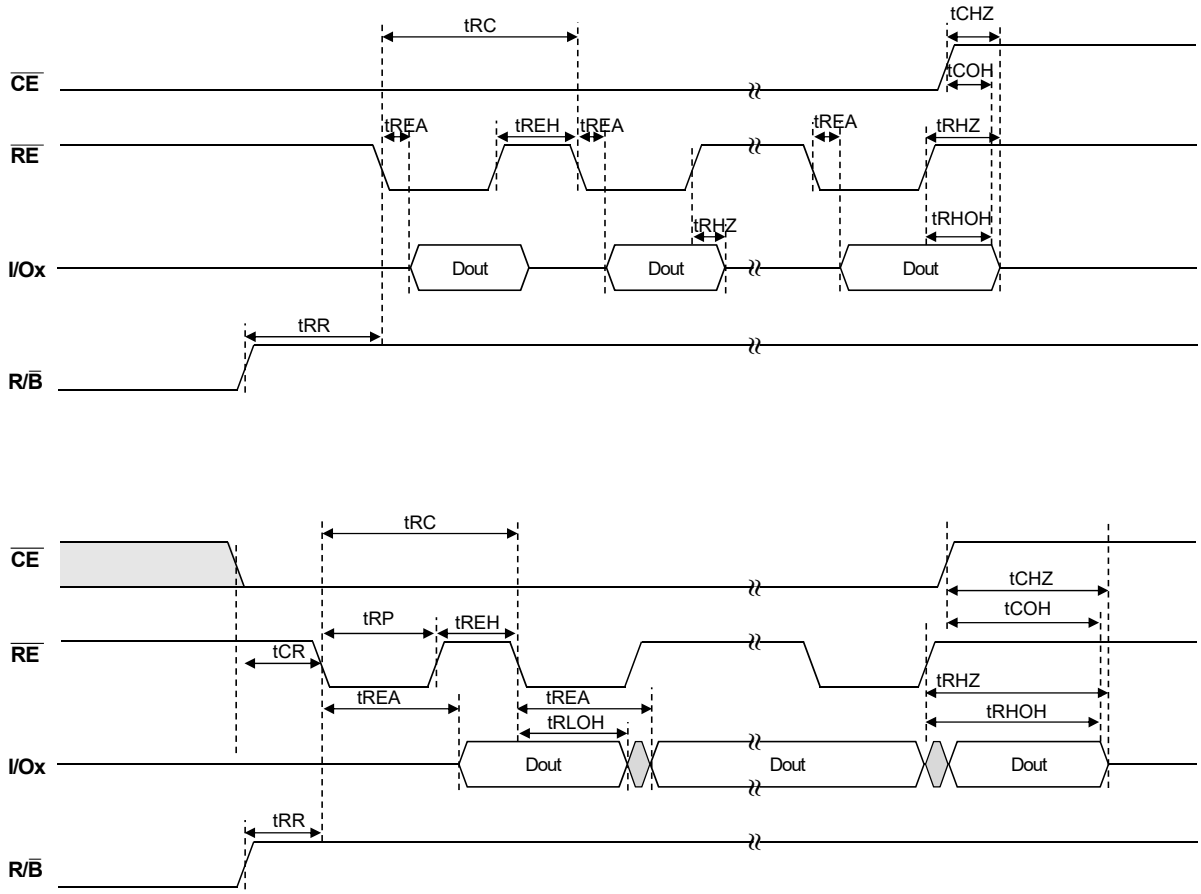
5.1.2 Address Latch Cycle



5.1.3 Input Data Latch Cycle

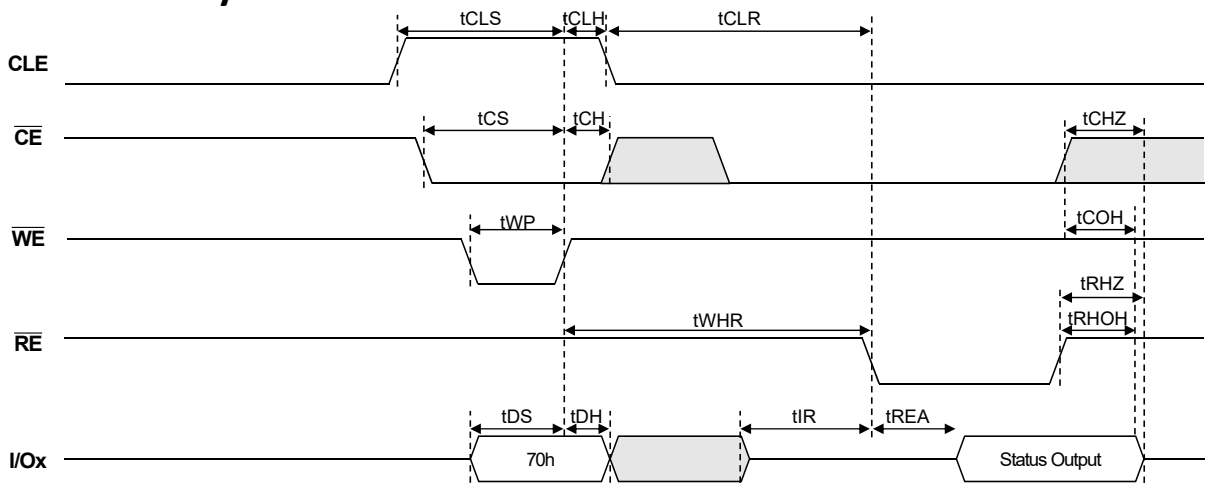


5.1.4 Serial Access Cycle after Read

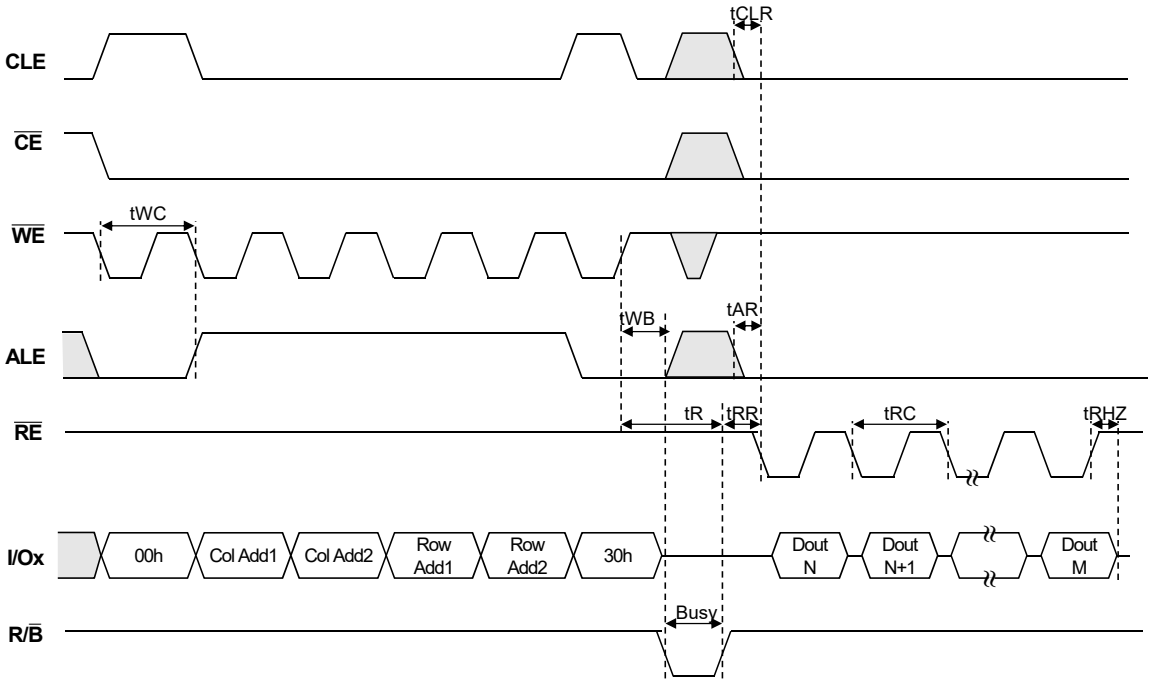


NOTE :
1)Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.(tCHZ, tRHZ)
2) tRHOH starts to be valid when frequency is lower than 33Mhz.
3) tRLOH is valid when frequency is higher than 33MHz

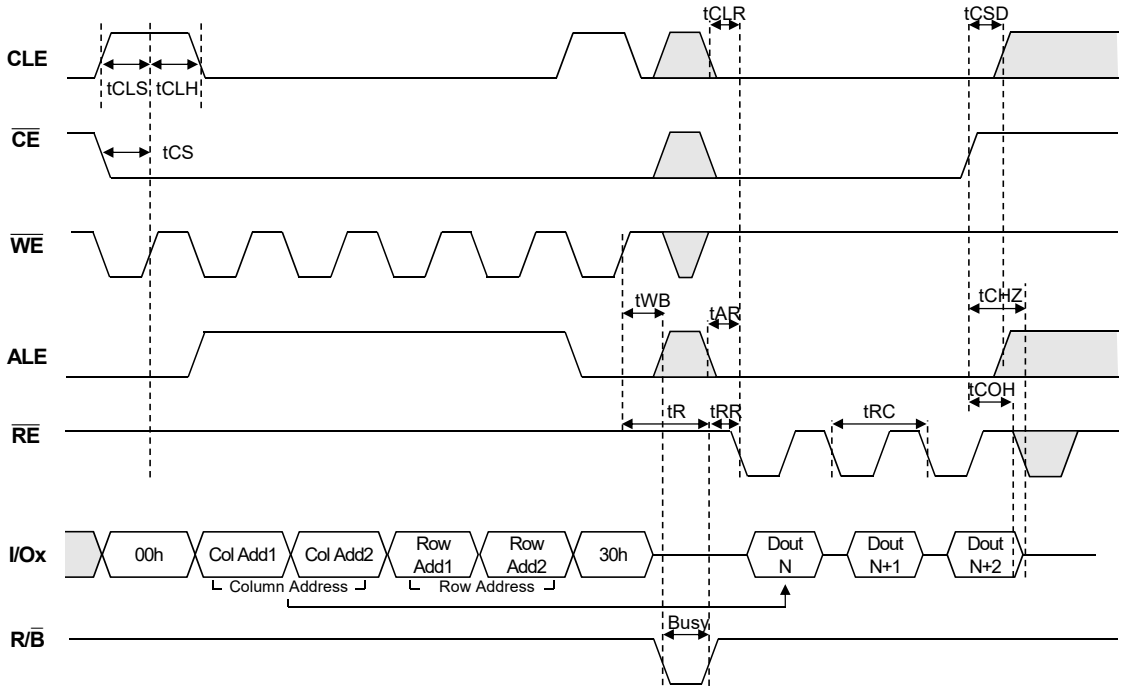
5.2 Read Status Cycle



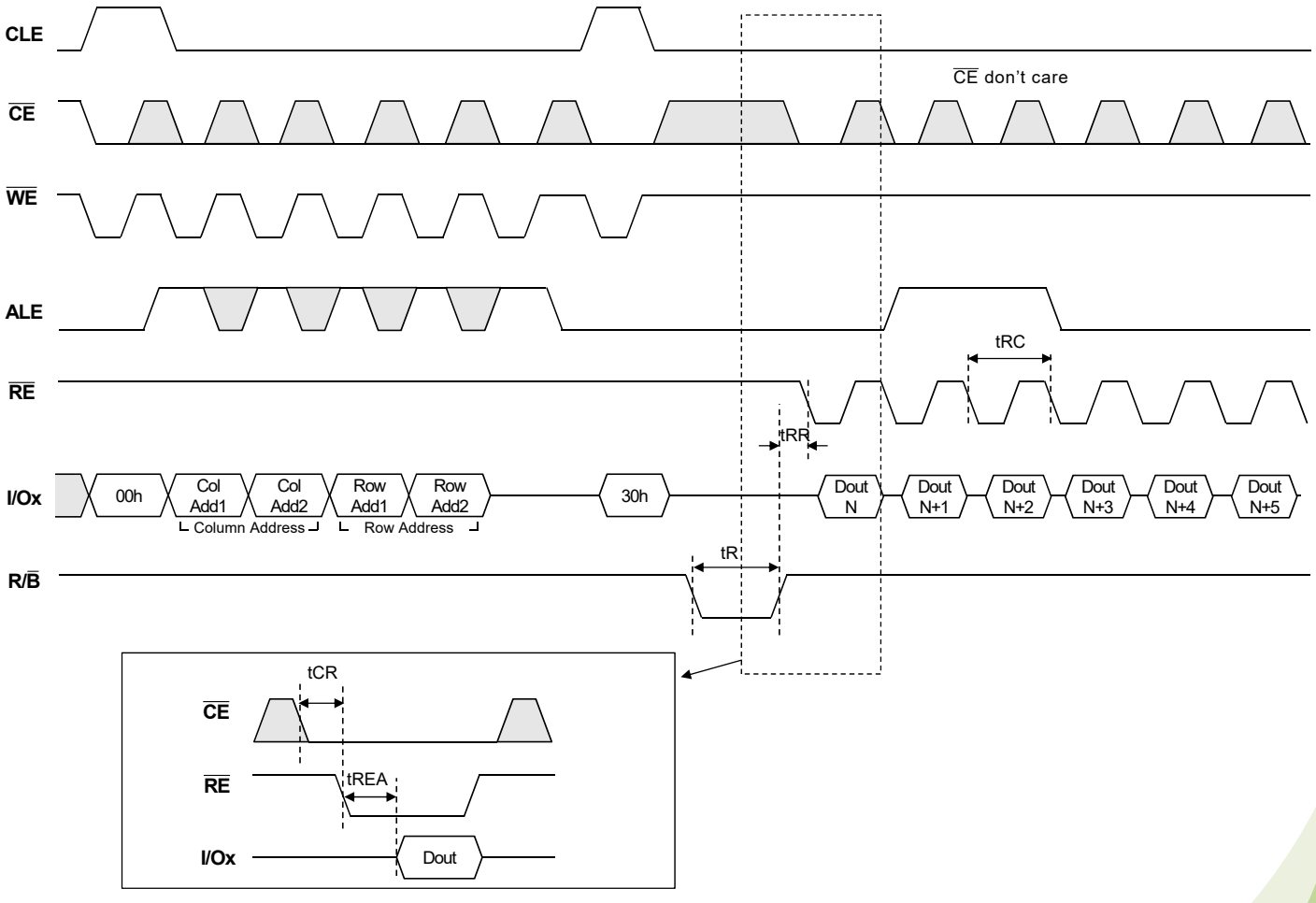
5.3 Page Read Operation



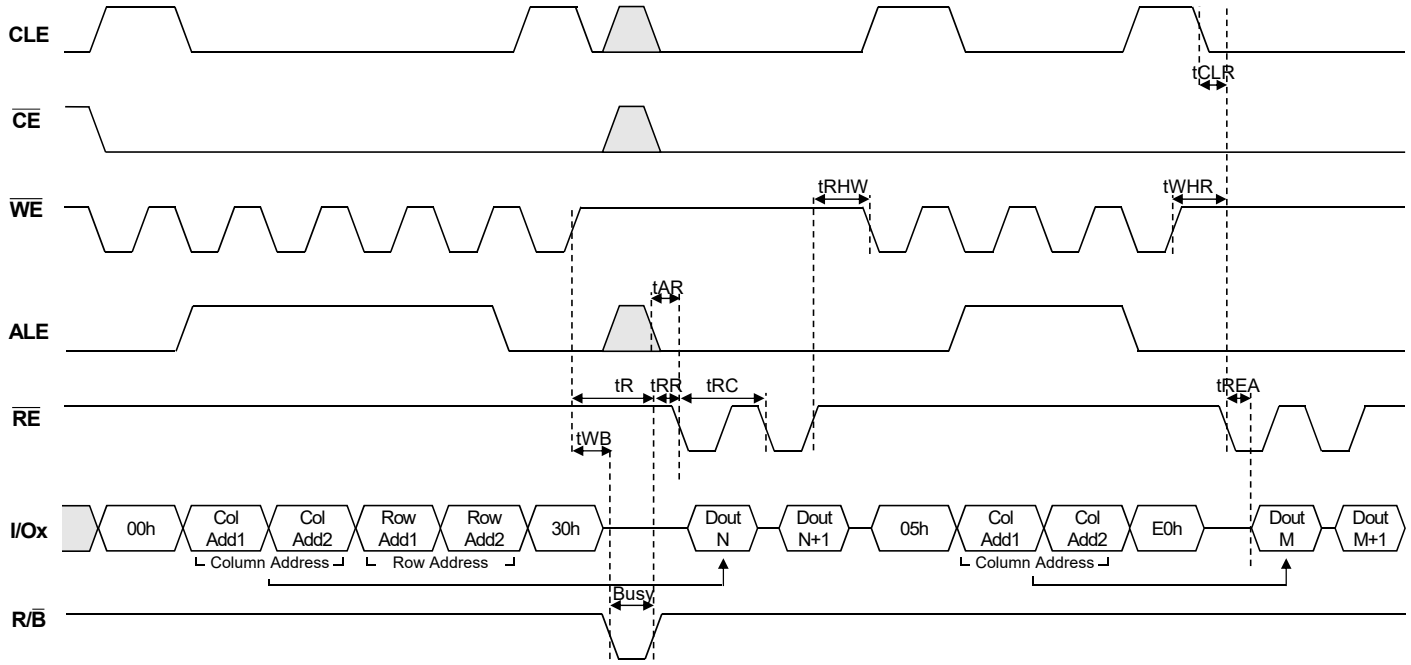
5.4 Page Read Operation (Intercepted by $\overline{CE}$)



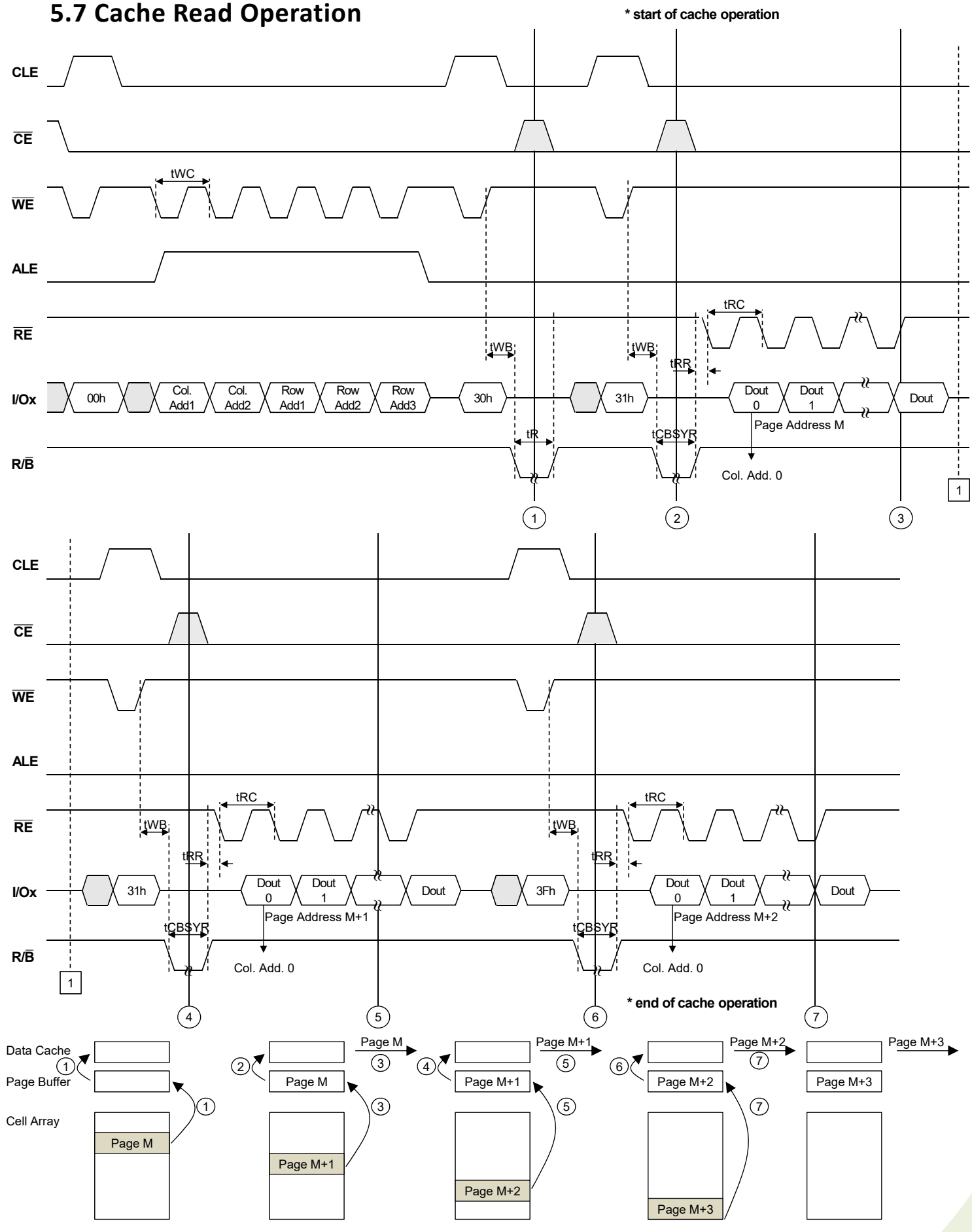
5.5 Page Read Operation with $\overline{CE}$ don't care



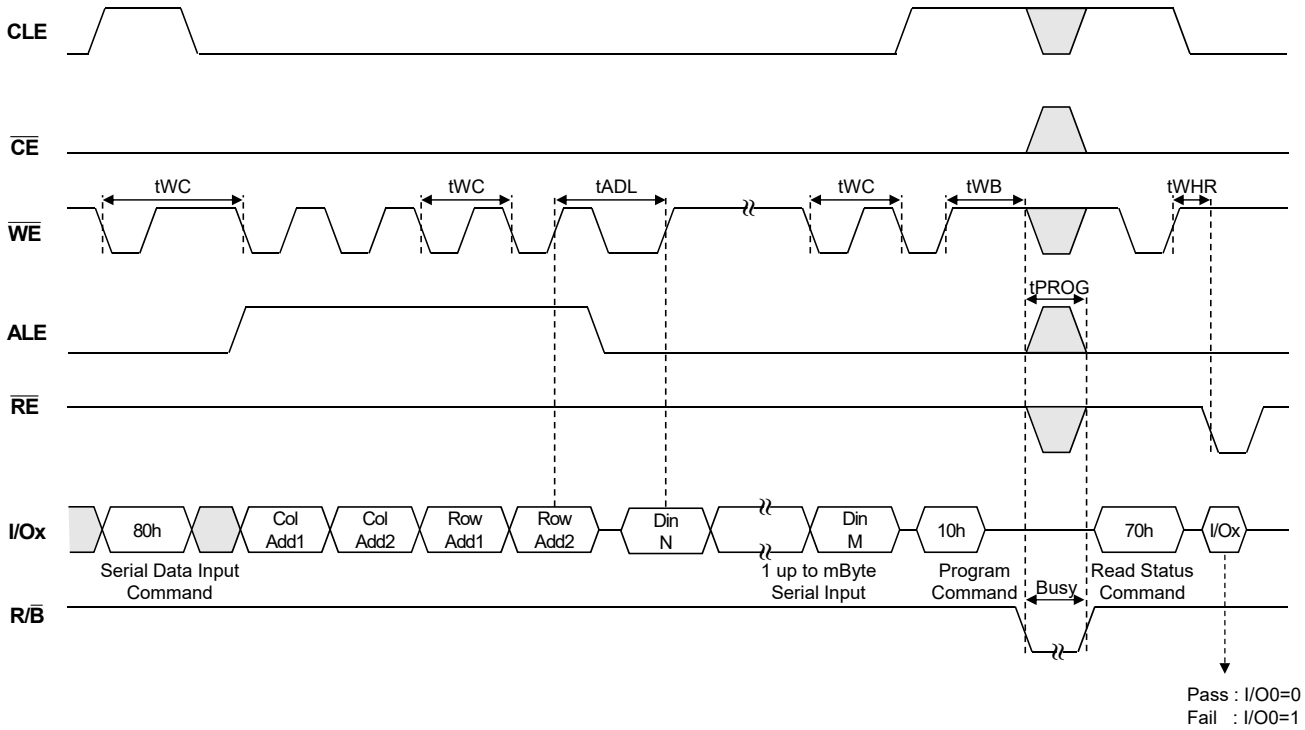
5.6 Random Data Output In a Page Operation



5.7 Cache Read Operation

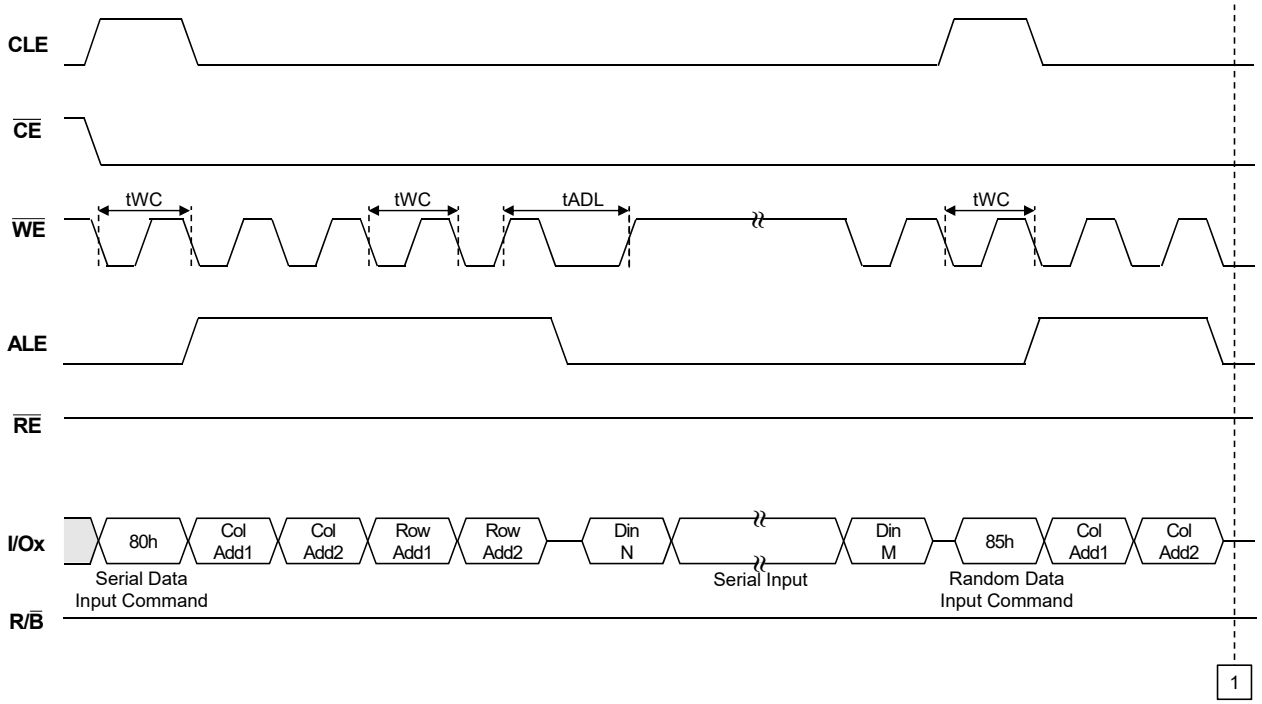


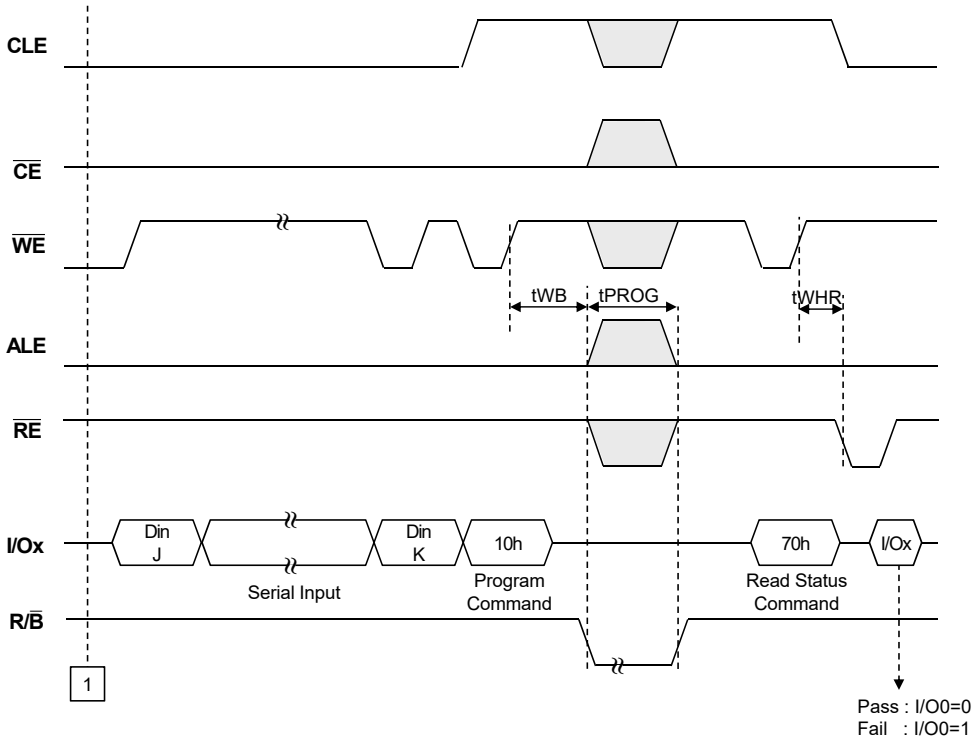
5.8 Page Program Operation



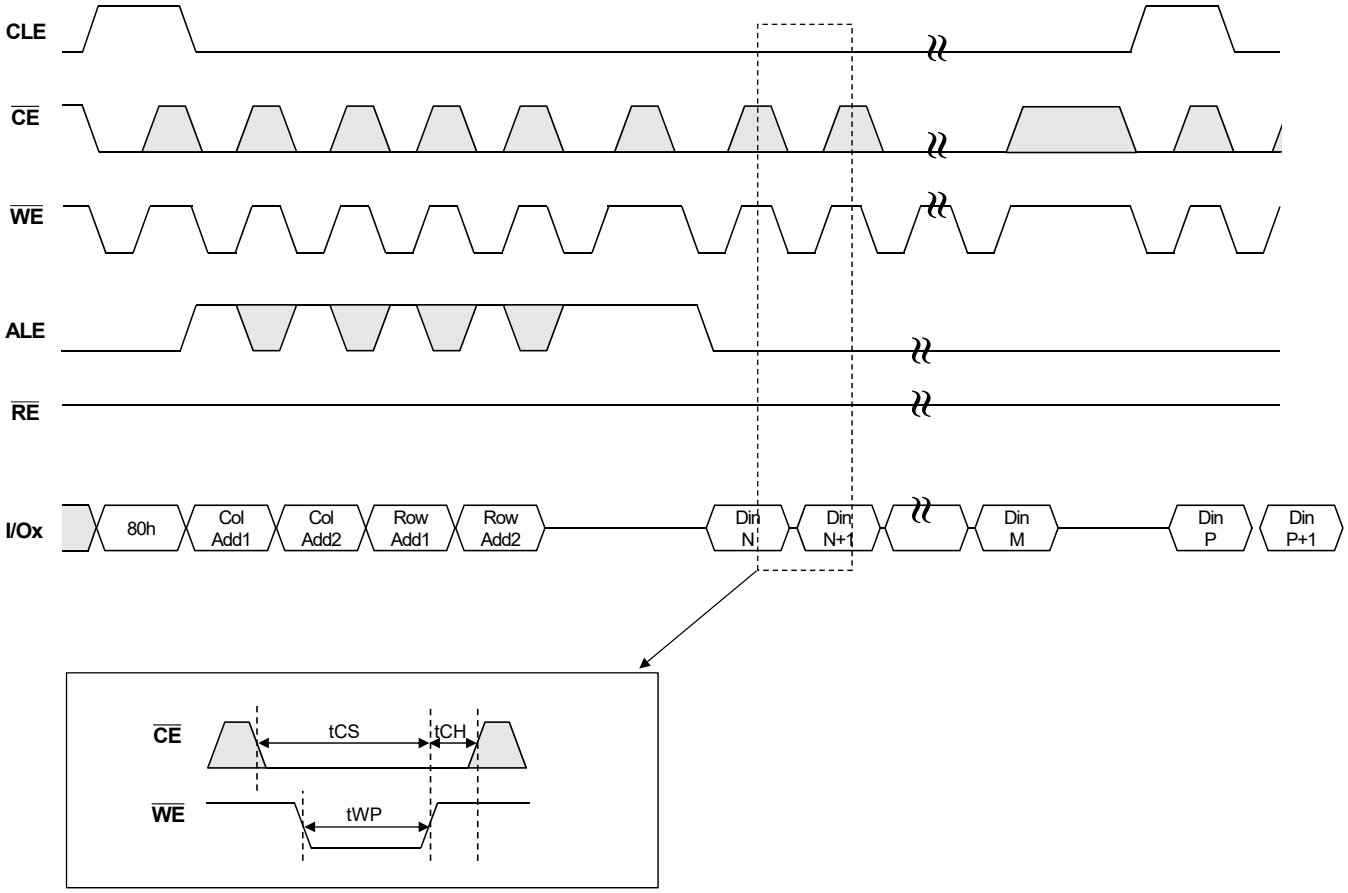
NOTE :
tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

5.9 Page Program Operation with Random Data Input Operation

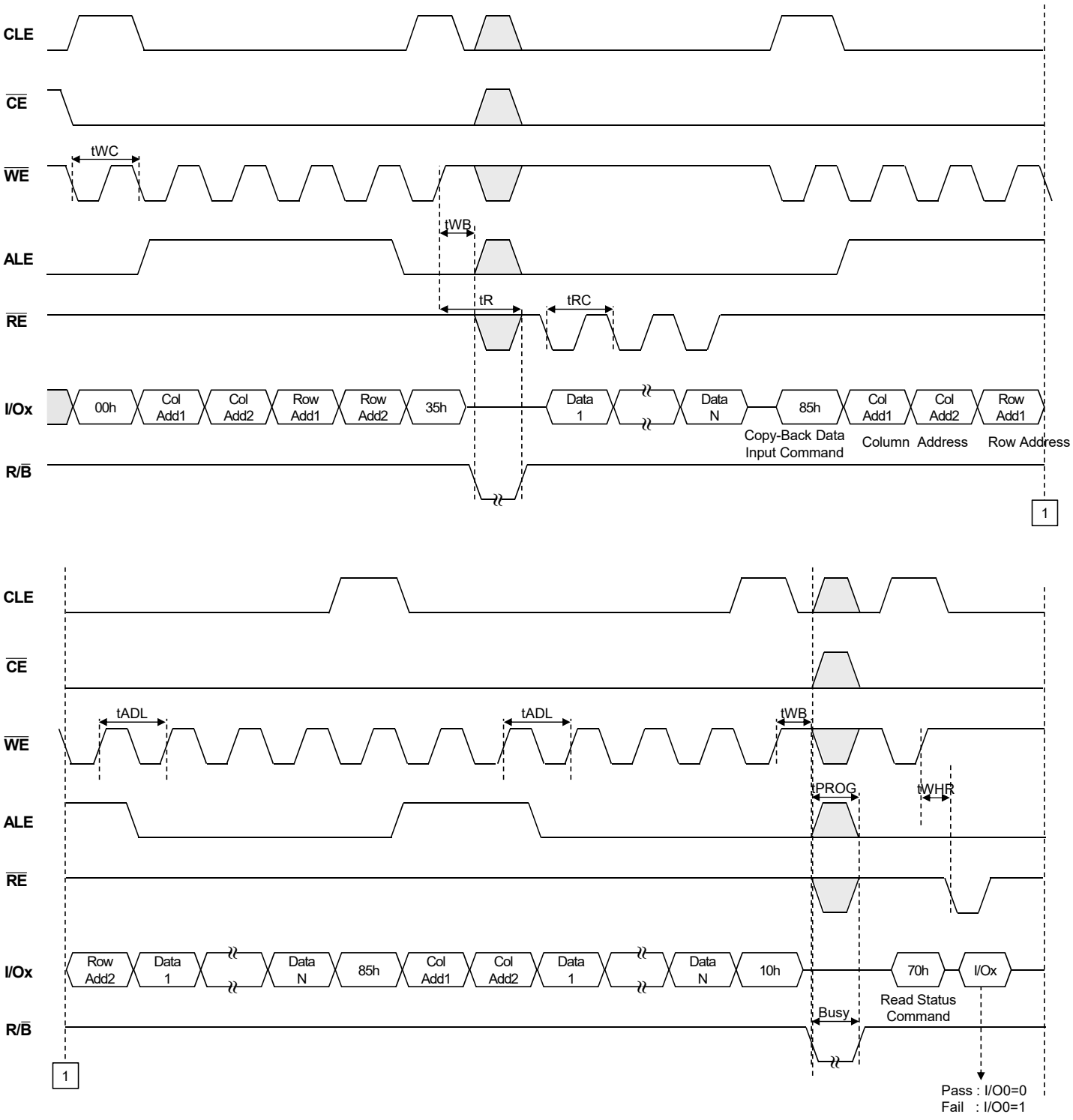




5.10 Page Program Operation with $\overline{CE}$ don't care

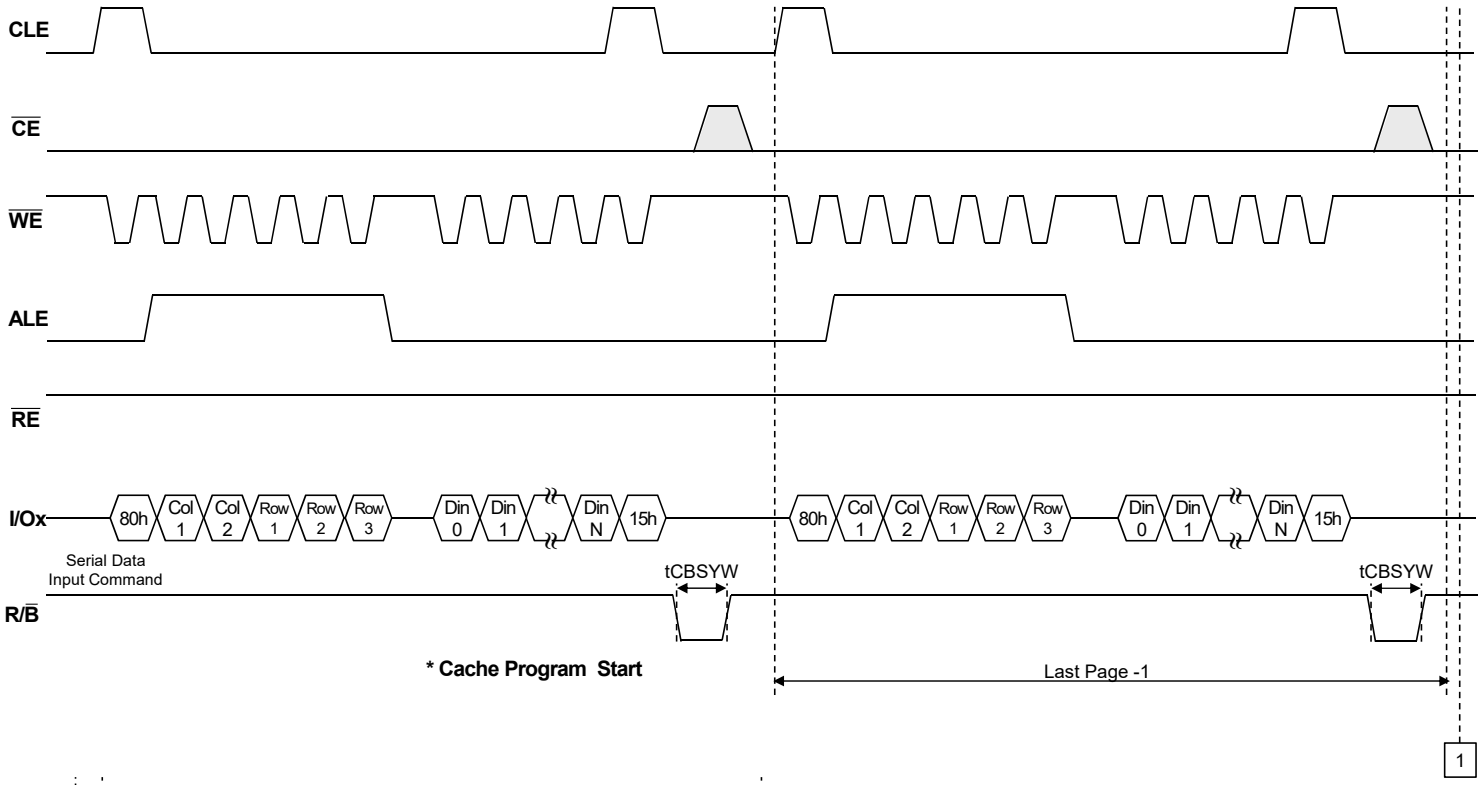


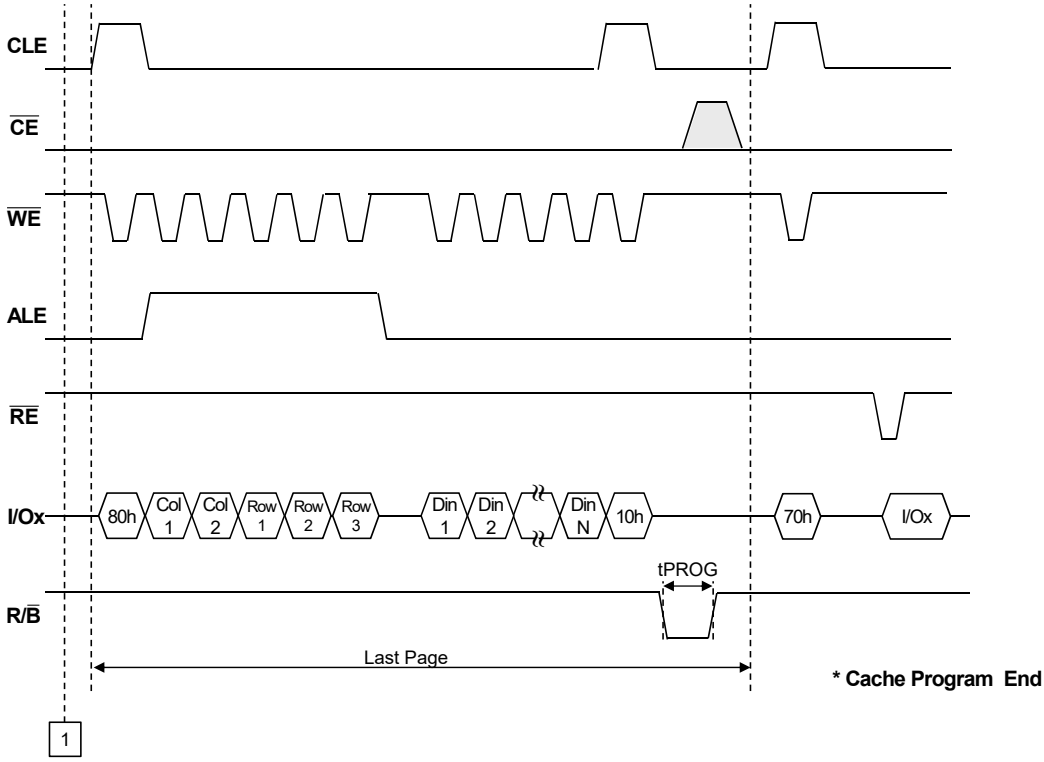
5.11 Copy-Back Program Operation with Random Data Input Operation



NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

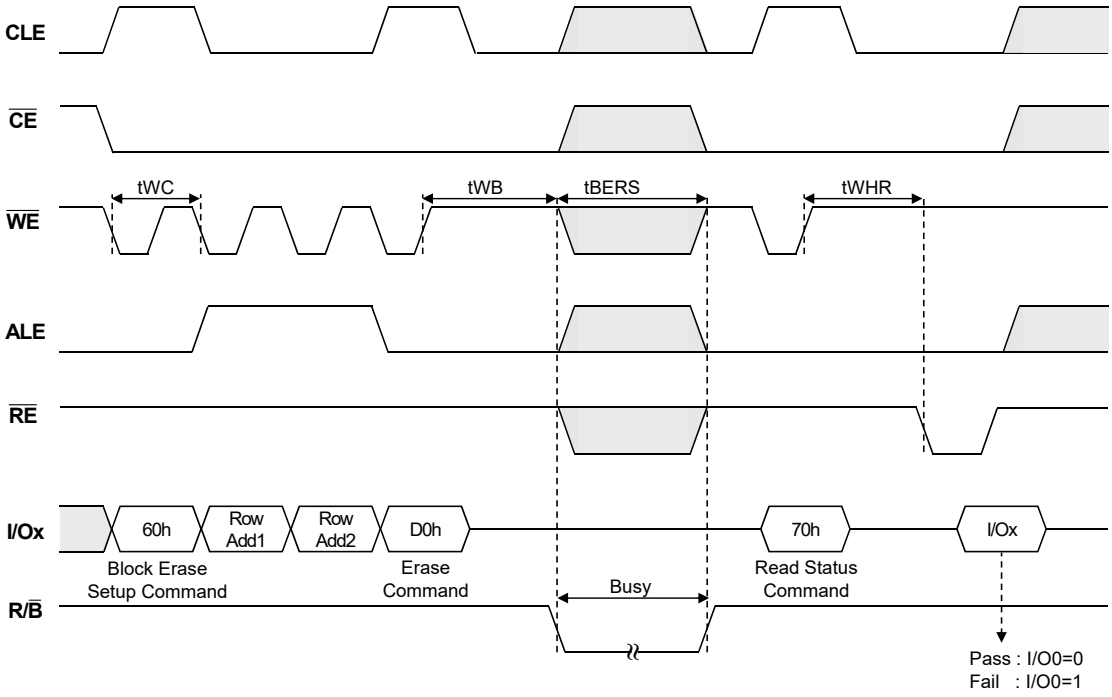
5.12 Cache Program Operation



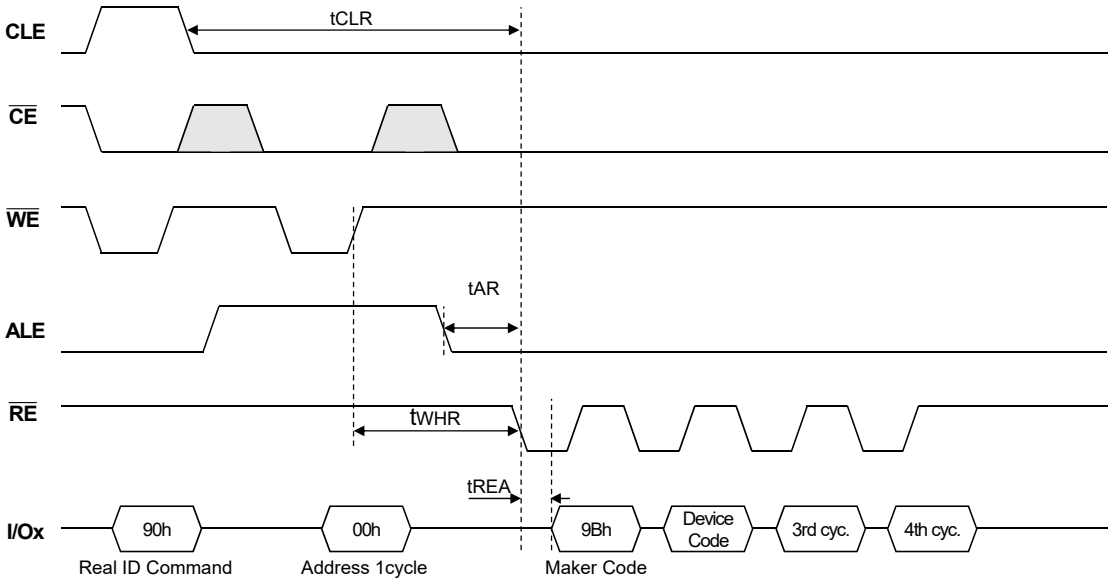


NOTE :
tPROG = Program time for the last page + Program time for the (last -1)th page - (command input cycle time + address input cycle time + Last page data loading time)

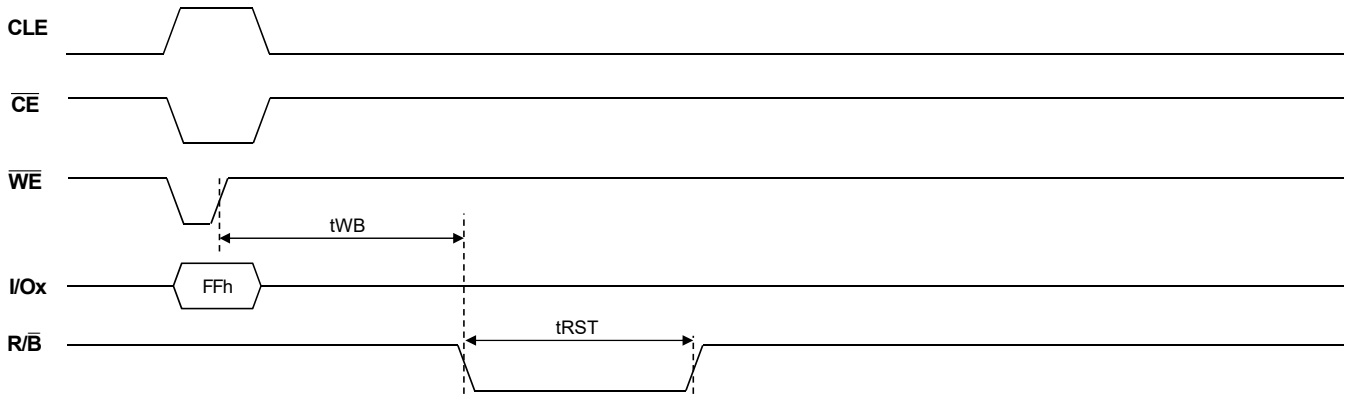
5.13 Block Erase Operation



5.14 Read ID Operation



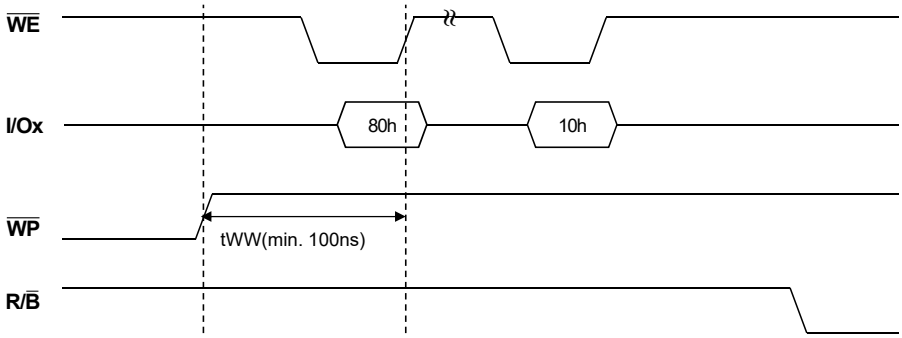
5.15 Reset Operation



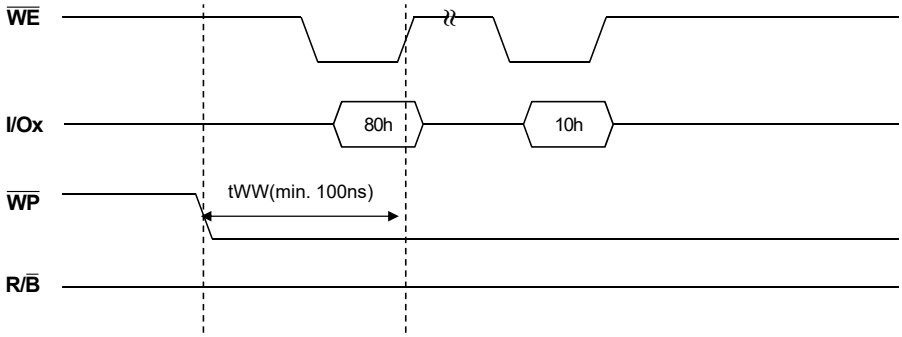
5.16 Write Protection Operation

Enabling $\overline{WP}$ during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

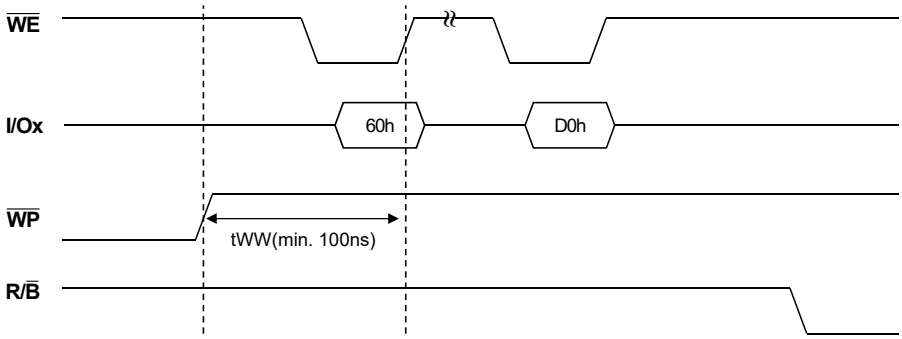
- Program Enable Mode



- Program Disable Mode



- Erase Enable Mode



- Erase Disable Mode