



# Low Power Pseudo SRAM

1M word x 16 bit

CS26LV16173

Cover Sheet and Revision Status				
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1.0	20180019	29-MAY.-2018	New issue	Hank Lin
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# Low Power Pseudo SRAM

1M word x 16 bit

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Product Description.....	1
Features.....	1
Product Family .....	1
Functional Block Diagram .....	2
Pin Descriptions.....	3
Truth Table .....	3
Absolute Maximum Ratings <sup>(1)</sup> .....	3
Revommended DC Operating Conditions.....	4
DC and Operating Characteristics .....	4
Capacitance <sup>(1)</sup> .....	5
AC Input/Output Reference Waveform.....	5
AC Test Conditions .....	5
AC Characteristicts .....	6
Power Up Sequence .....	6
Standby Mode State machines .....	7
Standby Mode Characteristics .....	7
Timing Diagrams.....	8
Power_On Timing .....	9
Deep Power Down Mode Entry/Exit.....	10
Order information.....	10
Package Dimensions: .....	11



### ■ Product Description

The CS26LV16173 is a high performance, high speed, low power pseudo SRAM organized as 1M words by 16 bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced DRAM technology and circuit techniques provide both high speed and maximum access time of 70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers. The CS26LV16173 has the page access operation, page size is 16 words, and has a deep power down feature, reducing the power consumption significantly when chip is deselected. The CS26LV16173 is available 48-ball TFBGA package.

### ■ Features

- Single power supply voltage of 2.7 to 3.6V
- Direct TTL compatibility for all inputs and outputs.
- Deep power-down mode: Memory cell data invalid.
- Page operation mode
- Page read operation by 16 words.
- Logic compatible with SRAM R/W pin.
- Standby Current
  - Standby 120 uA(Max)
  - Deep power-down standby 15 uA (Max.)
- Access Time
  - /CE1 Access Time: 70ns
  - /OE Access Time: 25ns
  - Page Access Time: 25ns

### ■ Product Family

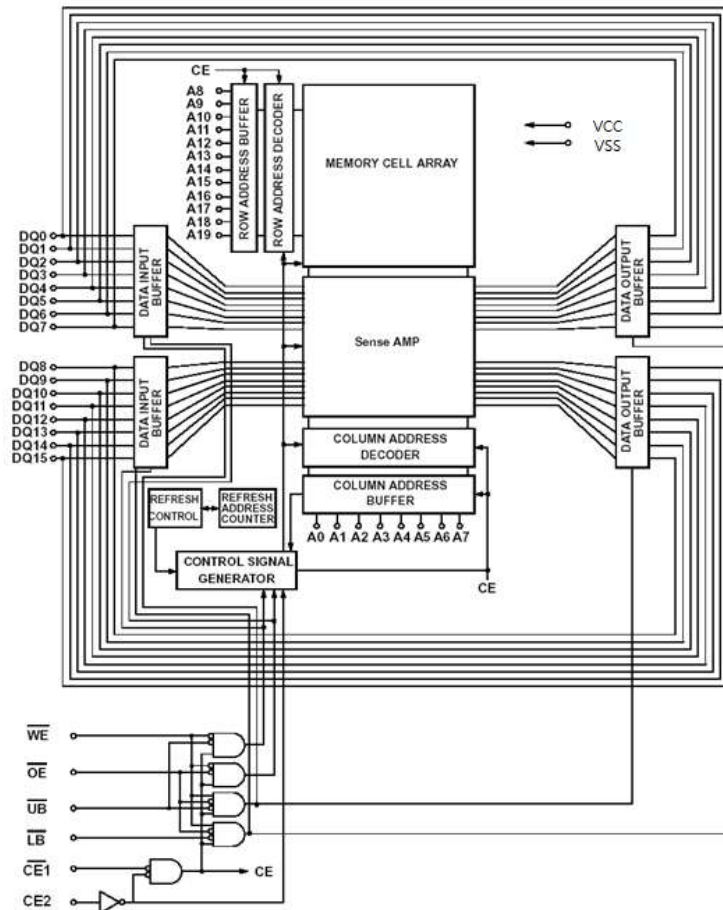
Product Family	Operating Temp	Vcc. Range	Speed(ns)	Standby (Max.)	Package Type
CS26LV16173	0~70°C	2.7~3.6	70	120 uA	48ball TFBGA-6*8mm
	-40~85°C				

## Pin Configuration



48 TFBGA - Top View

## ■ Functional Block Diagram





### ■ Pin Descriptions

Name	Type	Function
A0~A19	input	Address input
CE1	input	Chip Enable Input1, Low : Enable
CE2	input	Chip Enable Input2, High: Enable, Low: Enter Power Down mode
/WE	input	Write Enable input, Low :Enable
/OE	input	Output Enable input, Low :Enable
/LB	input	Lower byte write control
/UB	input	Upper byte write control
DQ0~DQ15	I/O	Data inputs/outputs
V <sub>CC</sub>	Power	Device Power supply
V <sub>SS</sub>	Power	V <sub>SS</sub> must be connected ground
V <sub>CCQ</sub>	Power	I/O Power supply
V <sub>SSQ</sub>	Power	V <sub>SSQ</sub> must be connected ground
DNU		Do not use

### ■ Truth Table

MODE	/CE1	CE2	/OE	/WE	/LB	/UB	DQ0~7	DQ8~15	V <sub>CC</sub> Current
Standby	H	H	X	X	X	X	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
Output Disabled	L	H	H	H	X	X	High Z	High Z	I <sub>CC</sub>
Read	L	H	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub>
Upper Byte Read					L	H	D <sub>OUT</sub>	High Z	I <sub>CC</sub>
Lower Byte Read					H	L	High Z	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	H	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC</sub>
Upper Byte Write					L	H	D <sub>IN</sub>	Invalid	I <sub>CC</sub>
Lower Byte Write					H	L	Invalid	D <sub>IN</sub>	I <sub>CC</sub>

Note: X means don't care. (Must be low or high state)

### ■ Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Parameter	Rating	Unit
V <sub>IN</sub>	Input Voltage	-0.2 to V <sub>CC</sub> +0.3	V
V <sub>OUT</sub>	Output Voltage	-0.2 to V <sub>CC</sub> +0.3	
V <sub>CC</sub>	Device Power Supply Voltage	-0.2 to 3.6	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>A</sub>	Operating Temperature	-40 to +85	°C
P <sub>D</sub>	Power Dissipation	1.0	W

1. Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device.

Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### ■ Recommended DC Operating Conditions

( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.0\text{V}$ )

Item	Symbol	CS26LV16173			Unit
		Min	Typ	Max	
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V
I/O operating voltage ( $V_{CCQ} \leq V_{CC}$ )	$V_{CCQ}$	2.7	3.0	3.6	V
Ground	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	$0.7V_{CCQ}$	$V_{CC}$	$V_{CC}+0.2^{1)}$	V
Input low voltage	$V_{IL}$	$-0.2^{2)}$	0	$0.2V_{CCQ}$	V

Note :

1. Overshoot :  $V_{CC}+1.0\text{V}$  in case of pulse width  $\leq 20\text{ns}$ .
2. Undershoot :  $-1.0\text{V}$  in case of pulse width  $\leq 20\text{ns}$ .
3. Overshoot and undershoot are sampled, not 100% tested.

### ■ DC and Operating Characteristics

Item	Symbol	Test Conditions	Min.	Typ	Max.	unit
Input leakage current	$I_{LI}$	$V_{IN}=V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$
Output leakage current	$I_{LO}$	$/CS=V_{IH}, /ZZ=V_{IH}, /OE=V_{IH}$ or $/WE=V_{IL}, V_{IO}=V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$
Average operating current	$I_{CC1}$	Cycle time=1 $\mu\text{s}$ , 100%duty, $I_{IO}=0\text{mA}$ , $/CS \leq 0.2\text{V}$ , $/ZZ=V_{IH}, V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}$	-	-	3	$\text{mA}$
	$I_{CC2}$	Cycle time=Min, $I_{IO}=0\text{mA}$ , 100% duty, $/CS=V_{IL}$ , $/ZZ=V_{IH}, V_{IN}=V_{IL}$ or $V_{IH}$	-	-	20	$\text{mA}$
Page mode operating current	$I_{CCP}$	Cycle time=Min ( $t_{RC}, t_{PC}$ ), $I_{IO}=0\text{mA}$ , 100% duty, $/CS=V_{IL}, /ZZ=V_{IH}, V_{IN}=V_{IL}$ or $V_{IH}$	-	-	15	$\text{mA}$
Output low voltage	$V_{OL}$	$I_{OL}=0.5\text{mA}$			$0.2^*$ $V_{CCQ}$	V
Output high voltage	$V_{OH}$	$I_{OH}=-0.5\text{mA}$	$0.8^*$ $V_{CCQ}$			V
Standby Current(TTL)	$I_{SB}$	$/CS=V_{IH}, /ZZ=V_{IH}$ , Other inputs= $V_{IH}$ or $V_{IL}$	-	-	0.3	$\text{mA}$
Standby Current(CMOS)	$I_{SB1}$	$/CS \geq V_{CC}-0.2\text{V}, /ZZ \geq V_{CC}-0.2\text{V}$ , Other inputs= $0 \sim V_{CC}$	-	-	120	$\mu\text{A}$
Deep Power Down Modes	$I_{SB0}$	$/ZZ \leq 0.2\text{V}$ , Other inputs= $0 \sim V_{CC}$ , No refresh(DPD)	-	-	15	$\mu\text{A}$

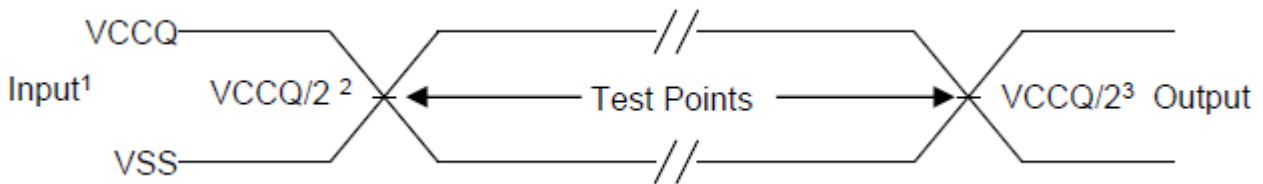
## ■ Capacitance <sup>(1)</sup>

(TA = 25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Min.	MAX.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	2	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =0V	3.5	5	pF

1. This parameter is sampled periodically and is not 100% tested

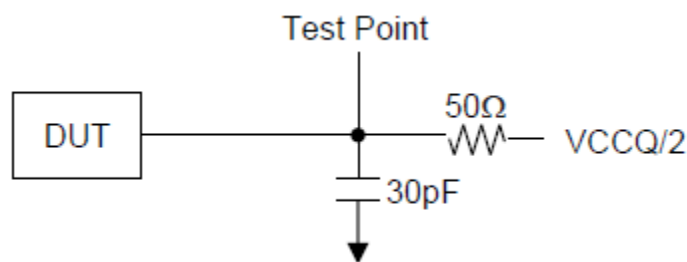
## ■ AC Input/Output Reference Waveform



NOTE:

1. AC test inputs are driven at V<sub>CCQ</sub> for a logic 1 and V<sub>SS</sub> for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at V<sub>CCQ</sub>/2.
3. Output timing ends at V<sub>CCQ</sub>/2.

## ■ AC Test Conditions



### ■ AC Characteristics

(V<sub>CC</sub>=2.7V~3.6V, Commercial product: TA=-0 to 70 °C , Industrial product : TA=-40 to 85 °C)

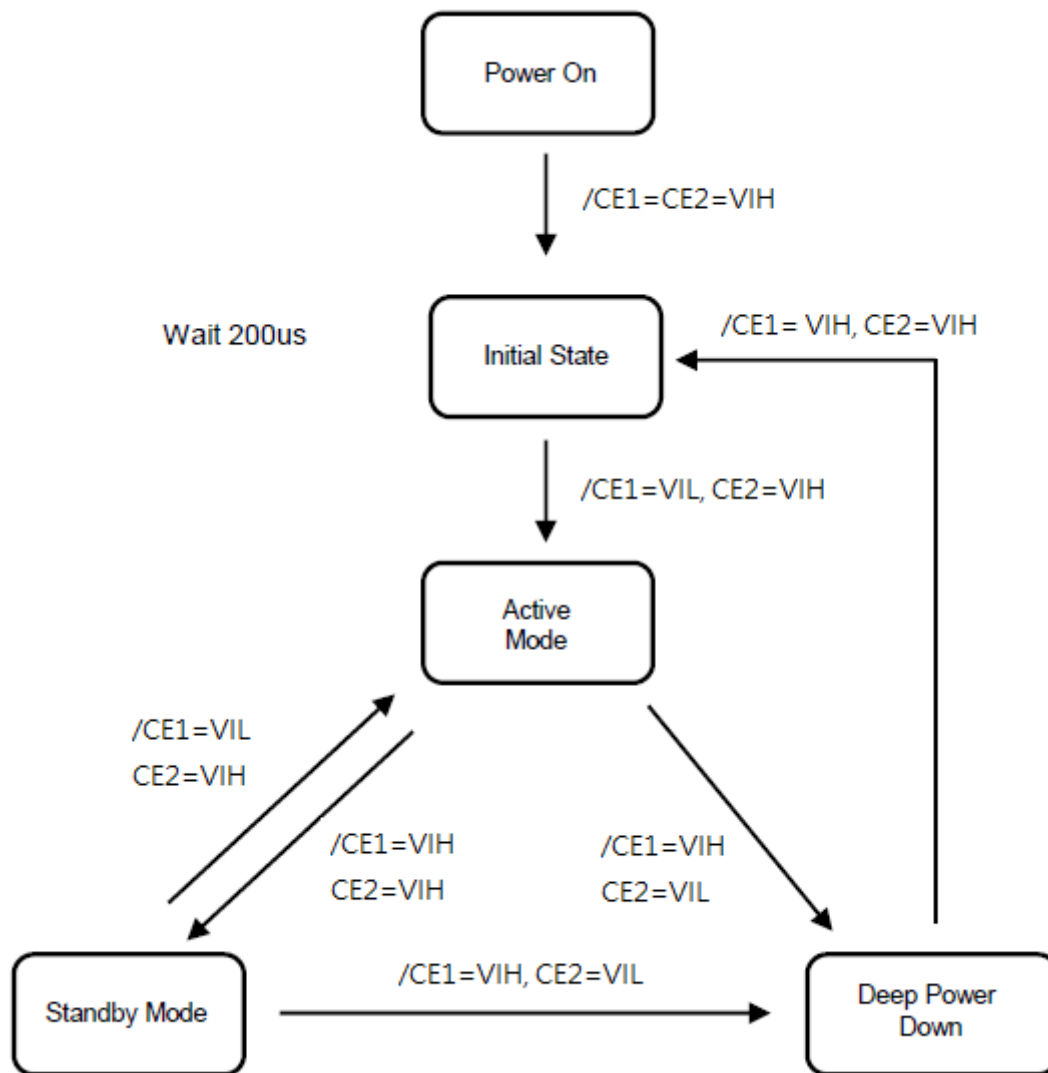
Parameter List		Symbol	70ns		Units
			Min	Max	
Read	Read Cycle Time	t <sub>RC</sub>	70	-	ns
	Address Access Time	t <sub>AA</sub>	-	70	ns
	Chip Select to Output	t <sub>CO</sub>	-	70	ns
	Output Enable to Valid Output	t <sub>OE</sub>	-	20	ns
	/UB, /LB Access Time	t <sub>BA</sub>	-	25	ns
	Chip Select to Low-Z Output	t <sub>LZ</sub>	10	-	ns
	/UB, /LB Enable to Low-Z Output	t <sub>BLZ</sub>	0	-	ns
	Output Enable to Low-Z Output	t <sub>OLZ</sub>	0	-	ns
	Chip Disable to High- Z Output	t <sub>HZ</sub>	0	8	ns
	/UB, /LB Disable to High- Z Output	t <sub>BHZ</sub>	0	8	ns
	Output Disable to High- Z Output	t <sub>OHZ</sub>	0	8	ns
	Output Hold from Address Change	t <sub>OH</sub>	5	-	ns
Write	Write Cycle Time	t <sub>WC</sub>	70	20k	ns
	Chip Select to End of Write	t <sub>CW</sub>	60	-	ns
	Address Set-up Time	t <sub>AS</sub>	0	-	ns
	Address Valid to End of Write	t <sub>AW</sub>	60	-	ns
	/UB, /LB Valid to End of Write	t <sub>BW</sub>	60	-	ns
	Write Pulse Width	t <sub>WP</sub>	50	-	ns
	Write Recovery Time	t <sub>WR</sub>	0	-	ns
	Write to Output High-Z	t <sub>WHZ</sub>	0	8	ns
	Data to Write Time Overlap	t <sub>DW</sub>	20	-	ns
	Data Hold from Write Time	t <sub>DH</sub>	0	-	ns
	End Write to Output Low-Z	t <sub>OW</sub>	5	-	ns
Page	Page Mode Cycle Time	t <sub>PC</sub>	25	-	ns
	Page Mode Address Access Time	t <sub>PAA</sub>	-	25	ns
	Maximum Cycle Time	t <sub>MRC</sub>	-	20k	ns
/CS High Pulse Width		t <sub>CP</sub>	10	-	ns

### ■ Power Up Sequence

1. Apply Power
2. Maintain stable power for a minimum of 200us with /CE1=CE2=V<sub>IH</sub>



## ■ Standby Mode State machines

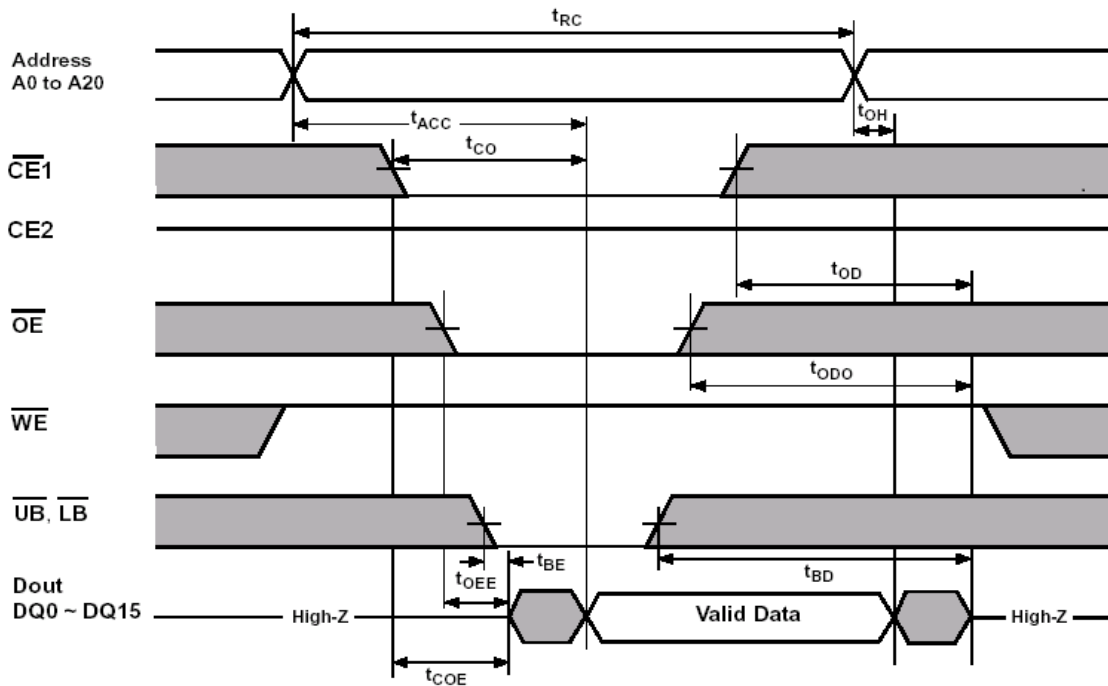


## ■ Standby Mode Characteristics

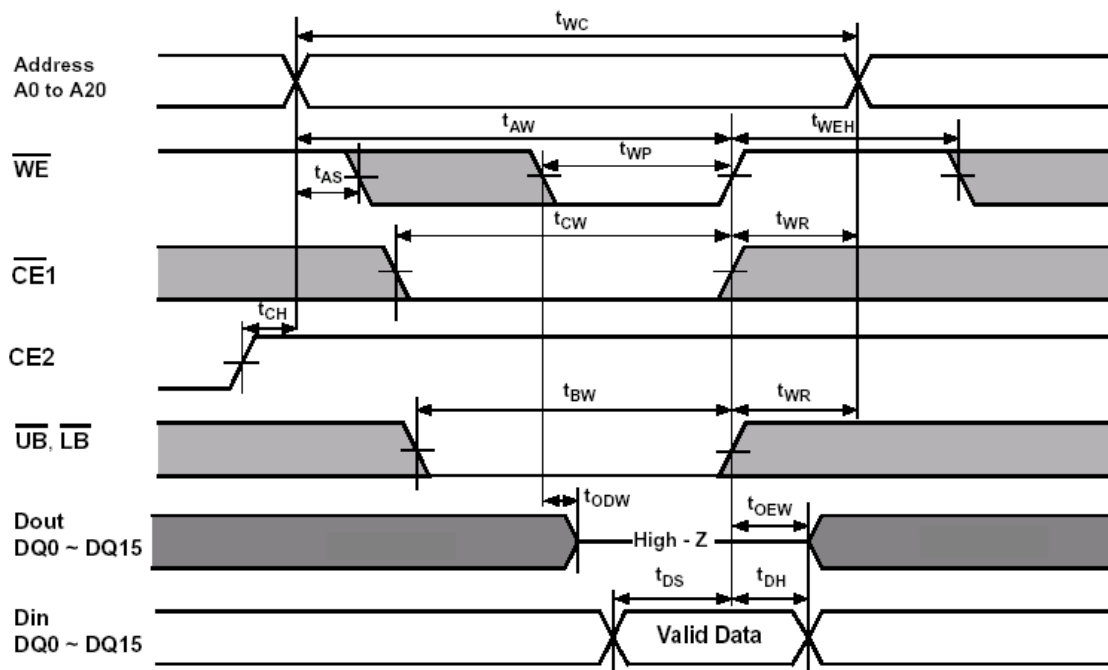
Mode	Memory Cell Data	Standby Current(uA)	Wait Time(us)
Standby	Valid	120 (ISB1)	0
Deep Power Down	Invalid	15 (ISB0)	200

## ■ Timing Diagrams

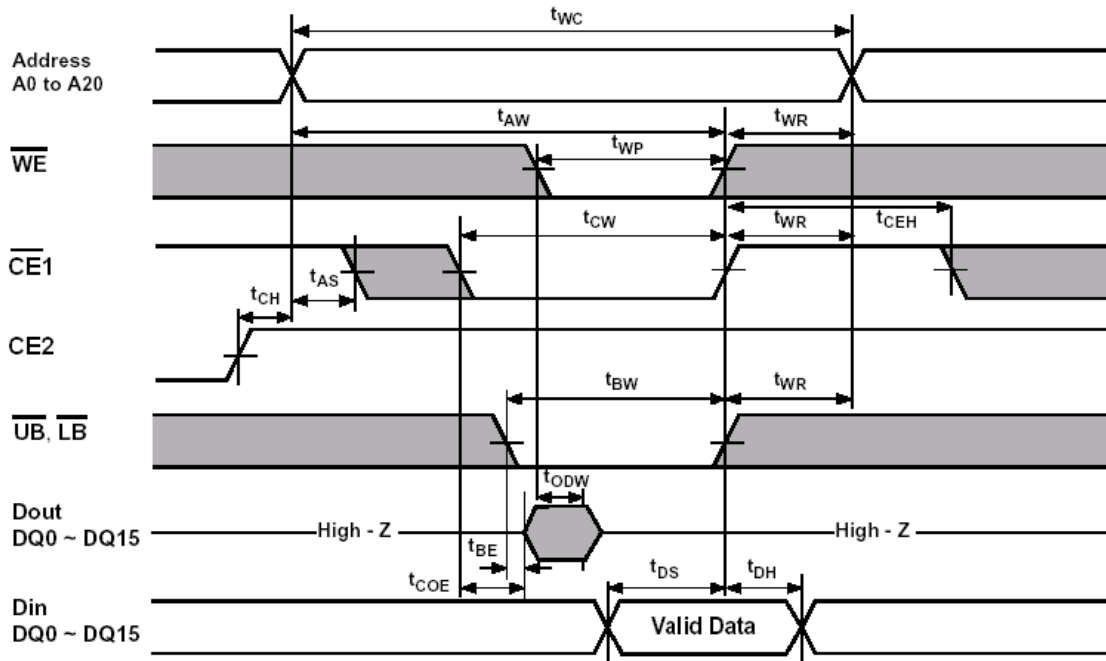
### <Read Cycle>



### Write Cycle (1) (/WE controlled)



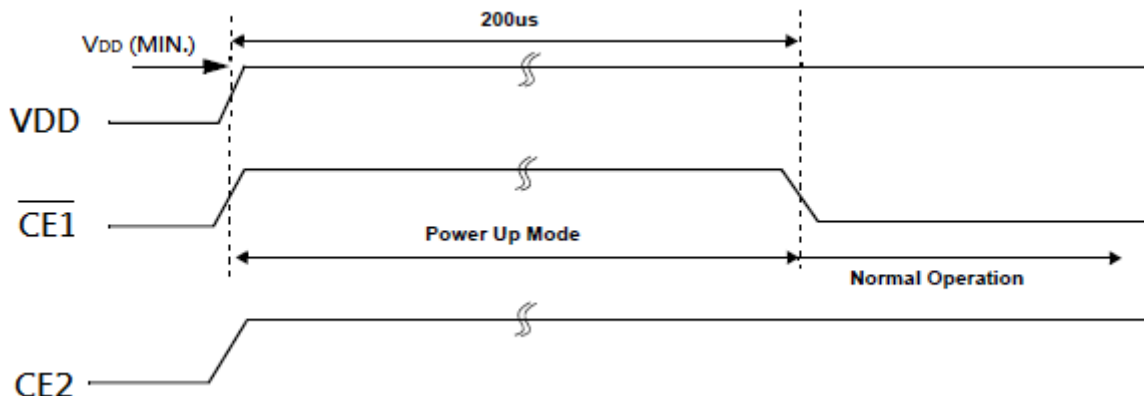
## Write Cycle (2) (/CE1 controlled)



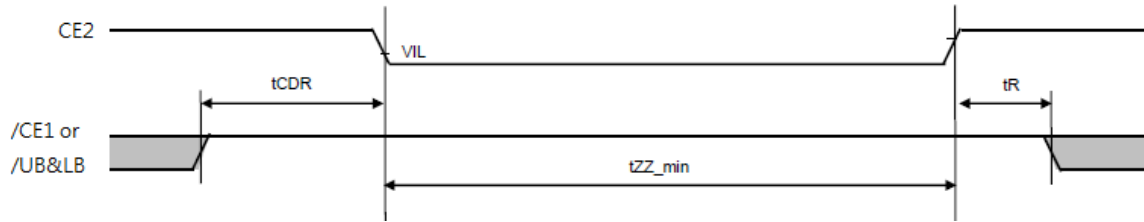
### NOTES

1. AC measurement are assumed  $t_R, t_F = 5\text{ns}$ .
2. Parameters  $t_{OD}, t_{ODO}, t_{BD}$  and  $t_{ODW}$  define the time at which the output goes the open condition and are not output voltage reference levels.
3. If /OE is high during the write cycle, the outputs will remain at high impedance.
4. During the output state of DQ signals, input signals of reverse polarity must not be applied.
5. If /CE1 or /LB&/UB goes LOW coincident with or after /WE goes LOW, the outputs will remain at high impedance.
6. If /CE1 or /LB&/UB goes HIGH coincident with or before /WE goes HIGH, the outputs will remain at high impedance.

## ■ Power\_On Timing

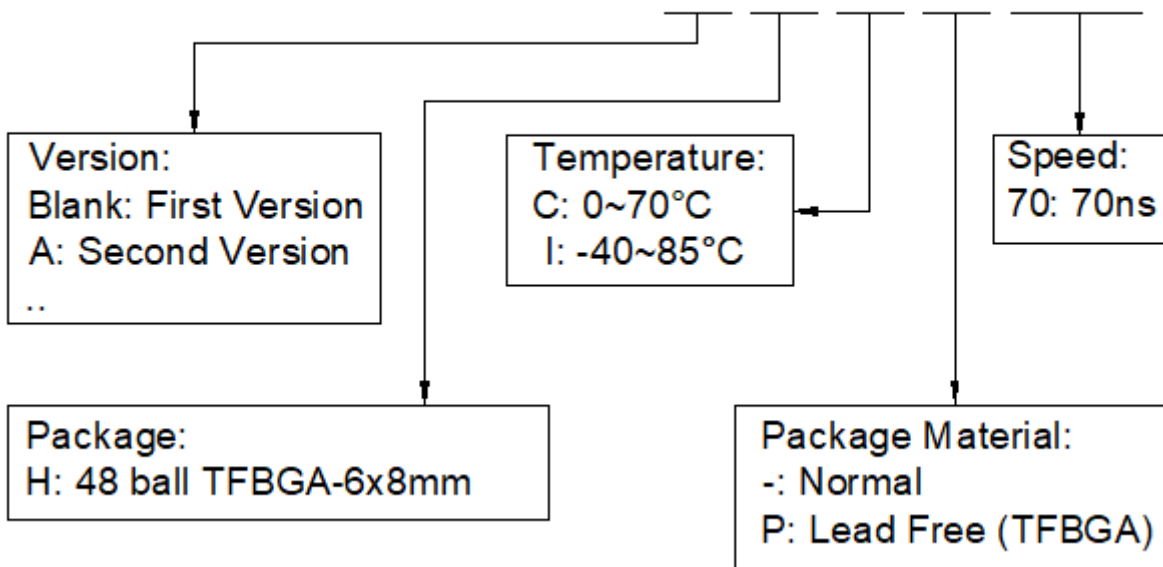


### ■ Deep Power Down Mode Entry/Exit



### ■ Order information

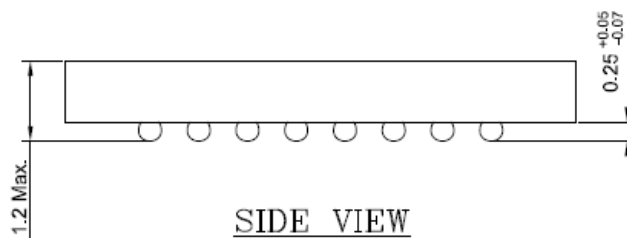
# CS26LV16173X X X X XX



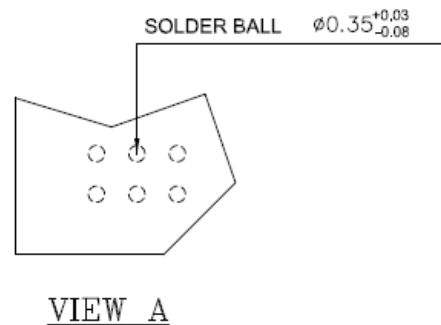
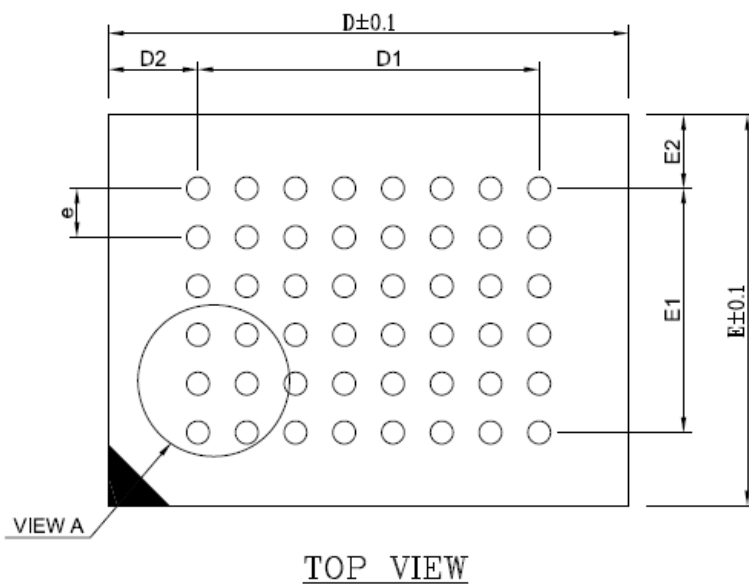
Note: Package material code "P" meets RoHS

### ■ Package Dimensions:

#### 48 ball TFBGA-6x8mm



BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125



**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:  
 LINEAR : X.X = ±0.1  
           X.XX = ±0.05  
           X.XXX = ±0.025