原盛科技股份有限公司
PrimeSensor Technology Inc.

PS5260
DATA SHEET

PRELIMINARY

1/2.7” Full-HD 1080p HDR CMOS IMAGE SENSOR

May 2018

Version 0.2

PS5260 Full-HD 1080p HDR CMOS IMAGE SENSOR

General Description

The **PS5260** is a low power, highly integrated CMOS image sensor that output of **1920x1080 (Full HD-1080p)** pixels with rolling shutter readout. It embedded the new FinePixel™ and HDR sensor technology to perform the excellent image quality and single-shot high dynamic range synthesized image output. **PS5260** outputs 12bit/10-bit compressed RGB raw data through a parallel digital video port or via serial MIPI interface through one-lane or dual-lane transmission. It is available in **CSP** package.

The **PS5260** can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip black level correction and high temperature image quality control.

Features

- **1928 x 1088 pixels with Bayer-RGB color filter array and micro-lens**
- **Output format:**
  - 14bit HDR-RAW RGB
  - 12bit/10bit Companded HDR-RAW RGB
  - 10bit RAW RGB
- **Output interface**
  - 12bit parallel DVP output
  - Dual lanes serial MIPI CSI2 output (up to 800Mbps per lane)
- **On-chip column A/D converter**
- **On-chip manual analog gain control**
- **Continuous variable frame time & exposure time**
- **I2C™ Interface**
- **Automatic black-level calibration**
- **Black sun cancellation**
- **Support WOI and subsampling**
- **Support dummy line & pixel timing**
- **Support output Hsync at Vsync**
- **Support sensor frame synchronization**
- **Support on-chip HDR synthesis**
- **On-chip PLL (input_clock / PLL_m >= 1MHz)**

Specifications

Parameter	Typical Value
Active array size	1928(H) x 1088(V)
Pixel size	3.0um (H) x 3.0um (V)
Shutter type	Electronic rolling shutter (ERS)
Optical format	1/2.7-inch
Lens chief ray angle	17 degree
ADC	10-bit
Sensitivity	4700 mV/Lux-sec
SNRmax	TBD dB
Dynamic range	83 dB
Scan mode	Progressive scan
Input clock	Max 50MHz
Pixel clock	Max 148.5MHz
Max. frame rate	1080p: 1920x1080 @ 60fps 1080p: 1920x1080 HDR @30fps
Supply voltage	Analog: 3.3 V Digital: 1.2 V I/O: 1.8V / 3.3V
Power consumption	92mW @HDR 1080p30 (MIPI) 77mW @HDR 1080p30 (DVP w/o I/O)
Operating temperature	-30ºC ~ 85ºC

Applications

- **Surveillance HD-CCTV Camera**
- **Surveillance IP Camera**
- **Car Video Recorder**
- **Video Door Phone**

Ordering Information

Part Number	Description
PS5260LT	48-ball CSP

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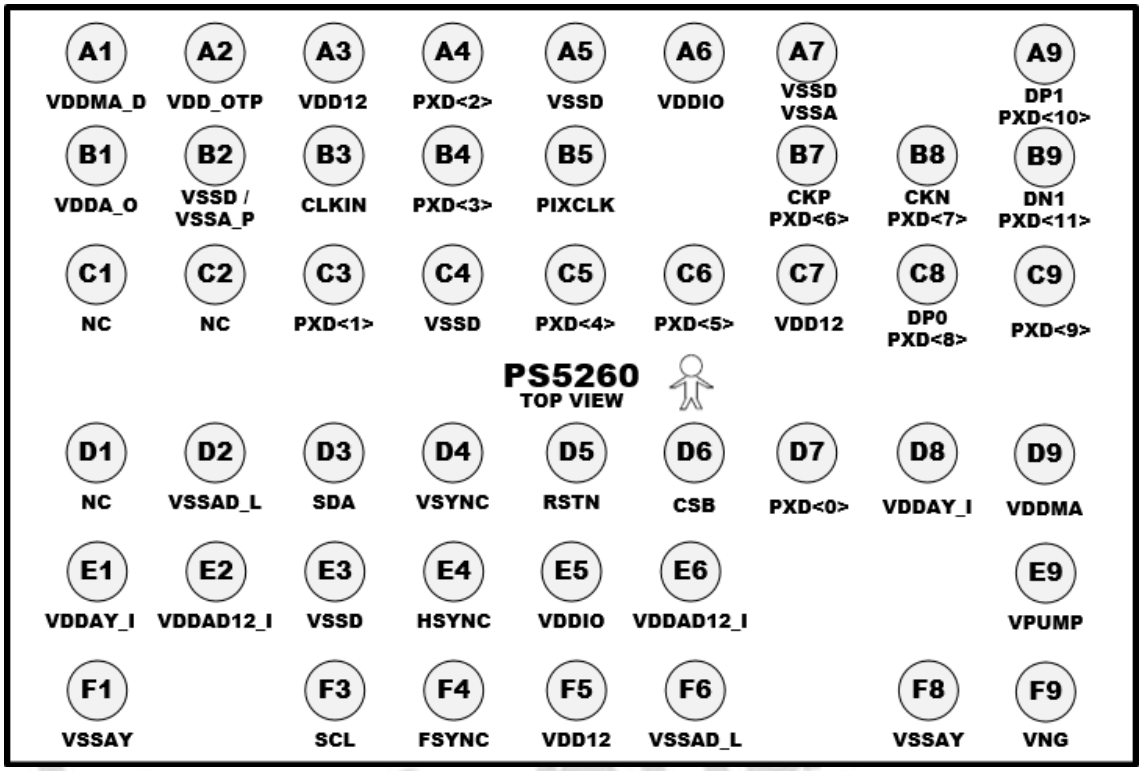
1. Pin Assignment



Pin No.	Name	Type	Description
A1	**VDDMA_D**	Power	Analog power : 3.3V
A2	**VDD_OTP**	Power	External voltage for OTP device
A3	**VDD12**	Power	Digital power : 1.2V
A4	**PXD<2>**	Output	Pixel data output
A5	**VSSD**	GND	GND
A6	**VDDIO**	Power	I/O power : 1.8V ~ 3.3V
A7	**VSSD/VSSA**	GND	GND
A9	**DP1 PXD<10>**	Output	Pixel data output ; MIPI digital data output_1 positive terminal
B1	**VDDA_O**	Power	VDDA LDO output voltage(2.7-3.0V)
B2	**VSSD/VSSA_P**	GND	GND
B3	**CLKIN**	Input	Master clock input
B4	**PXD<3>**	Output	Pixel data output
B5	**PIXCLK**	Output	Pixel clock output
B7	**CKP PXD<6>**	Output	Pixel data output ; MIPI output clock positive terminal
B8	**CKN PXD<7>**	Output	Pixel data output ; MIPI output clock negative terminal
B9	**DN1 PXD<11>**	Output	Pixel data output ; MIPI digital data output_1 negative terminal
C1	**NC**		

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C2	**NC**		
C3	**PXD<1>**	Output	Pixel data output
C4	**VSSD**	GND	GND
C5	**PXD<4>**	Output	Pixel data output
C6	**PXD<5>**	Output	Pixel data output
C7	**VDD12**	Power	Digital power : 1.2V
C8	**DP0** **PXD<8>**	Output	Pixel data output ; MIPI digital data output_0 positive terminal
C9	**PXD<9>**	Output	Pixel data output
D1	**NC**		
D2	**VSSAD_L**	GND	GND
D3	**SDA**	I/O	I2C data, open drain type
D4	**VSYNC**	Output	Asserted when frame data is valid
D5	**RSTN**	Input	Reset signal, active low, internal pull high
D6	**CSB**	Input	Suspend control, "1" : suspend, "0" : normal function
D7	**PXD<0>**	Output	Pixel data output
D8	**VDDAY_I**	Power	Sensor power input
D9	**VDDMA**	Power	Analog power : 3.3V
E1	**VDDAY_I**	Power	Sensor power input
E2	**VDDAD12_I**	Power	Analog power input voltage(1.2V)
E3	**VSSD**	GND	GND
E4	**HSYNC**	Output	Asserted when line data is valid
E5	**VDDIO**	Power	I/O power : 1.8V ~ 3.3V
E6	**VDDAD12_I**	Power	Analog power input voltage(1.2V)
E9	**VPUMP**	Power	Positive pump output voltage
F1	**VSSAY**	GND	GND
F3	**SCL**	I/O	I2C clock, open drain type
F4	**FSYNC**	Input	Frame sync signal
F5	**VDD12**	Power	Digital power : 1.2V
F6	**VSSAD_L**	GND	GND
F8	**VSSAY**	GND	GND
F9	**VNG**	Power	Reference voltage

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2. Specifications

Absolute Maximum Ratings		
Operating Temperature (sensor junction temperature)		-30ºC ~ 85ºC
Ambient Storage Temperature		-40ºC ~ 125ºC
Supply Voltage (with respect to ground)	V_{DDA}	4.5V
	V_{DDD}	3.0V
	V_{DDIO}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to V_{DDIO} + 0.5V
Lead-free temperature, Surface-mount process		245ºC
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = -30℃ ~ 85℃)					
Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDA}	DC supply voltage – Analog	3.14	3.3	3.47	V
V_{DDD}	DC supply voltage – Digital core	1.14	1.2	1.26	V
V_{DDIO}	DC supply voltage – I/O	1.7	1.8	3.47	V
I_{DDA}	Operating Current – Analog (DVP)		10.70		mA
	Operating Current – Analog (MIPI)		11.88		mA
I_{DDD}	Operating Current – Digital (DVP)		34.54		mA
	Operating Current – Digital (MIPI)		44.01		mA
I_{DDIO}	Operating Current – IO 1.8V (DVP)		TBD		mA
Type : IN & I/O					
V_{IH}	Input Voltage HIGH	V_{DDIO} * 0.7			V
V_{IL}	Input Voltage LOW			V_{DDIO} * 0.3	V
Type : OUT & I/O					
V_{OH}	Output Voltage HIGH	V_{DDIO} * 0.9			V
V_{OL}	Output Voltage LOW			V_{DDIO} * 0.1	V

AC Operating Condition					
Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency		27	50	MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%

Sensor Characteristics		
Parameter	Typ.	Unit
Sensitivity	4700	mV/Lux-Sec
Maximum Signal to Noise Ratio	TBD	dB
Dynamic Range	83	dB

†: Sensor function works in the ambient operating temperature range. However, the image quality may change at high temperature condition.

†: The power consumption is measured with 4X analog gain.

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3. I²C™ Bus

PS5260 supports I²C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1001000" and supports receiving / transmitting speed as maximum 400 kHz.

I²C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 3.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 3.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

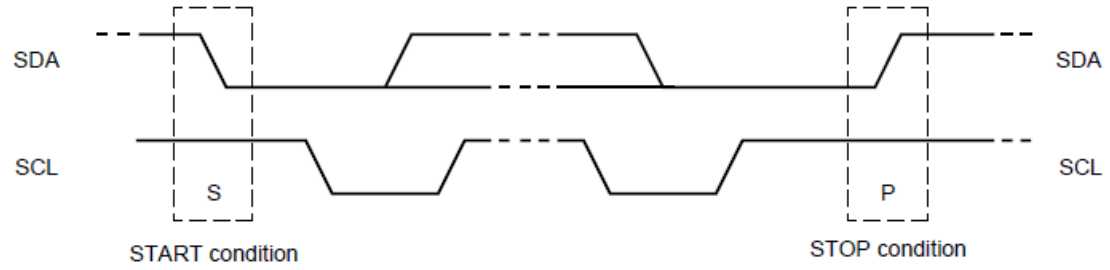

Fig.3.1 Start and Stop Condition

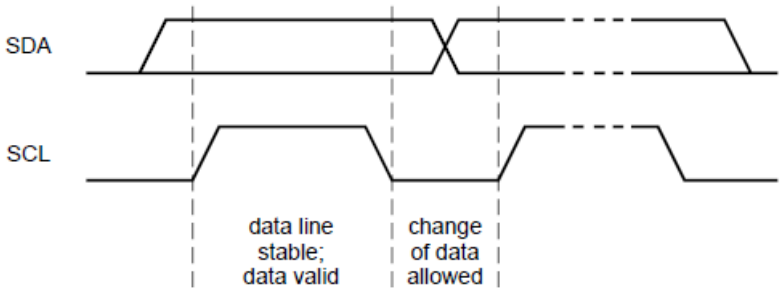

Fig.3.2 Valid Data

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Data Transfer Format

Master transmits data to salve (write cycle)

- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of **PS5260** internal control registers. (Please refer to **PS5260** register description)

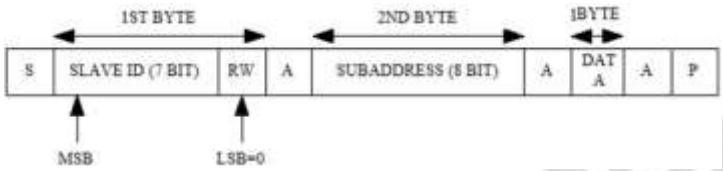

Fig.3.3 Master-transmitter transmits to slave-receiver

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (**PS5260**) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the **PS5260** acknowledgment, the master places the 8 bits data on SDA line and transmit to **PS5260** control register (address was assigned by 2nd byte). After **PS5260** issues acknowledgment, the master can generate a stop condition to end of this write cycle. Every control registers value inside **PS5260** can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.

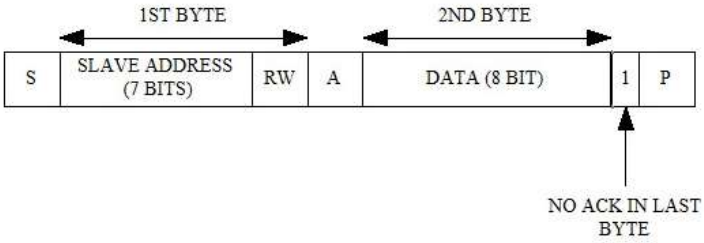

Fig.3.4 Slave-transmitter transmits to master-receiver

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by **PS5260**. The 8 bits data was read from **PS5260** internal control register that address was assigned by previous write cycle. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (**PS5260**) must releases SDA line to master to generate STOP condition.

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I²C™ Bus Timing

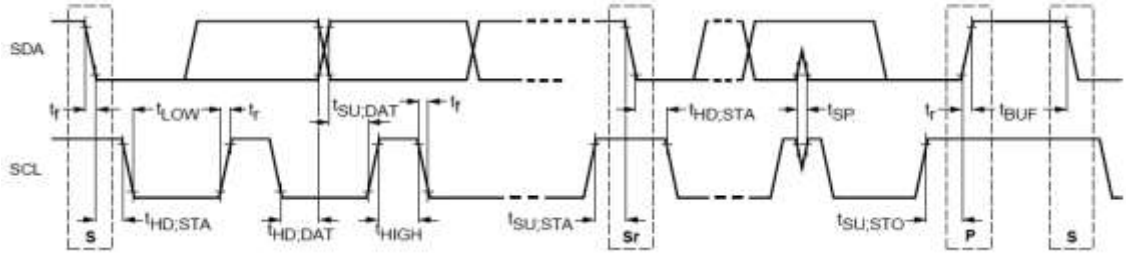

Fig.3.5 Definition of timing for F/S mode devices on the I2C-bus

I²C™ Bus Timing Specification						
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency.	f_{scl}	10	100	0	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	0.6	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	1.3	-	µs
High period of the SCL clock.	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	5.0	3.45	0	0.9	µs
Data set-up time.	$t_{SU;DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals.	t_r	-	1000	-	300	ns (note l)
Fall time of both SDA and SCL signals.	t_f	-	300	-	300	ns (note l)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line.	C_b	-	400	-	400	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-		0.1 VDD	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-		0.2 VDD	V

Note: It depends on the “high” period time of SCL.

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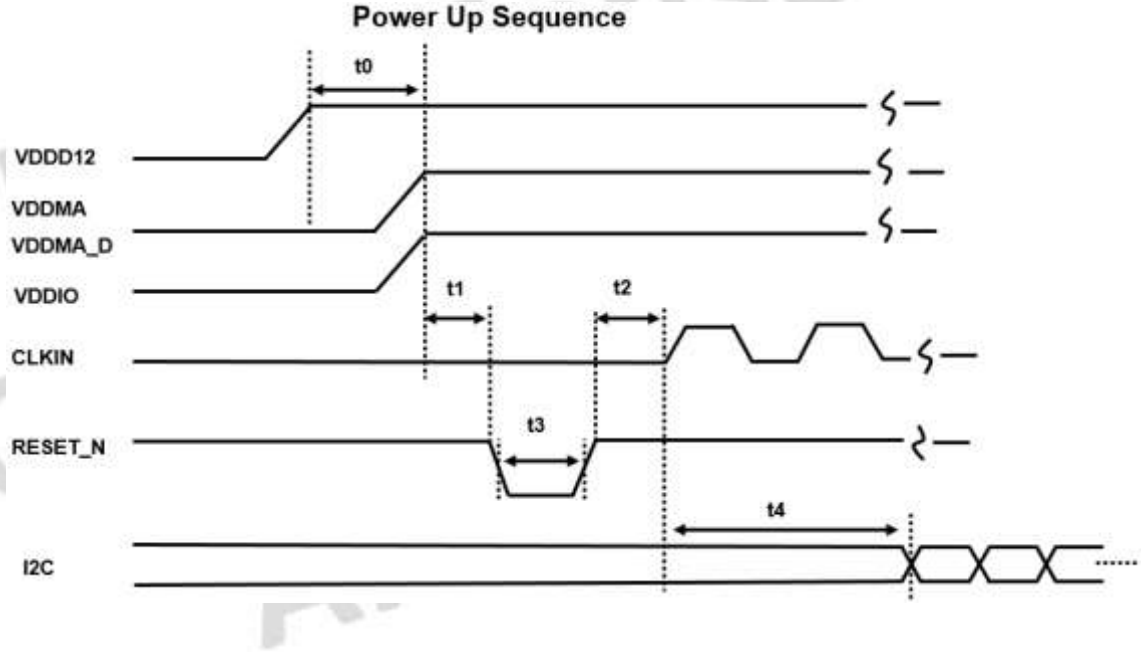
4. Power Sequence

Power-Up Sequence

The recommended power-up sequence for the PS5260 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn on VDDD12 power supply.
2. After 100µs (t0), VDDMA, VDDMA_D and VDDIO power supply simultaneously.
3. After 100µs (t1), RESET_N must go low.
4. RESET_N active low for at least 1ms (t3).
5. After 100µs (t2), enable CLKIN.
6. Wait at least 1ms (t4), I2C starts to write commands.



Power-Down Sequence

The recommended power-down sequence for the PS5260 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn off VDDMA, VDDMA_D and VDDIO power supply simultaneously.
2. After 100µs (t0), turn off VDDD12 power supply.

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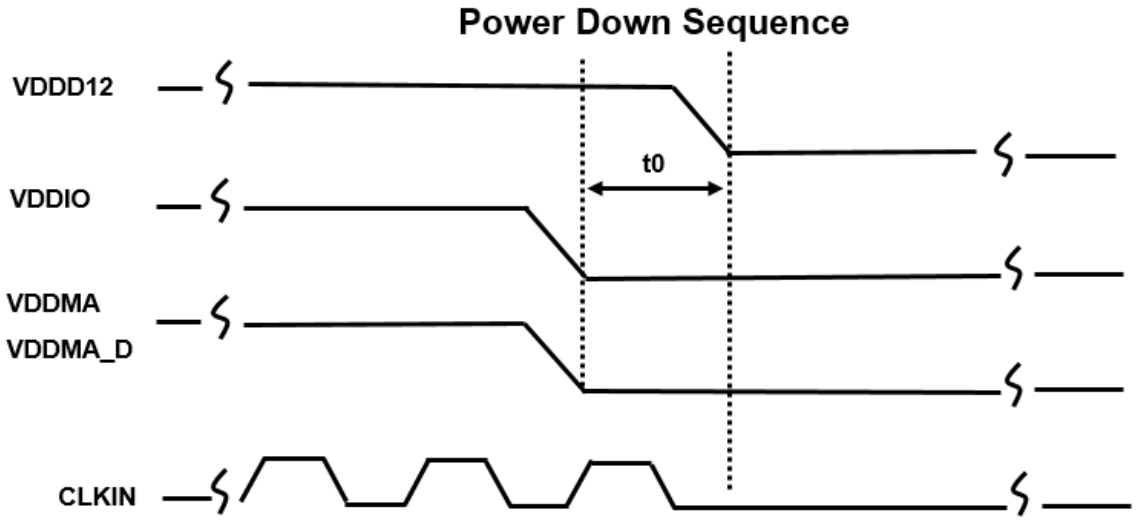


CSB Suspend Sequence

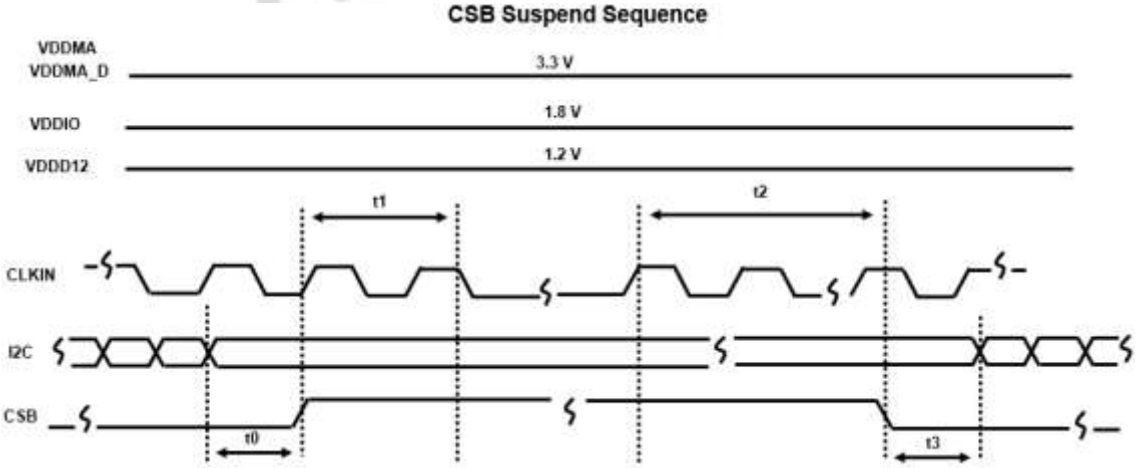
The recommended CSB Suspend sequence for the PS5260 is shown as the following figure. The available power supplies must have the separation specified below.

ON → OFF :

1. I2C must write commands to turn off internal clock for PS5260 .
2. After 100µs (t0), CSB must go high
3. After 100µs (t1), turn off CLKIN.

OFF → ON :

1. Turn on CLKIN.
2. After 100µs (t2), CSB must go low.
3. Wait at least 1ms (t3) for internal clock stable.
4. I2C starts to write commands.



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5. Register Table

Bank	Address		Bit	Name	R/W	Description
	Hex	Dec				
0	00	00	[7:0]	PartID[15:8]	R	Sensor ID
0	01	01	[7:0]	PartID[7:0]	R	Sensor ID
0	02	02	[3:0]	VersionID[3:0]	R	Sensor ID
0	03	03	[3:0]	SubID[3:0]	R	Sensor ID
0	11	17	[7]	Cmd_GatedAllClk	R/W	Clock Gated Control (1: Gate Clock)
0	BE	190	[6]	Cmd_Pxclk_Inv	R/W	Invert Pxclk Out
			[5]	Cmd_Vsync_Inv	R/W	Invert Vsync Out
			[4]	Cmd_Hsync_Inv	R/W	Invert Hsync Out
1	04	04	[6:4]	R_PxclkO_dly[2:0]	R/W	Timing Delay for Pxclk
			[2:0]	R_HsyncO_dly[2:0]	R/W	Timing Delay for Hsync
1	05	05	[6:4]	R_VsyncO_dly[2:0]	R/W	Timing Delay for Vsync
			[3]	Cmd_10_TriState	R/W	TriState IO of PxData[1:0]
			[2]	Cmd_Sw_PwrDn	R/W	Power-Down Control
			[1]	Cmd_Sw_TriState	R/W	TriState IO of PxData, Hsync, Vsync, and Pxclk
1	09	09	[0]	UpdateFlag	R/W	Exposure & Gain Update Control (Write 0x01)
1	0A	10	[7:0]	Cmd_Lpf [15:8]	R/W	Line per frame = Cmd_Lpf+ 1
1	0B	11	[7:0]	Cmd_Lpf [7:0]	R/W	Line per frame = Cmd_Lpf+ 1
1	0C	12	[7:0]	Cmd_OffNy1[15:8]	R/W	Exposure Control
1	0D	13	[7:0]	Cmd_OffNy1[7:0]	R/W	Exposure Control
1	0E	14	[4:0]	Cmd_OffNe1[12:8]	R/W	Exposure Control
1	0F	15	[7:0]	Cmd_OffNe1[7:0]	R/W	Exposure Control
1	18	24	[0]	Cmd_SGHD	R/W	High/Low Sensitivity Selection : 0: High Sensitivity Mode 1: Low Sensitivity Mode
1	1B	27	[7]	Cmd_Hflip	R/W	Horizontal Flip
			[6:5]	Cmd_Askip_H[1:0]	R/W	Horizontal Skip
			[2:0]	Cmd_Hsize_e1[10:8]	R/W	Raw Image Horizontal Size
1	1C	28	[7:0]	Cmd_Hsize_e1[7:0]	R/W	Raw Image Horizontal Size
1	1D	29	[7]	Cmd_Vflip	R/W	Vertical Flip
			[6:5]	Cmd_Askip_V[1:0]	R/W	Vertical Skip

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			[2:0]	Cmd_Vsize[10:8]	R/W	Raw Image Vertical Size
1	1E	30	[7:0]	Cmd_Vsize[7:0]	R/W	Raw Image Vertical Size
1	1F	31	[2:0]	Cmd_Vstart[10:8]	R/W	Raw Image Vertical Offset
1	20	32	[7:0]	Cmd_VStart[7:0]	R/W	Raw Image Vertical Offset
1	27	39	[4:0]	Cmd_LineTime [12:8]	R/W	Line Time = Cmd_LineTime* 0.5 clock cycles
1	28	40	[7:0]	Cmd_LineTime [7:0]	R/W	Line Time = Cmd_LineTime* 0.5 clock cycles
1	80	128	[7:0]	Cmd_DG_gain_idx[7:0]	R/W	Sensor Digital Gain index
1	83	131	[7:0]	Cmd_gain_idx[7:0]	R/W	Sensor Analog Gain index
1	8F	143	[3]	R_ImgSyn_SGHD_EnH	R/W	When Cmd_ImgSyn_EnH =1, 0: HDR Image don't use SGHD 1: HDR Image use SGHD
			[2]	Cmd_ImgSyn_Mode	R/W	HDR Image Mode : 0: anglog nonHDR-mode 1: analog HDR-mode
			[0]	Cmd_ImgSyn_EnH	R/W	HDR Image Synthesis Enable
1	90	144	[0]	Cmd_Adc_sample_posedge	R/W	ADC sample timing control
1	92	146	[4:0]	R_ISP_TestMode[4:0]	R/W	Test Image Control
1	93	147	[7:0]	R_ISP_TestValueLo[7:0]	R/W	Test Image Control
1	94	148	[7:0]	R_ISP_TestValueHi[7:0]	R/W	Test Image Control
1	97	151	[0]	Cmd_Pga_D1frm	R/W	Pga Gain auto-delay one frame
1	A3	163	[4]	Cmd_WOI_VOffset_sign	R/W	Vertical offset of output image
			[2:0]	Cmd_WOI_VOffset[10:8]	R/W	Vertical offset of output image
1	A4	164	[7:0]	Cmd_WOI_VOffset[7:0]	R/W	Vertical offset of output image
1	A5	165	[2:0]	Cmd_WOI_VSize[10:8]	R/W	Vertical size of output image
1	A6	166	[7:0]	Cmd_WOI_VSize[7:0]	R/W	Vertical size of output image
1	A7	167	[4]	Cmd_WOI_HOffset_sign	R/W	Horizontal offset of output image
			[2:0]	Cmd_WOI_HOffset[10:8]	R/W	Horizontal offset of output image
1	A8	168	[7:0]	Cmd_WOI_HOffset[7:0]	R/W	Horizontal offset of output image
1	A9	169	[2:0]	Cmd_WOI_HSize[10:8]	R/W	Horizontal size of output image
1	AA	170	[7:0]	Cmd_WOI_HSize[7:0]	R/W	Horizontal size of output image
1	AB	171	[3:0]	Cmd_Np[3:0]	R/W	Frequency eliminate control
1	E3	227	[5]	T_SR_GPIO	R/W	IO slew control
			[1:0]	T_OPDRV_GPIO[1:0]	R/W	IO driving Strength
1	F1	241	[5:0]	T_spll_predivider[5:0]	R/W	PLL Control
1	F2	242	[5:0]	T_spll_postdivider [5:0]	R/W	PLL Control
1	F5	245	[1:0]	T_spll_modedivider [1:0]	R/W	PLL Control

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2	10	16	[1]	R_FrameSyncWait	R/W	0: Continuous output after one pulse trigger signal. 1: One frame output after one pulse trigger signal.
			[0]	R_FrameSyncMode	R/W	0: Normal Mode. 1: Frame Sync Mode.
2	46	70	[7]	Cmd_DigDac_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	47	71	[7:0]	Cmd_DigDac_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	48	72	[7]	Cmd_DigDac_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[2:0]	Cmd_DigDac_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel
2	49	73	[7:0]	Cmd_DigDac_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	4A	74	[7]	Cmd_DigDac_Gr_Sign	R/W	Black Level Offset for Gr Channel
			[2:0]	Cmd_DigDac_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	4B	75	[7:0]	Cmd_DigDac_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	4C	76	[7]	Cmd_DigDac_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	4D	77	[7:0]	Cmd_DigDac_R_Offset[7:0]	R/W	Black Level Offset for R Channel
2	A0	160	[7]	Cmd_DigDac2_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac2_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	A1	161	[7:0]	Cmd_DigDac2_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	A2	162	[7]	Cmd_DigDac2_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[2:0]	Cmd_DigDac2_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel
2	A3	163	[7:0]	Cmd_DigDac2_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	A4	164	[7]	Cmd_DigDac2_Gr_Sign	R/W	Black Level Offset for Gr Channel
			[2:0]	Cmd_DigDac2_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	A5	165	[7:0]	Cmd_DigDac2_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	A6	166	[7]	Cmd_DigDac2_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac2_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	A7	167	[7:0]	Cmd_DigDac2_R_Offset[7:0]	R/W	Black Level Offset for R Channel

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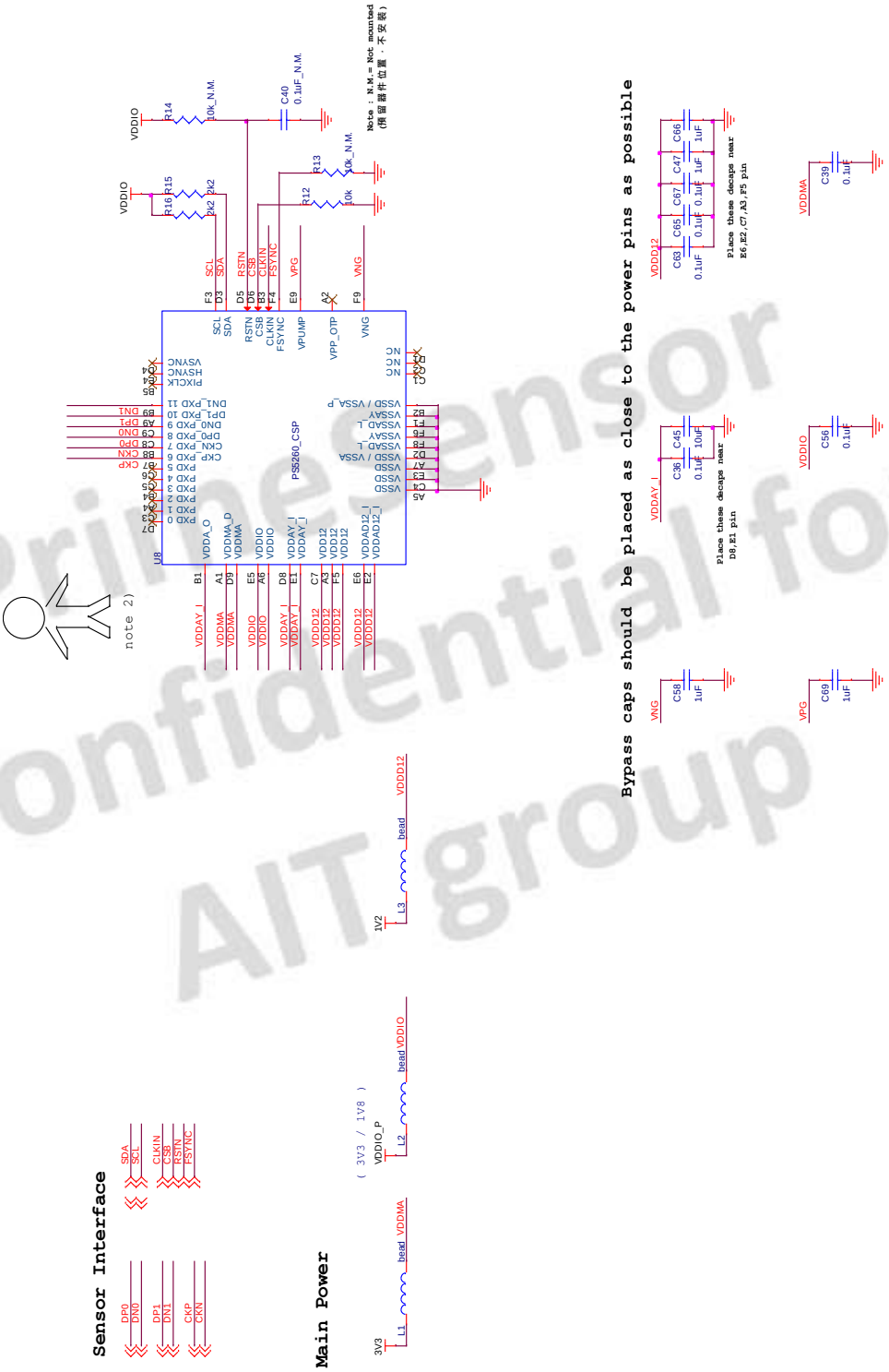
6. Reference Circuit Schematic

MIPI Interface:



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Parallel Interface:

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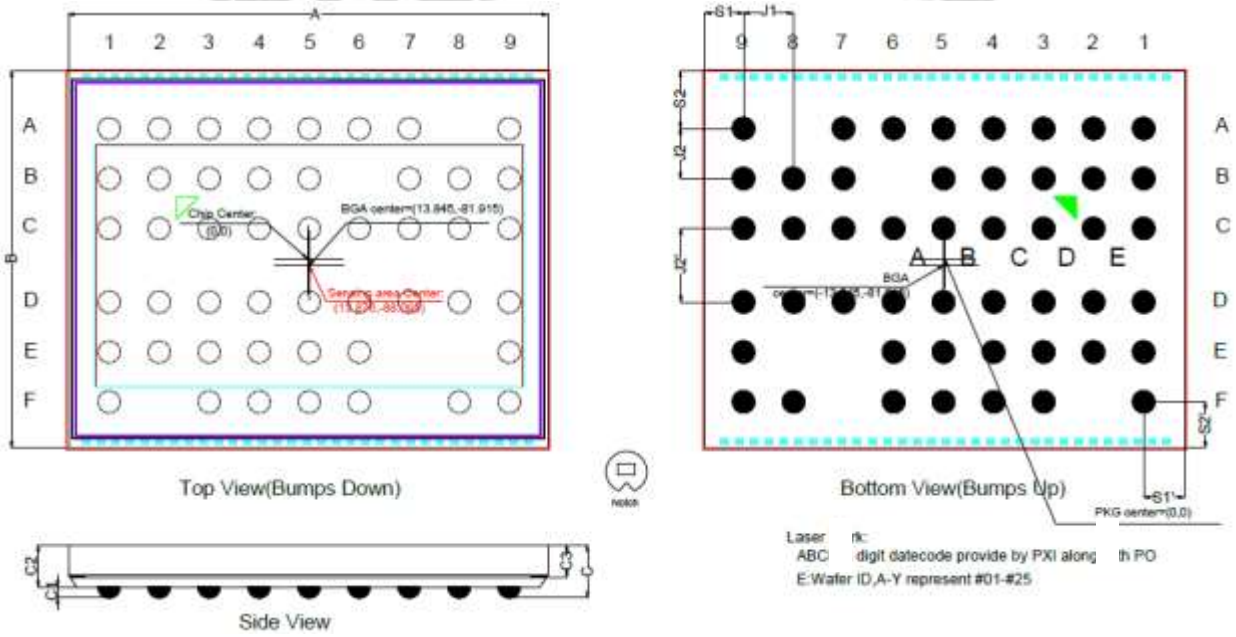
7. Package Information

- **Package Outline Dimension**

	Symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	6.519	6.494	6.544
Package Body Dimension Y	B	5.126	5.101	5.151
Package Height	C	0.790	0.730	0.850
Ball Height	C1	0.160	0.130	0.190
Package Body Thickness	C2	0.630	0.595	0.665
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465
Ball Diameter	D	0.300	0.270	0.330
Total Ball Count	N	48(3NC)		
Pins pitch X axis	J1	0.680		
Pins pitch Y axis	J2	0.680		
Pins pitch Y' axis	J2'	1.000		
Edge to Pin Center Distance along X	S1	0.525655	0.495655	0.555655
Edge to Pin Center Distance along Y	S2	0.784915	0.754915	0.814915
Edge to Pin Center Distance along X'	S1'	0.553345	0.523345	0.583345
Edge to Pin Center Distance along Y'	S2'	0.621085	0.591085	0.651085



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- **Recommended PCB Layout**

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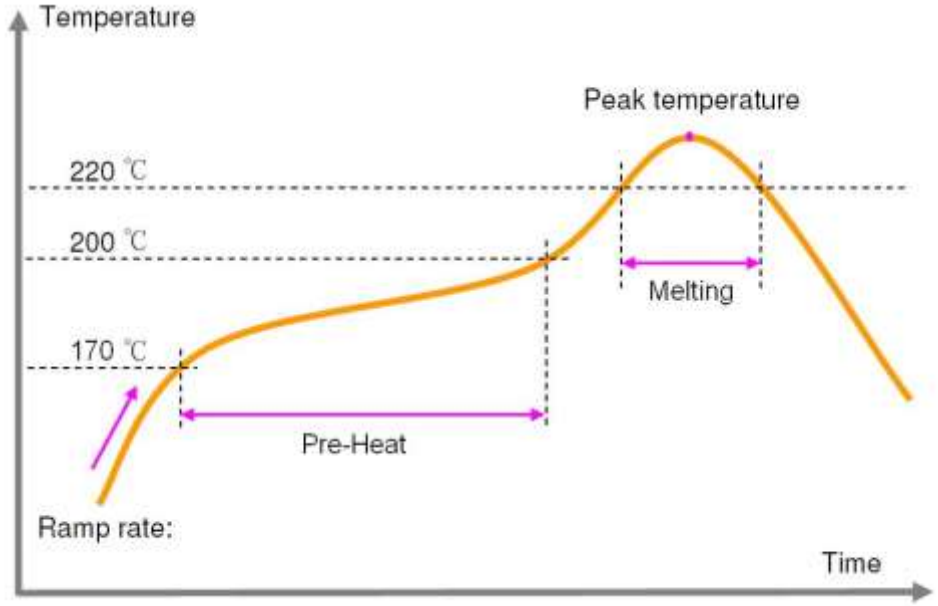
- **Recommended Guideline for PCB Assembly**

I. Recommended vender and type for Pb-free solder paste
   1 Almit LFM-48W TM-HP
   2 Senju M705-GRN360-K

II. IR Reflow Soldering Profile:

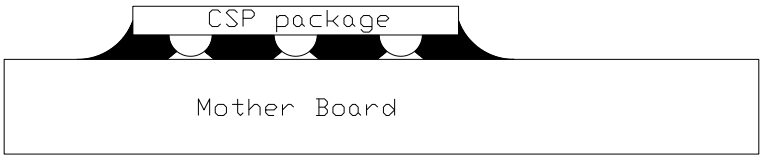
Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.



- **Reflow Profile**
  1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
  2. Preheat zone:
     2.1 Temp ramp from 170~ 200 degree C
     2.2 Exposure time: 90 +/- 30 sec
  3. Melting zone:
     3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
     3.2 Peak temperature: 245 degree C.

III. Others

- **Epoxy under-filled process is required post IC mounting process.**



- **Peek tweezers or plastic tweezers is required post IC manual handling for pick and place.**

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8. Revision History

Revision	Description	Date
V0.1	Preliminary data sheet released	May 9, 2018
V0.2	Correct DVP output interface from 10bit to 12bit	May 18, 2018

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