1Mb Low Power SRAM
M-die Specification

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Document Title
64Kx16 & 128Kx8 Bit Low Power SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Nov. 2015	Preliminary
0.1	Add typical I_{DR} value	Dec. 2015	Preliminary

1.0	Final version release
	Split Icc1 spec value depending on Vcc
	  ; 2.3~3.6V : 3mA
	  ; 4.5~5.5V : 4mA
	Add 32SOP and 32TSOP2
		Feb. 2016	Final

1.1	Add commercial temperature range	Apr. 2016	Final
1.2	Correct TSOP pin shape in PKG Dimensioin	Apr. 2017	Final
1.3	Correct Typo	Dec. 2018	Final

64Kx16 & 128Kx8 Bit Low Power SRAM

Features

- Fast Access Time : 45, 55, 70ns(Max.)
- CMOS Low Power Dissipation
  Standby Current (Typical) : 2μA
                  (Maximum) : 10μA
  Operating Current (Typical)   : 15mA (tAA=55ns)
                  (Maximum) : 20mA (tAA=55ns)
- Wide range or Single 5.0V Power Supply
  - S6L10xxW : 2.3V ~ 3.6V Vcc
  - S6L10xxC : 4.5V ~ 5.5V Vcc
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control (x16 Mode)
  $\overline{LB}$: I/O0~ I/O7, $\overline{UB}$: I/O8~ I/O15
- Standard 32SOP, 32TSOP1, 32sTSOP1, 32TSOP2,
  44TSOP2, 48FBGA Package Pin Configuration
- ROHS compliant
- Operating in Commercial and Industrial Temperature range.
- 2CS Option Available

General Description

The S6L1016(W/C) and S6L1008(W/C) are a 1,048,576-bit high-speed Static Random Access Memory organized as 64K (128K) words by 16(8) bits. S6L1016(W/C) allows that lower and upper byte access by data byte control($\overline{UB}$, $\overline{LB}$). The device is fabricated using advanced CMOS process,6-TR based cell technology and designed for low power circuit technology. It is particularly well suited for use in battery back up application for low data retention current.

The S6L1016(W/C) is packaged in a 44TSOP2 and 48FBGA. The S6L1008(W/C) is packaged in a 32SOP, 32TSOP1, 32sTSOP1 and 32TSOP2.

1Mb Low Power SRAM Ordering Information (64Kx16) - 1CS

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
1Mb	64Kx16	S6L1016W1M-UC(I)45	2.5, 3.3	45	20	44 TSOP2	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L1016W1M-UC(I)55	2.5, 3.3	55	25	44 TSOP2	
		S6L1016W1M-UC(I)70	2.5, 3.3	70	35	44 TSOP2	
		S6L1016C1M-UC(I)45	5.0	45	20	44 TSOP2	
		S6L1016C1M-UC(I)55	5.0	55	25	44 TSOP2	
		S6L1016C1M-UC(I)70	5.0	70	35	44 TSOP2	
		S6L1016W1M-XC(I)45	2.5, 3.3	45	20	48 FBGA	
		S6L1016W1M-XC(I)55	2.5, 3.3	55	25	48 FBGA	
		S6L1016W1M-XC(I)70	2.5, 3.3	70	35	48 FBGA	
		S6L1016C1M-XC(I)45	5.0	45	20	48 FBGA	
		S6L1016C1M-XC(I)55	5.0	55	25	48 FBGA	
		S6L1016C1M-XC(I)70	5.0	70	35	48 FBGA	

1Mb Low Power SRAM Ordering Information (64Kx16) - 2CS

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
1Mb	64Kx16	S6L1016W2M-XC(I)45	2.5, 3.3	45	20	48 FBGA	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L1016W2M-XC(I)55	2.5, 3.3	55	25	48 FBGA	
		S6L1016W2M-XC(I)70	2.5, 3.3	70	35	48 FBGA	
		S6L1016C2M-XC(I)45	5.0	45	20	48 FBGA	
		S6L1016C2M-XC(I)55	5.0	55	25	48 FBGA	
		S6L1016C2M-XC(I)70	5.0	70	35	48 FBGA	

1Mb Low Power SRAM Ordering Information (128Kx8) - 2CS

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
1Mb	128Kx8	S6L1008W2M-BC(I)45	2.5, 3.3	45	20	32 SOP	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L1008W2M-BC(I)55	2.5, 3.3	55	25	32 SOP	
		S6L1008W2M-BC(I)70	2.5, 3.3	70	35	32 SOP	
		S6L1008C2M-BC(I)45	5.0	45	20	32 SOP	
		S6L1008C2M-BC(I)55	5.0	55	25	32 SOP	
		S6L1008C2M-BC(I)70	5.0	70	35	32 SOP	
		S6L1008W2M-TC(I)45	2.5, 3.3	45	20	32 TSOP1	
		S6L1008W2M-TC(I)55	2.5, 3.3	55	25	32 TSOP1	
		S6L1008W2M-TC(I)70	2.5, 3.3	70	35	32 TSOP1	
		S6L1008C2M-TC(I)45	5.0	45	20	32 TSOP1	
		S6L1008C2M-TC(I)55	5.0	55	25	32 TSOP1	
		S6L1008C2M-TC(I)70	5.0	70	35	32 TSOP1	
		S6L1008W2M-LC(I)45	2.5, 3.3	45	20	32 sTSOP1	
		S6L1008W2M-LC(I)55	2.5, 3.3	55	25	32 sTSOP1	
		S6L1008W2M-LC(I)70	2.5, 3.3	70	35	32 sTSOP1	
		S6L1008C2M-LC(I)45	5.0	45	20	32 sTSOP1	
		S6L1008C2M-LC(I)55	5.0	55	25	32 sTSOP1	
		S6L1008C2M-LC(I)70	5.0	70	35	32 sTSOP1	
		S6L1008W2M-NC(I)45	2.5, 3.3	45	20	32TSOP2	
		S6L1008W2M-NC(I)55	2.5, 3.3	55	25	32TSOP2	
		S6L1008W2M-NC(I)70	2.5, 3.3	70	35	32TSOP2	
		S6L1008C2M-NC(I)45	5.0	45	20	32TSOP2	
		S6L1008C2M-NC(I)55	5.0	55	25	32TSOP2	
		S6L1008C2M-NC(I)70	5.0	70	35	32TSOP2	

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Logic Block Diagram - 64K x 16
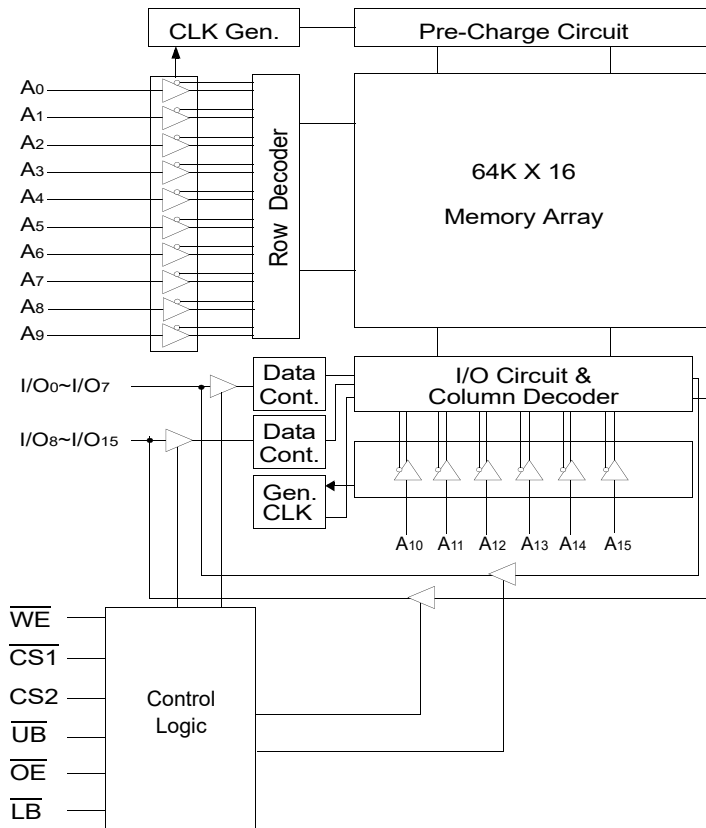
Logic Block Diagram - 128K x 8
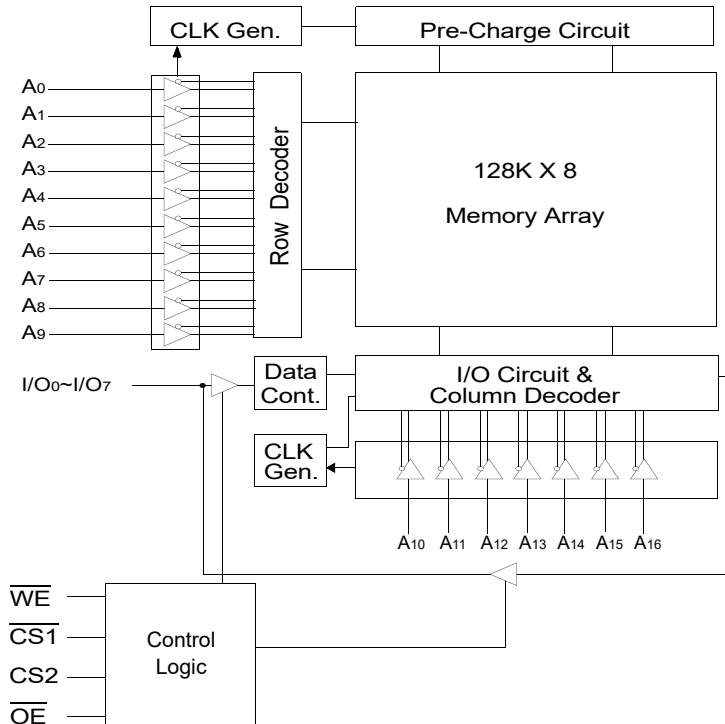
44 TSOP2 Package Pin Configurations(Top View) - S6L1016(W/C)1M (64K x 16) - 1CS
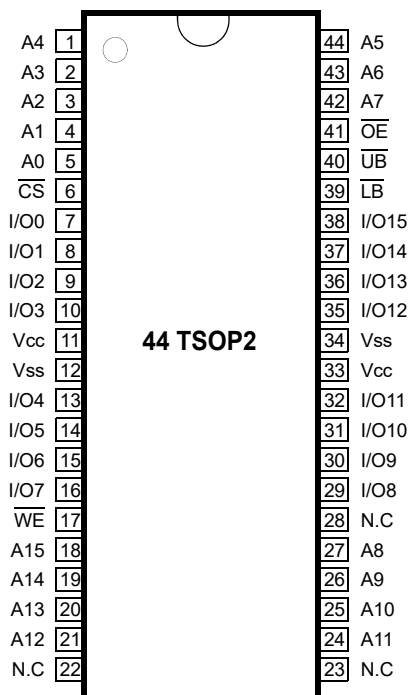
A4	1	44	A5
A3	2	43	A6
A2	3	42	A7
A1	4	41	$\overline{OE}$
A0	5	40	$\overline{UB}$
$\overline{CS}$	6	39	$\overline{LB}$
I/O0	7	38	I/O15
I/O1	8	37	I/O14
I/O2	9	36	I/O13
I/O3	10	35	I/O12
Vcc	11	34	Vss
Vss	12	33	Vcc
I/O4	13	32	I/O11
I/O5	14	31	I/O10
I/O6	15	30	I/O9
I/O7	16	29	I/O8
$\overline{WE}$	17	28	N.C
A15	18	27	A8
A14	19	26	A9
A13	20	25	A10
A12	21	24	A11
N.C	22	23	N.C

44 TSOP2

Pin Function

Pin Name	Pin Function
A_0 - A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-byte Control(I/O$_0$~I/O$_7$)
$\overline{UB}$	Upper-byte Control(I/O$_8$~I/O$_{15}$)
I/O$_0$ ~ I/O$_{15}$	Data Inputs/Outputs
VCC	Power
VSS	Ground
N.C	No Connection

48FBGA - S6L1016(W/C)1M (64K x 16) - 1CS - Top View

PKG Pin Configurations

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O8	$\overline{UB}$	A3	A4	$\overline{CS}$	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	VSS	I/O11	NC	A7	I/O3	VCC
E	VCC	I/O12	NC	NC	I/O4	VSS
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	$\overline{WE}$	I/O7
H	NC	A8	A9	A10	A11	NC

Pin Function

Pin Name	Pin Function
A_0 - A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-byte Control(I/O$_0$~I/O$_7$)
$\overline{UB}$	Upper-byte Control(I/O$_8$~I/O$_{15}$)
I/O$_0$ ~ I/O$_{15}$	Data Inputs/Outputs
VCC	Power
VSS	Ground
N.C	No Connection

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48FBGA - S6L1016(W/C)2M (64K x 16) - 2CS - Top View

PKG Pin Configurations

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CS2
B	I/O8	$\overline{UB}$	A3	A4	$\overline{CS1}$	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	Vss	I/O11	NC	A7	I/O3	Vcc
E	Vcc	I/O12	NC	NC	I/O4	Vss
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	$\overline{WE}$	I/O7
H	NC	A8	A9	A10	A11	NC
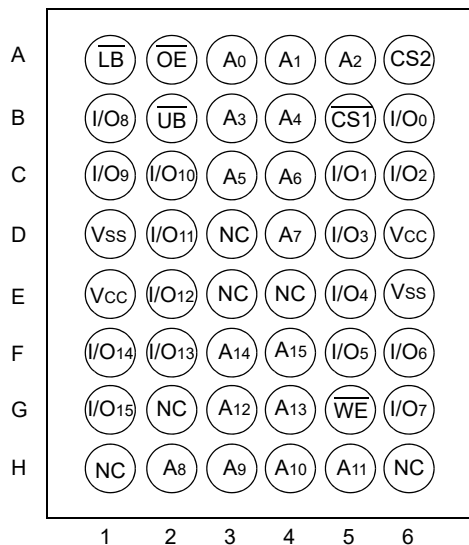
Pin Function

Pin Name	Pin Function
A0 - A15	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$	Chip Select Input1
CS2	Chip Select Input2
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-byte Control(I/O0~I/O7)
$\overline{UB}$	Upper-byte Control(I/O8~I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

32 TSOP1 and 32 sTSOP1 Package(Top View) - S6L1008(W/C)2M (128K x 8) - 2CS
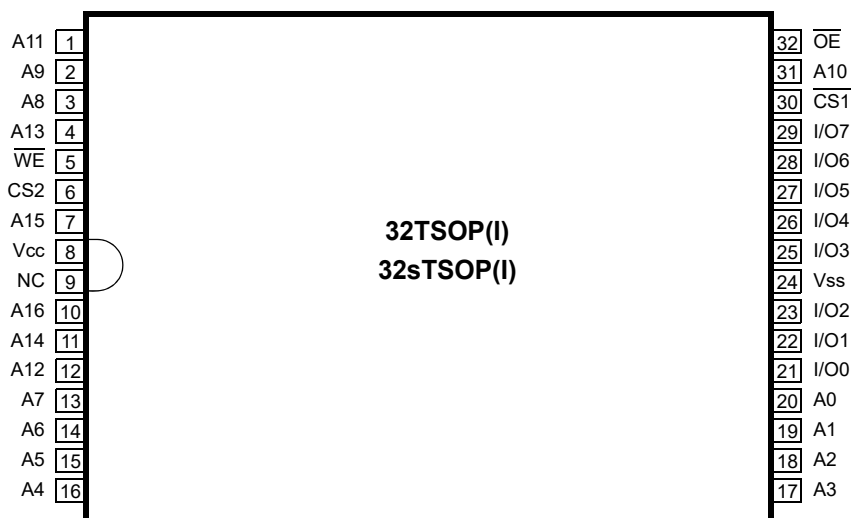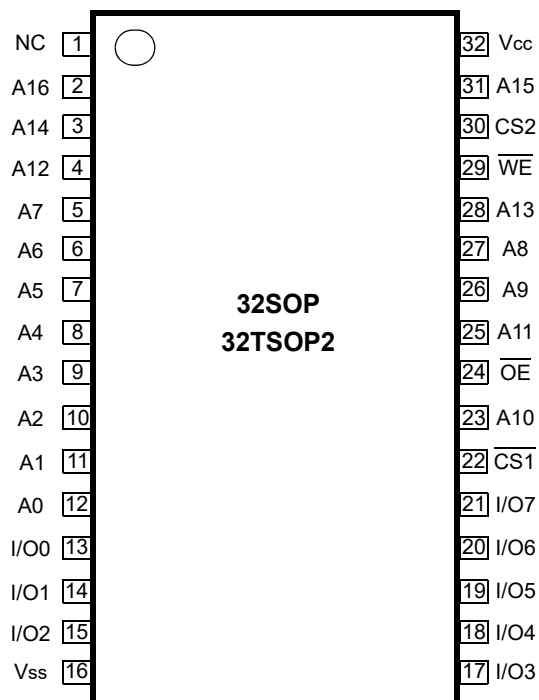
PKG Pin Configurations

Left	Pin		Pin	Right
A11	1		32	$\overline{OE}$
A9	2		31	A10
A8	3		30	$\overline{CS1}$
A13	4		29	I/O7
$\overline{WE}$	5		28	I/O6
CS2	6		27	I/O5
A15	7		26	I/O4
Vcc	8	32TSOP(I)	25	I/O3
NC	9	32sTSOP(I)	24	Vss
A16	10		23	I/O2
A14	11		22	I/O1
A12	12		21	I/O0
A7	13		20	A0
A6	14		19	A1
A5	15		18	A2
A4	16		17	A3

Pin Function

Pin Name	Pin Function
A0 - A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$	Chip Select1
CS2	Chip Select2
$\overline{OE}$	Output Enable
I/O0 ~ I/O7	Data Inputs/Outputs
Vcc	Power
Vss	Ground

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32 SOP and 32 TSOP2 Package(Top View) **- S6L1008(W/C)2M (128K x 8) - 2CS**

PKG Pin Configurations

NC	1	32	Vcc
A16	2	31	A15
A14	3	30	CS2
A12	4	29	$\overline{WE}$
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CS1}$
A0	12	21	I/O7
I/O0	13	20	I/O6
I/O1	14	19	I/O5
I/O2	15	18	I/O4
Vss	16	17	I/O3

32SOP
32TSOP2

Pin Function

Pin Name	Pin Function
A_0 - A_{16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$	Chip Select1
CS2	Chip Select2
$\overline{OE}$	Output Enable
I/O_0 ~ I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground

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Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin relative to V_{SS}		V_{IN}, V_{OUT}	-0.5 to Vcc+0.5V	V
Voltage on Vcc Supply Relative to V_{SS}	Wide Vcc** Product	V_{IN}, V_{OUT}	-0.5 to 4.6	V
	5.0V Product		-0.5 to 7.0	
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to +150	°C
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** Wide Vcc range is 2.3V ~ 3.6V.

Recommended DC Operating Conditions (TA= -40 to 85°C)

Parameter	Operating Vcc(V)	Symbol	Min	Typ	Max	Unit
Supply Voltage	5.0	V_{CC}	4.5	5.0	5.5	V
	Wide 2.3 ~ 3.6	V_{CC}	2.3	2.5/3.3	3.6	
Ground		V_{SS}	0	0	0	V
Input High Voltage	5.0	V_{IH}	2.2	-	Vcc+0.5	V
	Wide 2.3 ~ 2.7	V_{IH}	1.8	-	Vcc+0.3	
	Wide 2.7 ~ 3.6	V_{IH}	2.2	-	Vcc+0.3	
Input Low Voltage	5.0	V_{IL}	-0.3	-	0.8	V
	Wide 2.3 ~ 2.7	V_{IL}	-0.3	-	0.6	
	Wide 2.7 ~ 3.6	V_{IL}	-0.3	-	0.8	

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DC and Operating Characteristics (TA= -40 to 85°C)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}		-1	-	1	μA
Operating Current	I_{CC}	f=fmax,Vcc=Vccmax, I_{OUT}=0mA, V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V	45ns	-	-	20	mA
			55ns	-	-	20	
			70ns	-	-	15	
	I_{CC1}	f=1MHz, Vcc=Vccmax, I_{OUT}=0mA, V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V	Vcc=2.3~3.6V	-	-	3	mA
			Vcc=4.5~5.5V	-	-	4	
Standby Current	I_{SB} (TTL)	Vcc=Vccmax, CS2=V_{IL}, Others=V_{IH} or V_{IL}	2CS	-	-	0.3	mA
		Vcc=Vccmax, $\overline{CS1}$=V_{IH}, Others=V_{IH} or V_{IL}	1CS				
	I_{SB1} (CMOS)	Vcc=Vccmax, V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V, 1) CS2≤0.2V, or 2) CS2≥Vcc-0.2V, $\overline{CS1}$≥Vcc-0.2V, or 3)CS2≥Vcc-0.2V, CS1≤0.2V, UB=LB≥Vcc-0.2V	2CS	-	2	10	μA
		Vcc=Vccmax, V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V, 1) $\overline{CS}$≥Vcc-0.2V, or 2) $\overline{CS}$≤0.2V, UB=LB≥Vcc-0.2V	1CS				
Output Low Voltage Level	V_{OL}	Vcc=4.5V, I_{OL}=2.1mA, 5.0V Product		-	-	0.4	V
		Vcc=2.7V, I_{OL}=2.1mA, Wide Vcc* Product		-	-	0.4	
		Vcc=2.3V, I_{OL}=2.1mA, Wide Vcc* Product		-	-	0.4	
Output High Voltage Level	V_{OH}	Vcc=4.5V, I_{OH}=-1mA, 5.0V Product		2.4	-	-	V
		Vcc=2.7V, I_{OH}=-1mA, Wide Vcc* Product		2.4	-	-	
		Vcc=2.3V, I_{OH}=-1mA, Wide Vcc* Product		1.8	-	-	

Note : Typical parameters indicates the value for the center of distribution at Vcc=3.0V and Ta=25°C, and not 100% tested.
* Wide Vcc range is 2.3V ~ 3.6V.

Capacitance*(TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	TYP	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* Capacitance is sampled and not 100% tested.

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Functional Description (x8 Mode) - 2CS

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* X means Don't Care.

Functional Description (x16 Mode) - 1CS

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O Pin		Mode	Supply Current
					I/O$_0$~I/O$_7$	I/O$_8$~I/O$_{15}$		
H	X*	X	X	X	High-Z	High-Z	Not Select	I_{SB}, I_{SB1}
X	X	X	H	H	High-Z	High-Z	Not Select	I_{SB}, I_{SB1}
L	H	H	L	X	High-Z	High-Z	Output disable	I_{CC}
L	H	H	X	L	High-Z	High-Z	Output disable	I_{CC}
L	H	L	L	H	D_{OUT}	High-Z	Lower Byte Read	I_{CC}
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read	I_{CC}
L	H	L	L	L	D_{OUT}	D_{OUT}	Word Read	I_{CC}
L	L	X	L	H	D_{IN}	High-Z	Lower Byte Write	I_{CC}
L	L	X	H	L	High-Z	D_{IN}	Upper Byte Write	I_{CC}
L	L	X	L	L	D_{IN}	D_{IN}	Word Write	I_{CC}

* X means Don't Care.

Functional Description (x16 Mode) - 2CS

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O Pin		Mode	Supply Current
						I/O$_0$~I/O$_7$	I/O$_8$~I/O$_{15}$		
H	X*	X	X	X	X	High-Z	High-Z	Not Select	I_{SB}, I_{SB1}
X	L	X	X	X	X	High-Z	High-Z	Not Select	I_{SB}, I_{SB1}
X	X	X	X	H	H	High-Z	High-Z	Not Select	I_{SB}, I_{SB1}
L	H	H	H	L	X	High-Z	High-Z	Output disable	I_{CC}
L	H	H	H	X	L	High-Z	High-Z	Output disable	I_{CC}
L	H	H	L	L	H	D_{OUT}	High-Z	Lower Byte Read	I_{CC}
L	H	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read	I_{CC}
L	H	H	L	L	L	D_{OUT}	D_{OUT}	Word Read	I_{CC}
L	H	L	X	L	H	D_{IN}	High-Z	Lower Byte Write	I_{CC}
L	H	L	X	H	L	High-Z	D_{IN}	Upper Byte Write	I_{CC}
L	H	L	X	L	L	D_{IN}	D_{IN}	Word Write	I_{CC}

* X means Don't Care.

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Data Retention Characteristics (TA= -40 to 85°C)

Parameter	Symbol	Test Condition		Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	Refer to Data Retention Waveform		1.5	-	-	V
Data Retention Current	I_{DR}	V_{CC}=1.5V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V 1) CS2≤0.2V, or 2) CS2≥V_{CC}-0.2V, $\overline{CS1}$≥V_{CC}-0.2V, or 3) CS2≥V_{CC}-0.2V, $\overline{CS1}$≤0.2V, $\overline{UB}$=$\overline{LB}$≥V_{CC}-0.2V	2CS	-	2	10	μA
		V_{CC}=1.5V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V 1) $\overline{CS}$≥V_{CC}-0.2V, or 2) $\overline{CS}$≤0.2V, $\overline{UB}$=$\overline{LB}$≥V_{CC}-0.2V	1CS				
Data Retention Set-Up Time	t_{SDR}	Refer to Data Retention Waveform		0	-	-	ns
Recovery Time	t_{RDR}			t_{RC}	-	-	ns

Data Retention Wave Form (1) - $\overline{CS1}$ Controlled
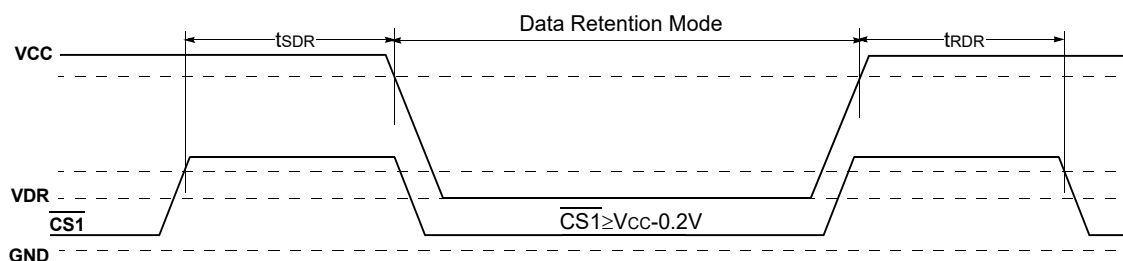
Data Retention Wave Form (2) - CS2 controlled
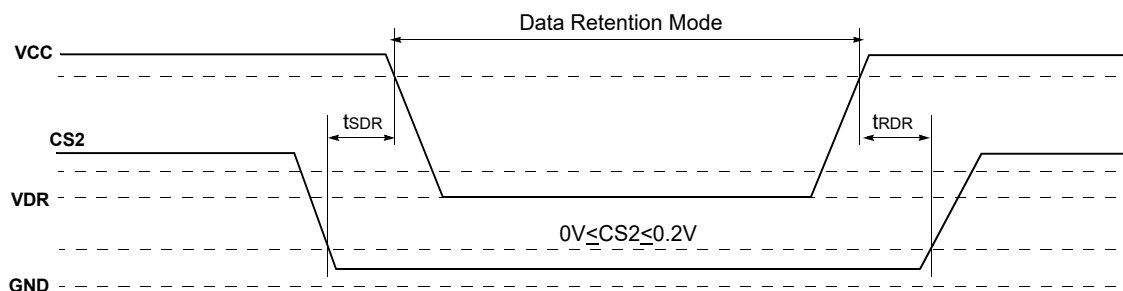
Data Retention Wave Form (3) - $\overline{UB}$, $\overline{LB}$ Controlled
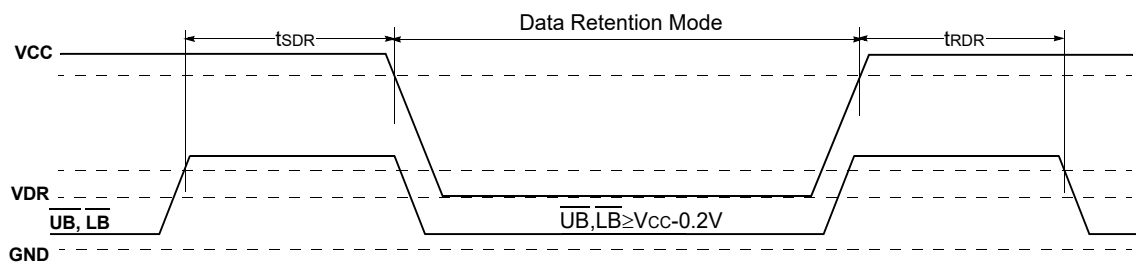
AC Test Conditions

Parameter	Value
Input Pulse Level	0 to 3.0V (Vcc=3.3V or 5.0V)
	0 to 2.5V (Vcc=2.5V)
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V (Vcc=3.3V or 5.0V)
	1/2Vcc (Vcc=2.5V)
Output Load	CL=30pF + 1TTL, I_{OH}/I_{OL}=-1mA/2.1mA

Read Cycle (TA= -40 to 85°C)

Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	45	-	55	-	70	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
$\overline{CS}$ Low to Valid Output	t_{CO}	-	45	-	55	-	70	ns
$\overline{OE}$ Low to Valid Output	t_{OE}	-	22	-	25	-	35	ns
$\overline{CS}$ Low to Low-Z Output	t_{LZ}	10	-	10	-	10	-	ns
$\overline{OE}$ Low to Low-Z Output	t_{OLZ}	5	-	5	-	5	-	ns
$\overline{CS}$ High to High-Z Output	t_{HZ}	-	18	0	20	0	25	ns
$\overline{OE}$ High to High-Z Output	t_{OHZ}	-	18	0	20	0	25	ns
$\overline{UB}, \overline{LB}$ Access Time	t_{BA}	-	45	-	55	-	70	ns
$\overline{UB}, \overline{LB}$ Low to Low-Z Output	t_{BLZ}	5	-	5	-	5	-	ns
$\overline{UB}, \overline{LB}$ High to High-Z Output	t_{BHZ}	-	18	0	20	0	25	ns

Write Cycle (TA= -40 to 85°C)

Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	45	-	55	-	70	-	ns
$\overline{CS}$ Low to End of Write	t_{CW}	35	-	45	-	60	-	ns
Address Set-up to Start of Write	t_{AS}	0	-	0	-	0	-	ns
Address Set-up to End of Write	t_{AW}	35	-	45	-	60	-	ns
Address Hold from End of Write	t_{WR}	0	-	0	-	0	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	35	-	40	-	55	-	ns
$\overline{UB}, \overline{LB}$ Low to End of Write	t_{BW}	35	-	45	-	60	-	ns
Data Set-up to End of Write	t_{DW}	25	-	25	-	30	-	ns
Data Hold from End of Write	t_{DH}	0	-	0	-	0	-	ns
$\overline{WE}$ Low to Output High-Z	t_{WHZ}	-	18	-	20	-	25	ns
$\overline{WE}$ High to Output Low-Z	t_{OW}	5	-	5	-	5	-	ns

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Timing Diagrams

Timing Waveform Of Read Cycle(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, CS2=$\overline{WE}=V_{IH}$, $\overline{UB}=\overline{LB}=V_{IL}$ *)
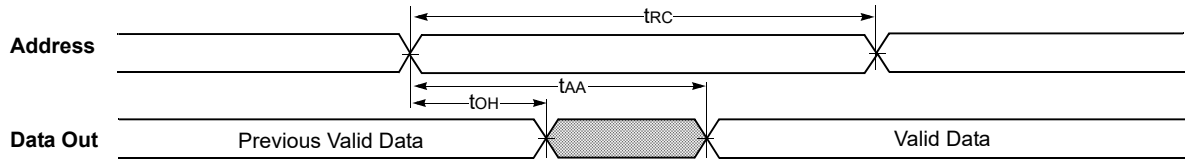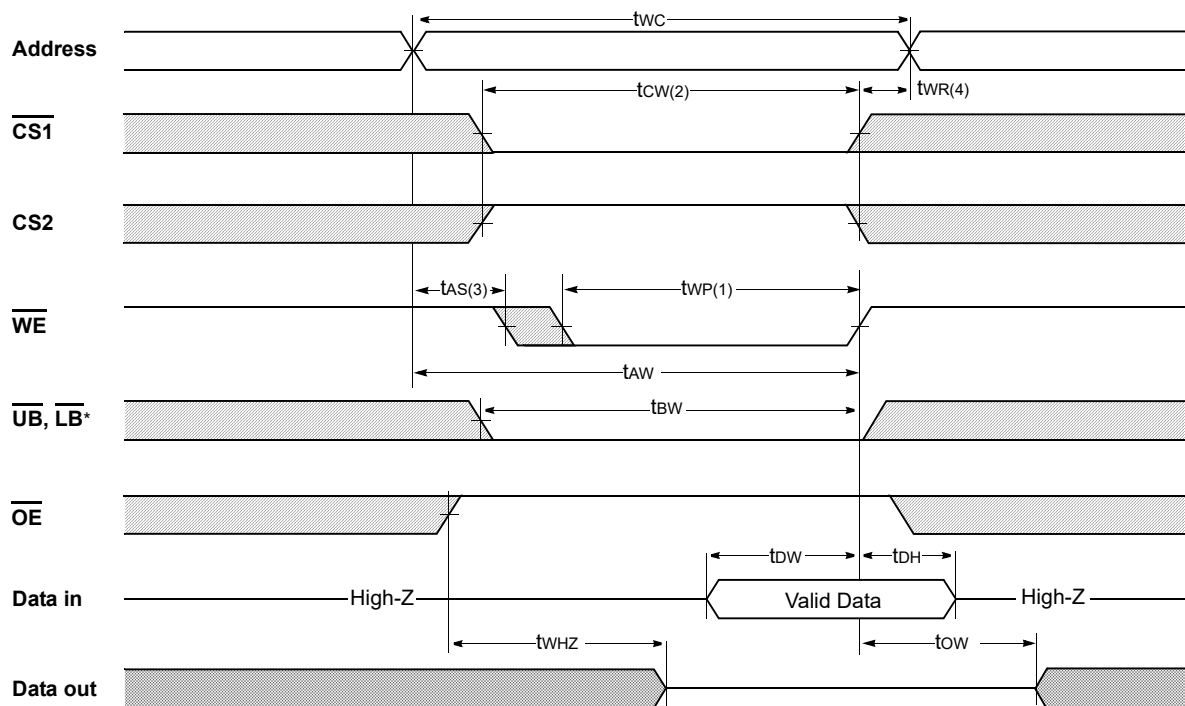

* Those parameters are applied for x16 mode only.

Timing Waveform Of Read Cycle(2) ($\overline{WE}=V_{IH}$, $\overline{OE}$ Controlled)
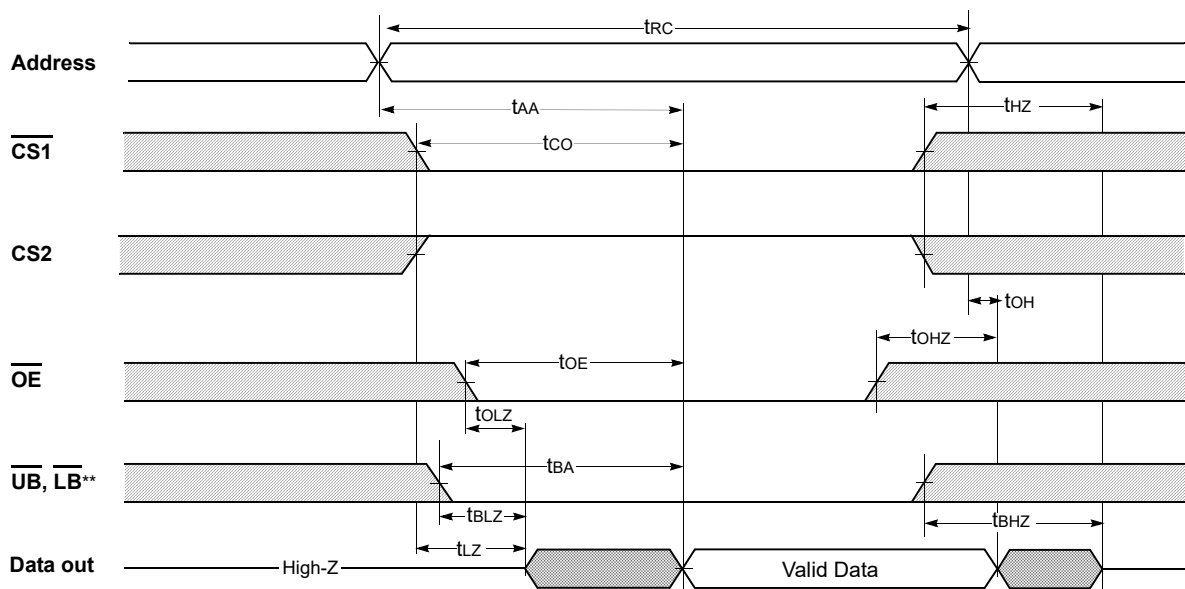

NOTES(Read Cycle)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

Timing Waveform Of Write Cycle(1) (WE Controlled)

* Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(2) (CS1, CS2 Controlled)
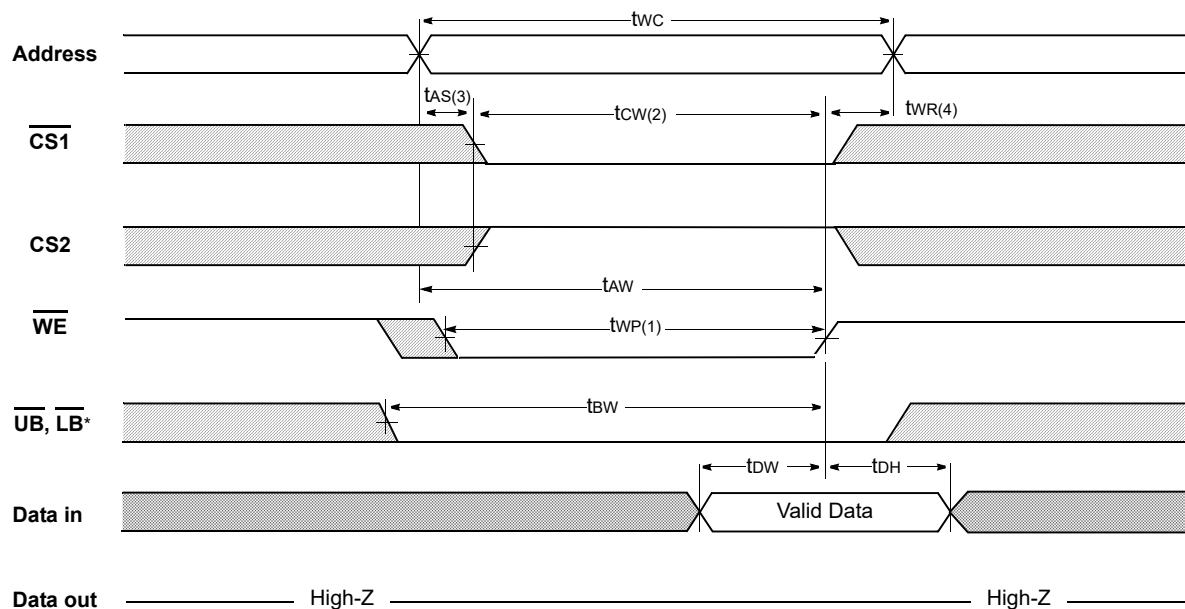
* Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(3) ($\overline{UB}$, $\overline{LB}$ Controlled)
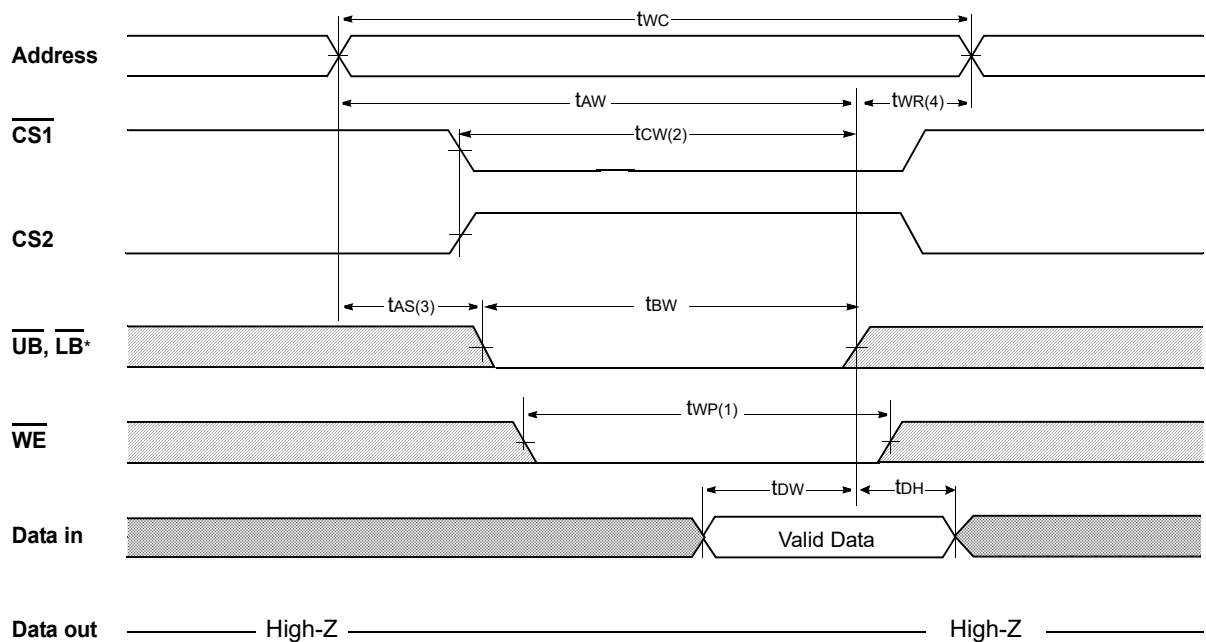
* Those parameters are applied for x16 mode only.

NOTES (Write Cycle)

1. A write occurs during the overlap(tWP) of low $\overline{CS1}$ and low $\overline{WE}$. A write begins when $\overline{CS1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and $\overline{WE}$ goes high. The tWP is measured from the beginning of write to the end of write.

2. tCW is measured from the $\overline{CS1}$ going low to the end of write.

3. tAS is measured from the address valid to the beginning of write.

4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high.
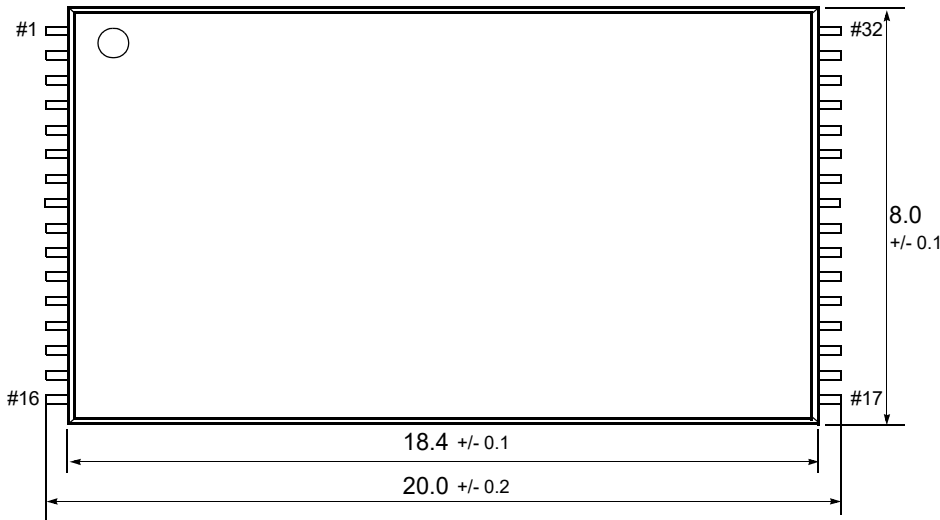
Package Dimensions

Units:millimeters/Inches

44-TSOP2-400BF

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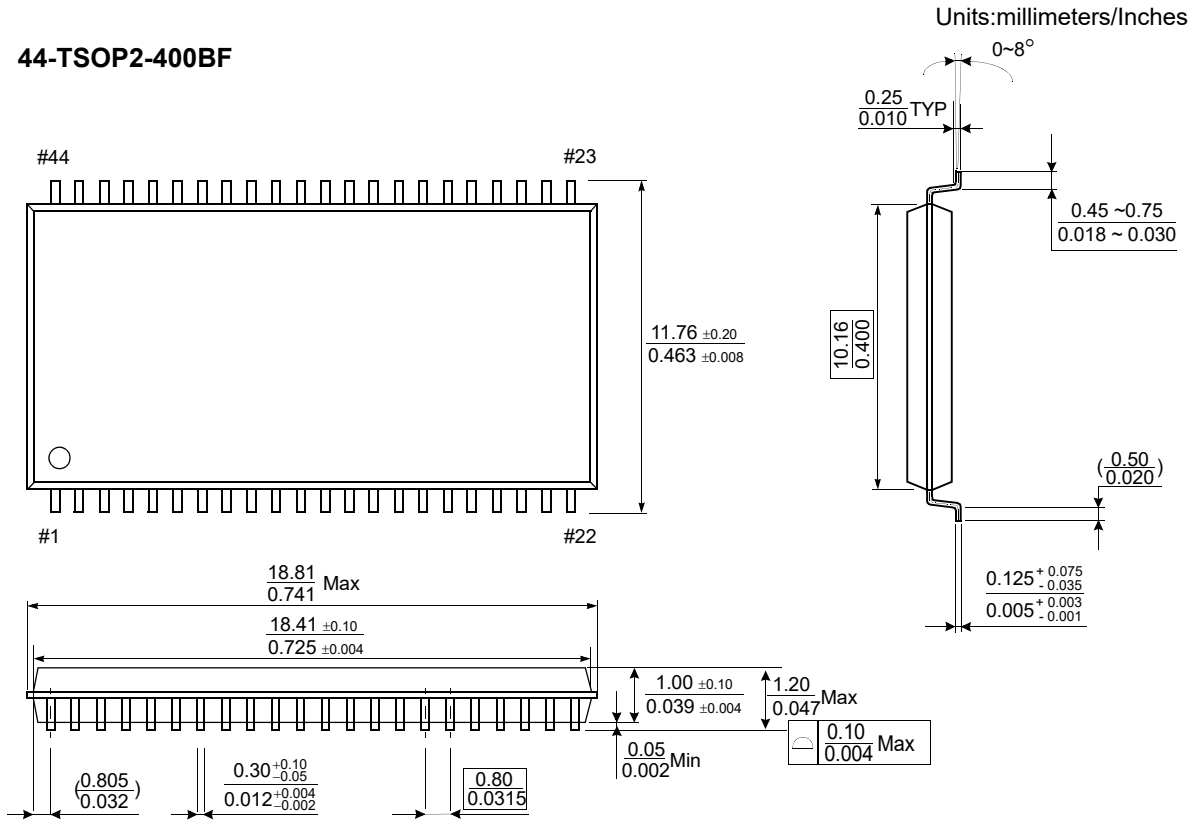
Package Dimensions

32TSOP1

Units:millimeters
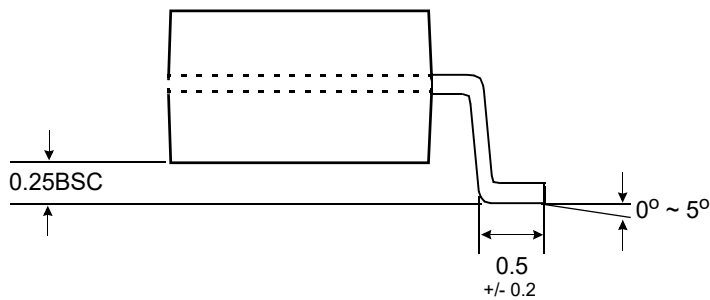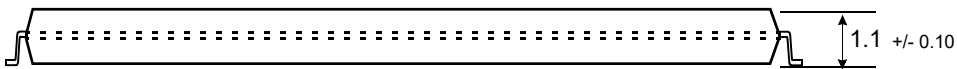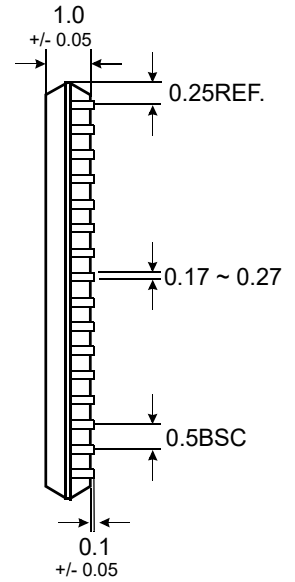
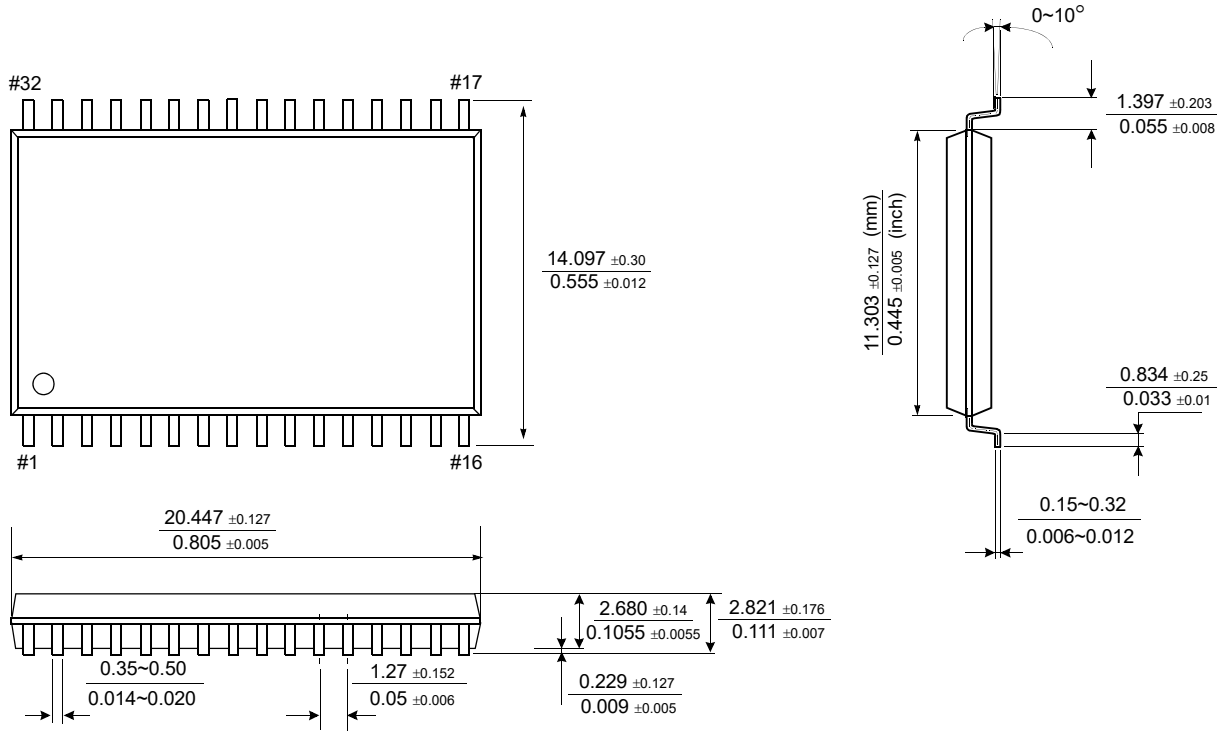## Package Dimensions

32sTSOP1

Units:millimeters
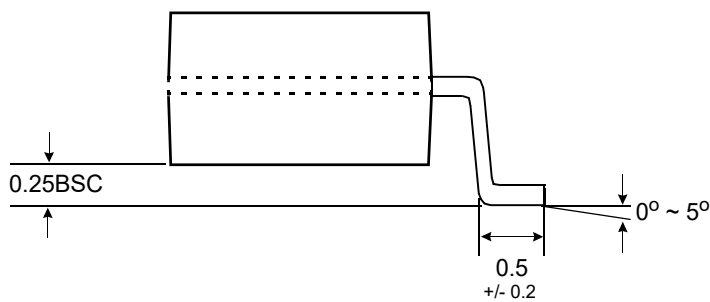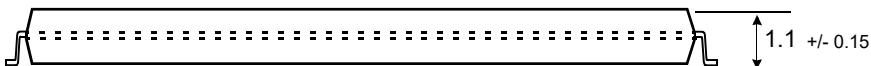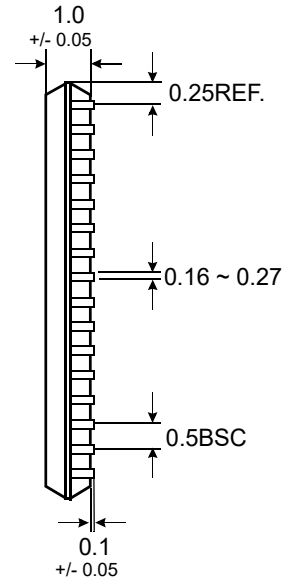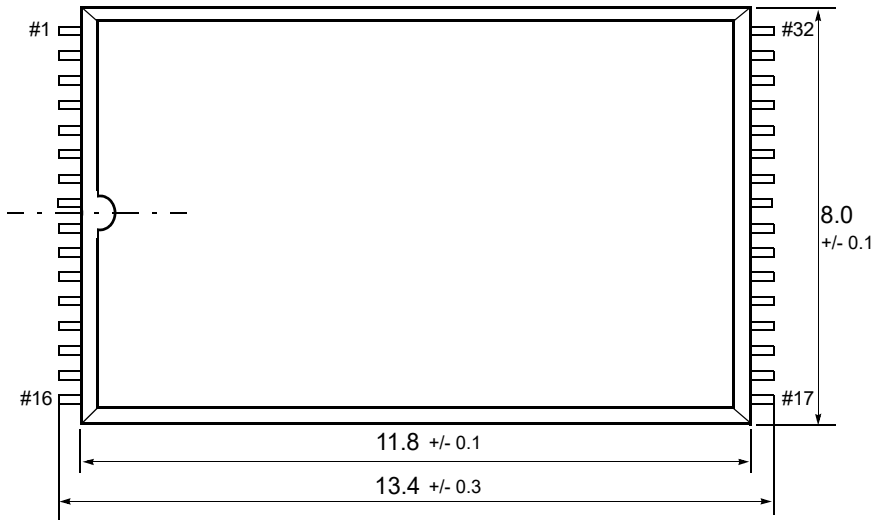
Package Dimensions

32SOP

Units:millimeters/Inches

#32   #17

$\dfrac{14.097 \pm 0.30}{0.555 \pm 0.012}$

#1   #16

$\dfrac{20.447 \pm 0.127}{0.805 \pm 0.005}$

$\dfrac{0.35\sim0.50}{0.014\sim0.020}$ $\dfrac{1.27 \pm 0.152}{0.05 \pm 0.006}$

$\dfrac{2.680 \pm 0.14}{0.1055 \pm 0.0055}$ $\dfrac{2.821 \pm 0.176}{0.111 \pm 0.007}$

$\dfrac{0.229 \pm 0.127}{0.009 \pm 0.005}$

0~10°

$\dfrac{1.397 \pm 0.203}{0.055 \pm 0.008}$

$\dfrac{11.303 \pm 0.127}{0.445 \pm 0.005}$ $\dfrac{(mm)}{(inch)}$

$\dfrac{0.834 \pm 0.25}{0.033 \pm 0.01}$

$\dfrac{0.15\sim0.32}{0.006\sim0.012}$

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Package Dimensions

32TSOP2

Units:millimeters/Inches

#32   #17

11.76 ±0.20
0.463 ±0.008

#1   #16

0~8°

0.80 ±0.10
0.031 ±0.004

10.16 ±0.13 (mm)
0.400 ±0.005 (inch)

0.50 ±0.10
0.033 ±0.004

0.12~0.21
0.0047~0.0082

20.95 ±0.13
0.825 ±0.005

1.00 ±0.05
0.04 ±0.002

1.20 max.
0.47 max.

0.30~0.52
0.012~0.020

1.27 bsc
0.05 bsc

0.10 ±0.05
0.004 ±0.002

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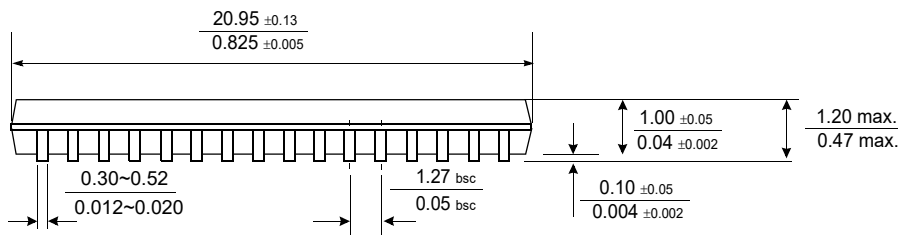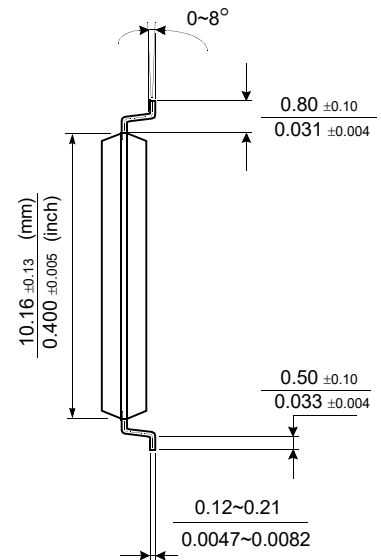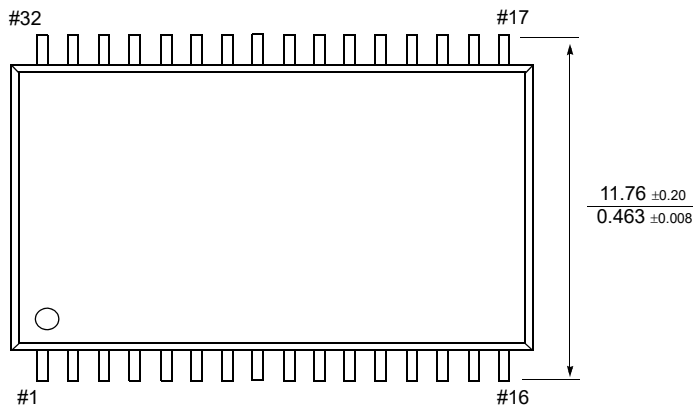
Package Dimensions

48-FBGA

6mm x 8mm Body, 0.75mm Bump Pitch, 6 x 8 Ball Grid Array

Top View

Bottom View

Side View
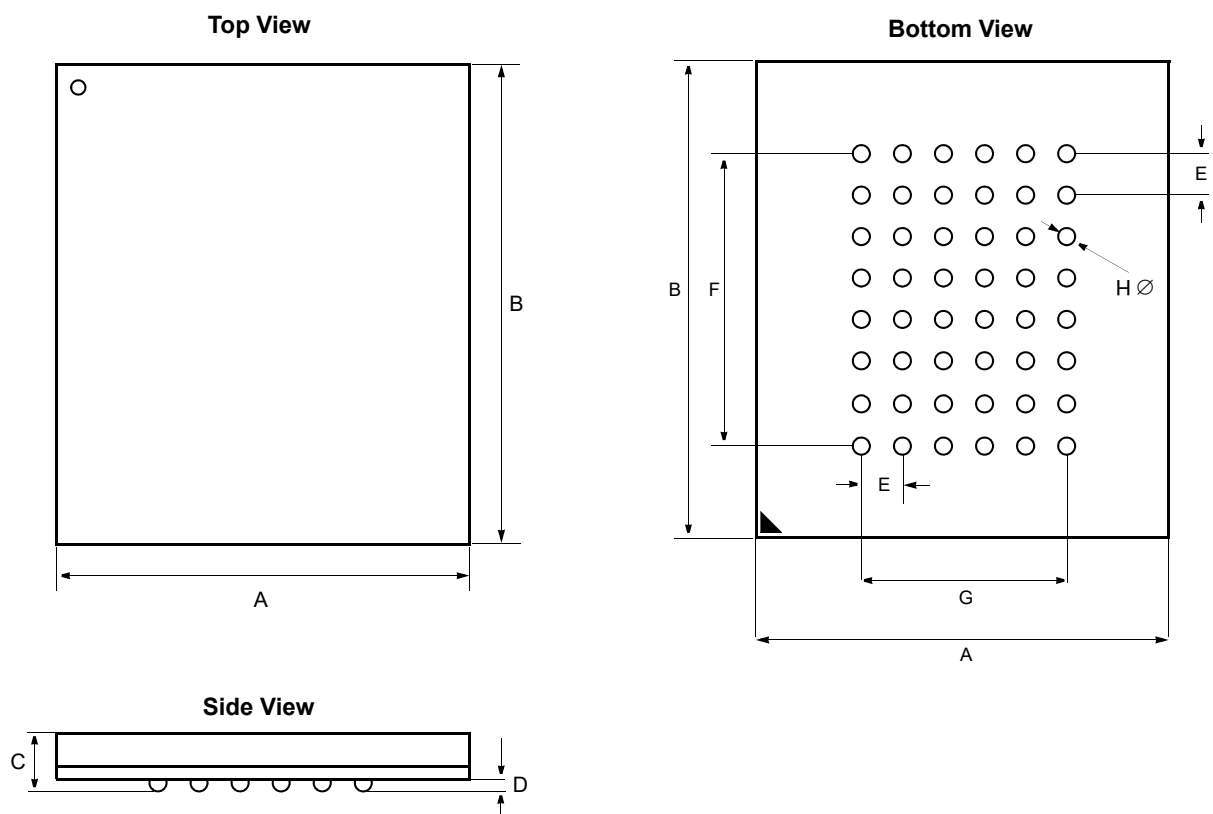
Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	6 ± 0.1	mm		**E**	0.75	mm	
B	8 ± 0.1	mm		**F**	5.25	mm	
C	1.1 ± 0.1	mm		**G**	3.75	mm	
D	0.25 ± 0.05	mm		**H**	0.35 ± 0.05	mm	