

# 8Mb Low Power SRAM M-die Specification

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**Document Title**

**512Kx16 & 1Mx8 Bit Low Power SRAM**

**Revision History**

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Nov. 2015	Preliminary
0.1	Add typical I <sub>DR</sub> value	Dec. 2015	Preliminary
1.0	Final version release Split I <sub>cc1</sub> spec value depending on V <sub>cc</sub> ; 2.3~3.6V : 6mA ; 4.5~5.5V : 8mA	Feb. 2016	Final
1.1	Add commercial temperature range	Apr. 2016	Final

# S6L8016W, S6L8016C S6L8008W, S6L8008C

## 8M Low Power SRAM

### 512Kx16 & 1Mx8 Bit Low Power SRAM

#### Features

- Fast Access Time : 45, 55, 70ns(Max.)
- CMOS Low Power Dissipation  
Standby Current (Typical) : 4 $\mu$ A  
(Maximum) : 20 $\mu$ A  
Operating Current (Typical) : 25mA (tAA=55ns)  
(Maximum) : 30mA (tAA=55ns)
- Wide range or Single 5.0V Power Supply  
- S6L80xxW : 2.3V ~ 3.6V Vcc  
- S6L80xxC : 4.5V ~ 5.5V Vcc
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control (x16 Mode)  
LB : I/O0~ I/O7, UB : I/O8~ I/O15
- Standard 44TSOP2, 48FBGA Package Pin Configuration
- ROHS compliant
- Operating in Commercial and Industrial Temperature range.
- 2CS Option Available

#### General Description

The S6L8016(W/C) and S6L8008(W/C) are a 8,388,608-bit high-speed Static Random Access Memory organized as 512K (1M) words by 16(8) bits. S6L8016(W/C) allows that lower and upper byte access by data byte control( $\overline{UB}$ ,  $\overline{LB}$ ). The device is fabricated using advanced CMOS process, 6-TR based cell technology and designed for low power circuit technology. It is particularly well suited for use in battery back up application for low data retention current.

The S6L8016(W/C) and S6L8008(W/C) are packaged in a 44TSOP2 and 48FBGA.

### 8Mb Low Power SRAM Ordering Information (512Kx16) - 1CS

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
8Mb	512Kx16	S6L8016W1M-UC(I)45	2.5, 3.3	45	20	44 TSOP2	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L8016W1M-UC(I)55	2.5, 3.3	55	25	44 TSOP2	
		S6L8016W1M-UC(I)70	2.5, 3.3	70	35	44 TSOP2	
		S6L8016C1M-UC(I)45	5.0	45	20	44 TSOP2	
		S6L8016C1M-UC(I)55	5.0	55	25	44 TSOP2	
		S6L8016C1M-UC(I)70	5.0	70	35	44 TSOP2	

### 8Mb Low Power SRAM Ordering Information (512Kx16) - 2CS

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
8Mb	512Kx16	S6L8016W2M-XC(I)45	2.5, 3.3	45	20	48 FBGA	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L8016W2M-XC(I)55	2.5, 3.3	55	25	48 FBGA	
		S6L8016W2M-XC(I)70	2.5, 3.3	70	35	48 FBGA	
		S6L8016C2M-XC(I)45	5.0	45	20	48 FBGA	
		S6L8016C2M-XC(I)55	5.0	55	25	48 FBGA	
		S6L8016C2M-XC(I)70	5.0	70	35	48 FBGA	

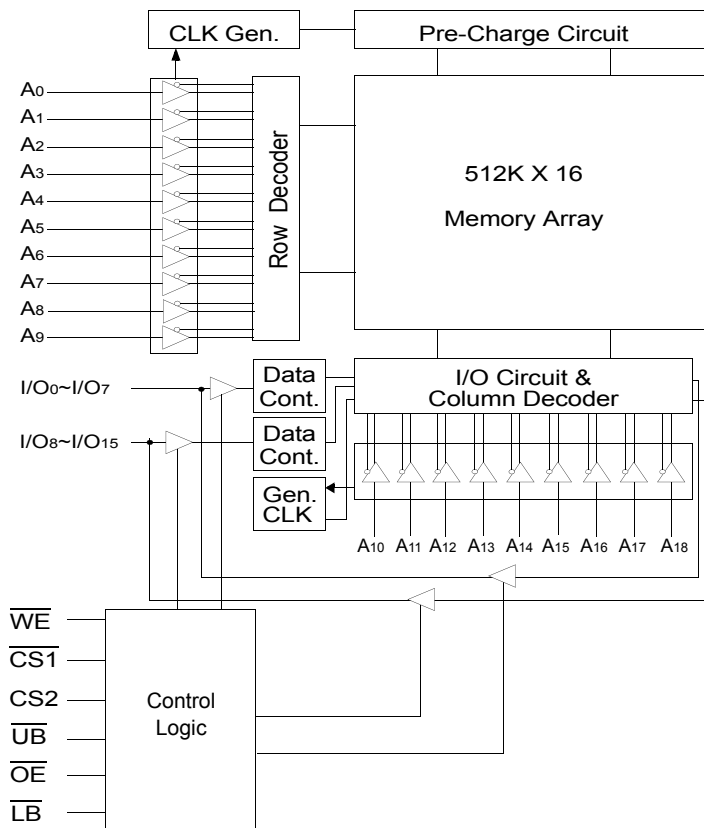
**S6L8016W, S6L8016C**  
**S6L8008W, S6L8008C**

**8M Low Power SRAM**

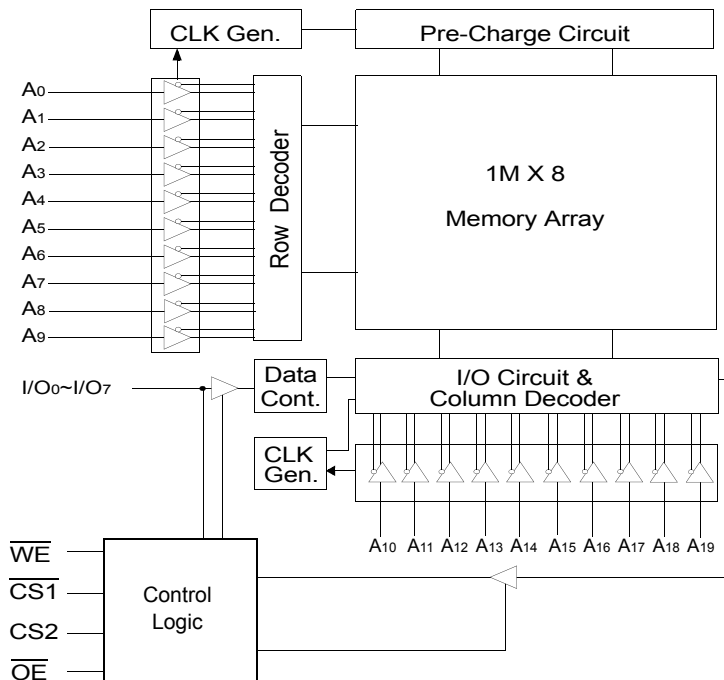
**8Mb Low Power SRAM Ordering Information (1Mx8) - 2CS**

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
8Mb	1Mx8	S6L8008W2M-UC(I)45	2.5, 3.3	45	20	44 TSOP2	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L8008W2M-UC(I)55	2.5, 3.3	55	25	44 TSOP2	
		S6L8008W2M-UC(I)70	2.5, 3.3	70	35	44 TSOP2	
		S6L8008C2M-UC(I)45	5.0	45	20	44 TSOP2	
		S6L8008C2M-UC(I)55	5.0	55	25	44 TSOP2	
		S6L8008C2M-UC(I)70	5.0	70	35	44 TSOP2	
		S6L8008W2M-XC(I)45	2.5, 3.3	45	20	48 FBGA	
		S6L8008W2M-XC(I)55	2.5, 3.3	55	25	48 FBGA	
		S6L8008W2M-XC(I)70	2.5, 3.3	70	35	48 FBGA	
		S6L8008C2M-XC(I)45	5.0	45	20	48 FBGA	
		S6L8008C2M-XC(I)55	5.0	55	25	48 FBGA	
		S6L8008C2M-XC(I)70	5.0	70	35	48 FBGA	

Logic Block Diagram - 512K x 16



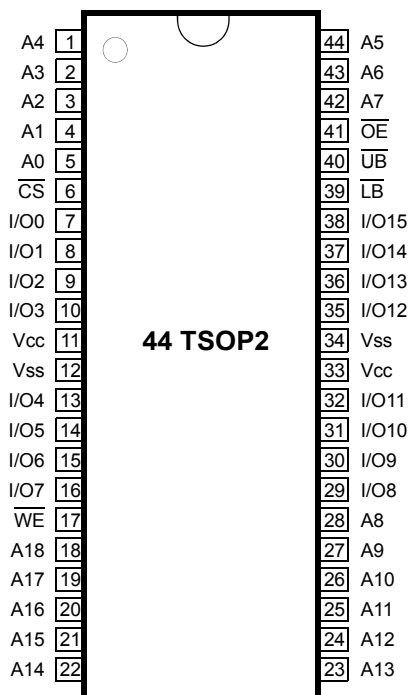
Logic Block Diagram - 1M x 8



**S6L8016W, S6L8016C  
S6L8008W, S6L8008C**

**8M Low Power SRAM**

**44 TSOP2 Package Pin Configurations (Top View) - S6L8016(W/C)1M (512K x 16) - 1CS**

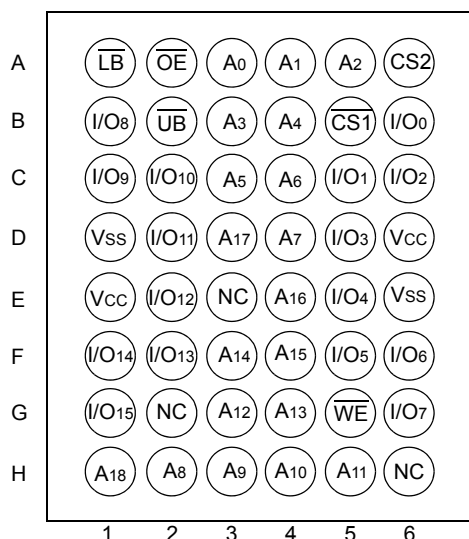


**Pin Function**

Pin Name	Pin Function
A0 - A18	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-byte Control(I/O0~I/O7)
$\overline{UB}$	Upper-byte Control(I/O8~I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground

**48FBGA - S6L8016(W/C)2M (512K x 16) - 2CS - Top View**

**PKG Pin Configurations**



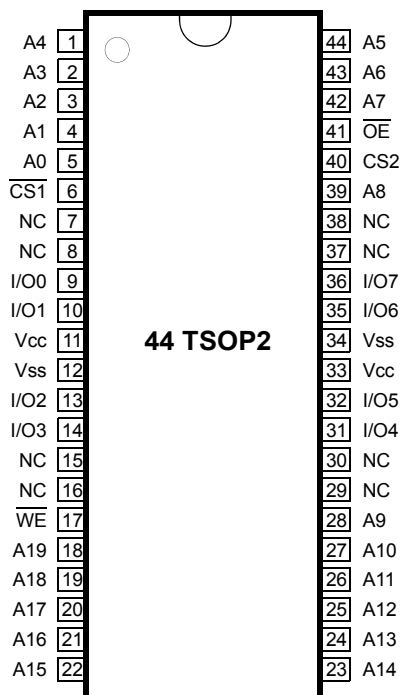
**Pin Function**

Pin Name	Pin Function
A0 - A18	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$	Chip Select Input1
CS2	Chip Select Input2
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-byte Control(I/O0~I/O7)
$\overline{UB}$	Upper-byte Control(I/O8~I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

**S6L8016W, S6L8016C  
S6L8008W, S6L8008C**

**8M Low Power SRAM**

**44 TSOP2 Package Pin Configurations (Top View) - S6L8008(W/C)2M (1M x 8) - 2CS**

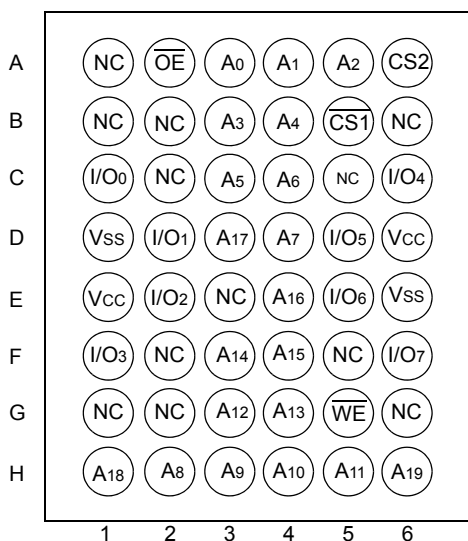


**Pin Function**

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable Input
CS1	Chip Select Input1
CS2	Chip Select Input2
OE	Output Enable Input
I/O0 ~ I/O7	Data Inputs/Outputs
Vcc	Power
Vss	Ground

**48FBGA - S6L8008(W/C)2M (1M x 8) - 2CS - Top View**

**PKG Pin Configurations**



**Pin Function**

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable Input
CS1	Chip Select Input1
CS2	Chip Select Input2
OE	Output Enable Input
I/O0 ~ I/O7	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

**S6L8016W, S6L8016C**  
**S6L8008W, S6L8008C**

**8M Low Power SRAM**

**Absolute Maximum Ratings\***

Parameter	Symbol	Rating	Unit
Voltage on Any Pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5V	V
Voltage on Vcc Supply Relative to Vss	Wide Vcc** Product	-0.5 to 4.6	V
	5.0V Product	-0.5 to 7.0	
Power Dissipation	P <sub>D</sub>	1.0	W
Storage Temperature	T <sub>STG</sub>	-65 to +150	°C
Operating Temperature	Commercial	0 to 70	°C
	Industrial	-40 to 85	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\* Wide Vcc range is 2.3V ~ 3.6V.

**Recommended DC Operating Conditions (TA= -40 to 85°C)**

Parameter	Operating Vcc(V)	Symbol	Min	Typ	Max	Unit
Supply Voltage	5.0	V <sub>CC</sub>	4.5	5.0	5.5	V
	Wide 2.3 ~ 3.6	V <sub>CC</sub>	2.3	2.5/3.3	3.6	
Ground		V <sub>SS</sub>	0	0	0	V
Input High Voltage	5.0	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5	V
	Wide 2.3 ~ 2.7	V <sub>IH</sub>	1.8	-	V <sub>CC</sub> +0.3	
	Wide 2.7 ~ 3.6	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3	
Input Low Voltage	5.0	V <sub>IL</sub>	-0.3	-	0.8	V
	Wide 2.3 ~ 2.7	V <sub>IL</sub>	-0.3	-	0.6	
	Wide 2.7 ~ 3.6	V <sub>IL</sub>	-0.3	-	0.8	



**S6L8016W, S6L8016C**  
**S6L8008W, S6L8008C**

**8M Low Power SRAM**

**DC and Operating Characteristics** (TA= -40 to 85°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS1}=V_{IH}$ or $\overline{CS2}=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$	-1	-	1	μA	
Operating Current	I <sub>CC</sub>	f=f <sub>max</sub> , V <sub>CC</sub> =V <sub>CCmax</sub> , I <sub>OUT</sub> =0mA, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V	45ns	-	-	30	mA
			55ns	-	-	30	
			70ns	-	-	25	
	I <sub>CC1</sub>	f=1MHz, V <sub>CC</sub> =V <sub>CCmax</sub> , I <sub>OUT</sub> =0mA, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V	V <sub>CC</sub> =2.3~3.6V		-	-	6
V <sub>CC</sub> =4.5~5.5V		-	-	8			
Standby Current	I <sub>SB1</sub> (CMOS)	V <sub>CC</sub> =V <sub>CCmax</sub> , V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V, 1) $\overline{CS2} \leq 0.2V$ , or 2) $\overline{CS2} \geq V_{CC}-0.2V$ , $\overline{CS1} \geq V_{CC}-0.2V$ , or 3) $\overline{CS2} \geq V_{CC}-0.2V$ , $\overline{CS1} \leq 0.2V$ , $\overline{UB}=\overline{LB} \geq V_{CC}-0.2V$	2CS	-	4	20	μA
			1CS	V <sub>CC</sub> =V <sub>CCmax</sub> , V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V, 1) $\overline{CS} \geq V_{CC}-0.2V$ , or 2) $\overline{CS} \leq 0.2V$ , $\overline{UB}=\overline{LB} \geq V_{CC}-0.2V$			
Output Low Voltage Level	V <sub>OL</sub>	V <sub>CC</sub> =4.5V, I <sub>OL</sub> =2.1mA, 5.0V Product	-	-	0.4	V	
		V <sub>CC</sub> =2.7V, I <sub>OL</sub> =2.1mA, Wide V <sub>CC</sub> * Product	-	-	0.4		
		V <sub>CC</sub> =2.3V, I <sub>OL</sub> =2.1mA, Wide V <sub>CC</sub> * Product	-	-	0.4		
Output High Voltage Level	V <sub>OH</sub>	V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-1mA, 5.0V Product	2.4	-	-	V	
		V <sub>CC</sub> =2.7V, I <sub>OH</sub> =-1mA, Wide V <sub>CC</sub> * Product	2.4	-	-		
		V <sub>CC</sub> =2.3V, I <sub>OH</sub> =-1mA, Wide V <sub>CC</sub> * Product	1.8	-	-		

Note : Typical parameters indicates the value for the center of distribution at V<sub>CC</sub>=3.0V and Ta=25°C, and not 100% tested.

\* Wide V<sub>CC</sub> range is 2.3V ~ 3.6V.

**Capacitance\***(TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	TYP	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF

\* Capacitance is sampled and not 100% tested.

**Functional Description (x8 Mode) -2CS**

$\overline{CS}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	X	Not Select	High-Z	ISB, ISB1
X	L	X	X	Not Select	High-Z	ISB, ISB1
L	H	H	L	Read	DOUT	Icc
L	H	L	X	Write	DIN	Icc
L	H	H	H	Output Disable	High-Z	Icc

\* X means Don't Care.

**Functional Description (x16 Mode) - 1CS**

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O Pin		Mode	Supply Current
					I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>		
H	X*	X	X	X	High-Z	High-Z	Not Select	ISB, ISB1
X	X	X	H	H				
L	H	H	L	X	High-Z	High-Z	Output Disable	Icc
L	H	H	X	L				
L	H	L	L	H	DOUT	High-Z	Lower Byte Read	Icc
			H	L	High-Z	DOUT	Upper Byte Read	
			L	L	DOUT	DOUT	Word Read	
L	L	X	L	H	DIN	High-Z	Lower Byte Write	Icc
			H	L	High-Z	DIN	Upper Byte Write	
			L	L	DIN	DIN	Word Write	

\* X means Don't Care.

**Functional Description (x16 Mode) - 2CS**

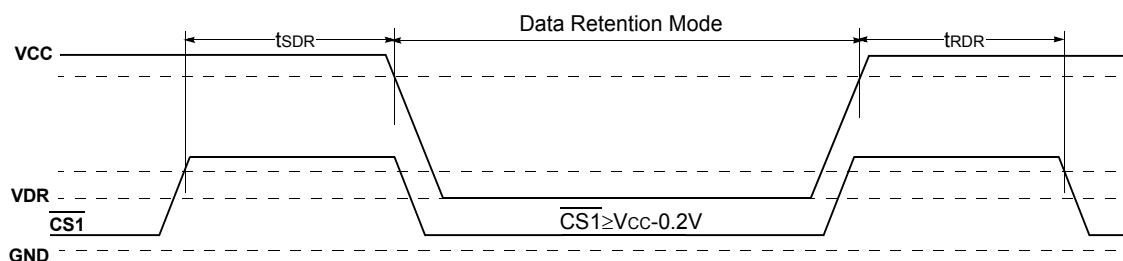
$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O Pin		Mode	Supply Current
						I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>		
H	X*	X	X	X	X	High-Z	High-Z	Not Select	ISB, ISB1
X	L	X	X	X	X				
X	X	X	X	H	H				
L	H	H	H	L	X	High-Z	High-Z	Output Disable	Icc
L	H	H	H	X	L				
L	H	H	L	L	H	DOUT	High-Z	Lower Byte Read	Icc
				H	L	High-Z	DOUT	Upper Byte Read	
				L	L	DOUT	DOUT	Word Read	
L	H	L	X	L	H	DIN	High-Z	Lower Byte Write	Icc
				H	L	High-Z	DIN	Upper Byte Write	
				L	L	DIN	DIN	Word Write	

\* X means Don't Care.

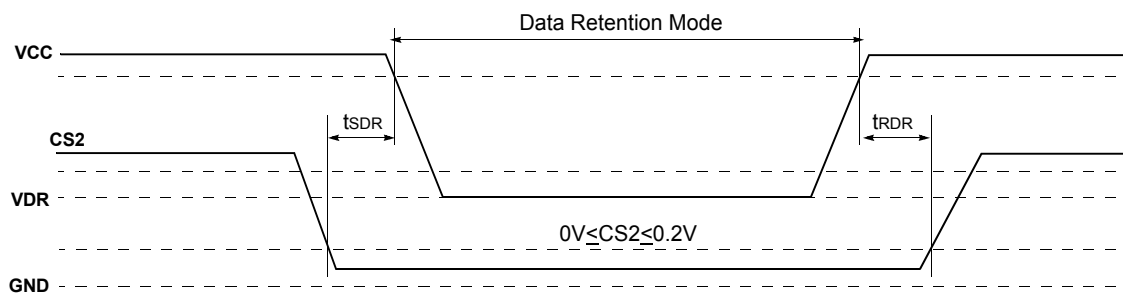
**Data Retention Characteristics** (TA= -40 to 85°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
VCC for Data Retention	VDR	Refer to Data Retention Waveform	1.5	-	-	V	
Data Retention Current	IDR	VCC=1.5V, VIN≥VCC-0.2V or VIN≤0.2V 1) CS2≤0.2V, or 2) CS2≥VCC-0.2V, CS1≥VCC-0.2V, or 3) CS2≥VCC-0.2V, CS1≤0.2V, UB=LB≥VCC-0.2V	2CS	-	4	20	μA
		VCC=1.5V, VIN≥VCC-0.2V or VIN≤0.2V 1) CS≥VCC-0.2V, or 2) CS≤0.2V, UB=LB≥VCC-0.2V	1CS				
Data Retention Set-Up Time	tSDR	Refer to Data Retention Waveform	0	-	-	ns	
Recovery Time	tRDR		tRC	-	-	ns	

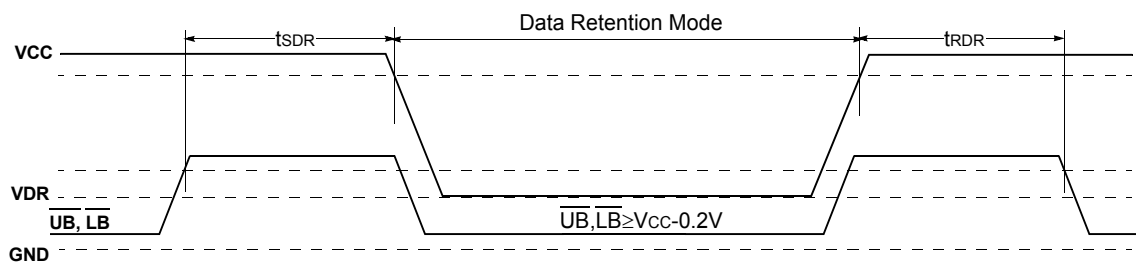
**Data Retention Wave Form (1) - CS1 Controlled**



**Data Retention Wave Form (2) - CS2 controlled**



**Data Retention Wave Form (3) - UB, LB Controlled**



**S6L8016W, S6L8016C  
S6L8008W, S6L8008C**

**8M Low Power SRAM**

**AC Test Conditions**

Parameter	Value
Input Pulse Level	0 to 3.0V (V <sub>CC</sub> =3.3V or 5.0V)
	0 to 2.5V (V <sub>CC</sub> =2.5V)
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V (V <sub>CC</sub> =3.3V or 5.0V)
	1/2V <sub>CC</sub> (V <sub>CC</sub> =2.5V)
Output Load	CL=30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> =-1mA/2.1mA

**Read Cycle (TA= -40 to 85°C)**

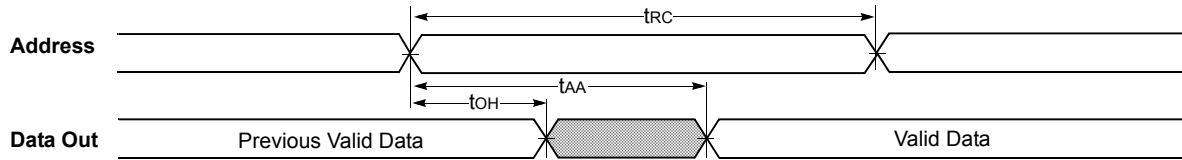
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	45	-	55	-	70	-	ns
Address Access Time	t <sub>AA</sub>	-	45	-	55	-	70	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	10	-	ns
$\overline{\text{CS}}$ Low to Valid Output	t <sub>CO</sub>	-	45	-	55	-	70	ns
$\overline{\text{OE}}$ Low to Valid Output	t <sub>OE</sub>	-	22	-	25	-	35	ns
$\overline{\text{CS}}$ Low to Low-Z Output	t <sub>LZ</sub>	10	-	10	-	10	-	ns
$\overline{\text{OE}}$ Low to Low-Z Output	t <sub>OLZ</sub>	5	-	5	-	5	-	ns
$\overline{\text{CS}}$ High to High-Z Output	t <sub>HZ</sub>	-	18	0	20	0	25	ns
$\overline{\text{OE}}$ High to High-Z Output	t <sub>OHZ</sub>	-	18	0	20	0	25	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Access Time	t <sub>BA</sub>	-	45	-	55	-	70	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Low to Low-Z Output	t <sub>BLZ</sub>	5	-	5	-	5	-	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ High to High-Z Output	t <sub>BHZ</sub>	-	18	0	20	0	25	ns

**Write Cycle (TA= -40 to 85°C)**

Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	45	-	55	-	70	-	ns
$\overline{\text{CS}}$ Low to End of Write	t <sub>CW</sub>	35	-	45	-	60	-	ns
Address Set-up to Start of Write	t <sub>AS</sub>	0	-	0	-	0	-	ns
Address Set-up to End of Write	t <sub>AW</sub>	35	-	45	-	60	-	ns
Address Hold from End of Write	t <sub>WR</sub>	0	-	0	-	0	-	ns
$\overline{\text{WE}}$ Pulse Width	t <sub>WP</sub>	35	-	40	-	55	-	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Low to End of Write	t <sub>BW</sub>	35	-	45	-	60	-	ns
Data Set-up to End of Write	t <sub>DW</sub>	25	-	25	-	30	-	ns
Data Hold from End of Write	t <sub>DH</sub>	0	-	0	-	0	-	ns
$\overline{\text{WE}}$ Low to Output High-Z	t <sub>WHZ</sub>	-	18	-	20	-	25	ns
$\overline{\text{WE}}$ High to Output Low-Z	t <sub>OW</sub>	5	-	5	-	5	-	ns

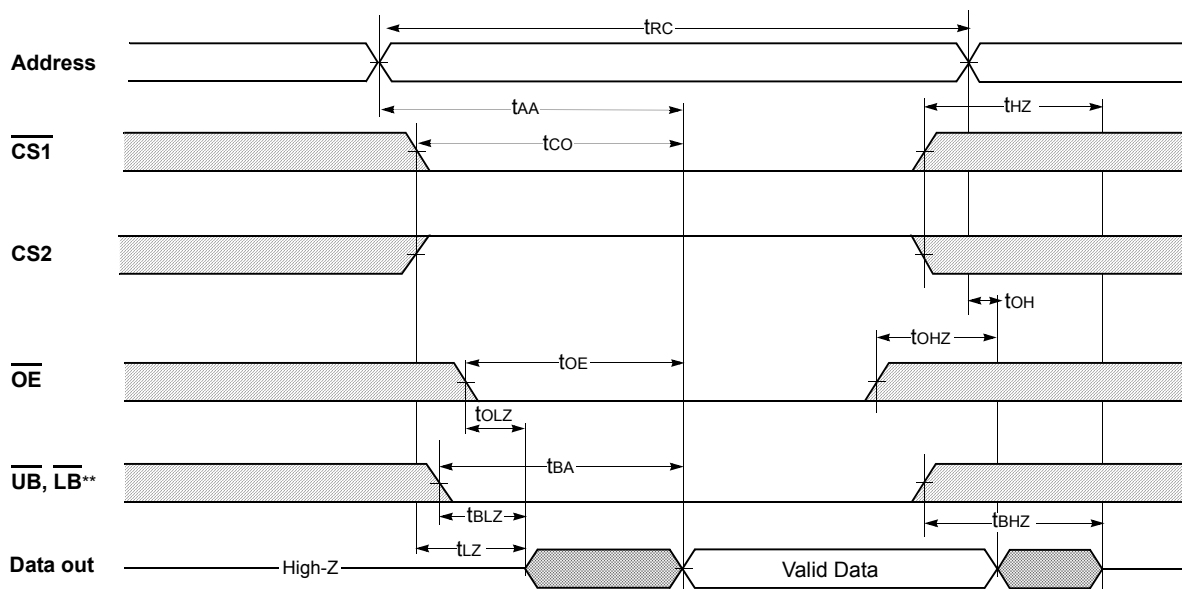
**Timing Diagrams**

**Timing Waveform Of Read Cycle(1)** (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ ,  $\overline{UB}=\overline{LB}=V_{IL}$  \*)



\* Those parameters are applied for x16 mode only.

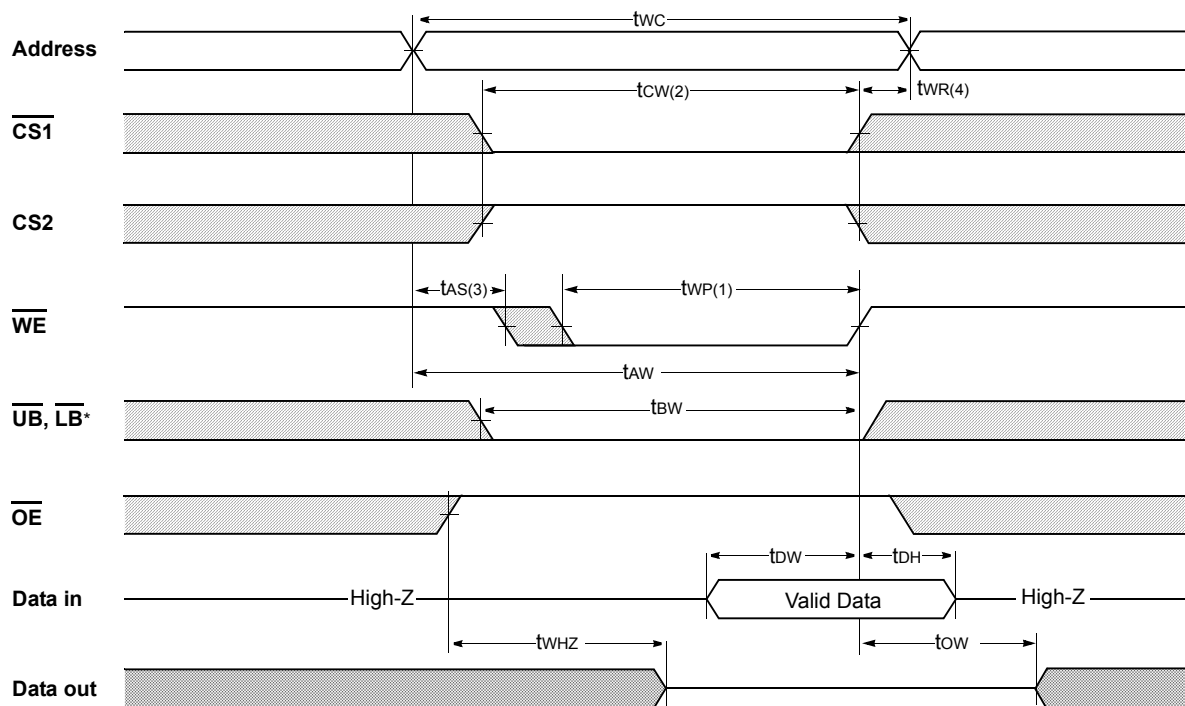
**Timing Waveform Of Read Cycle(2)** ( $\overline{WE}=V_{IH}$ ,  $\overline{OE}$  Controlled)



**NOTES(Read Cycle)**

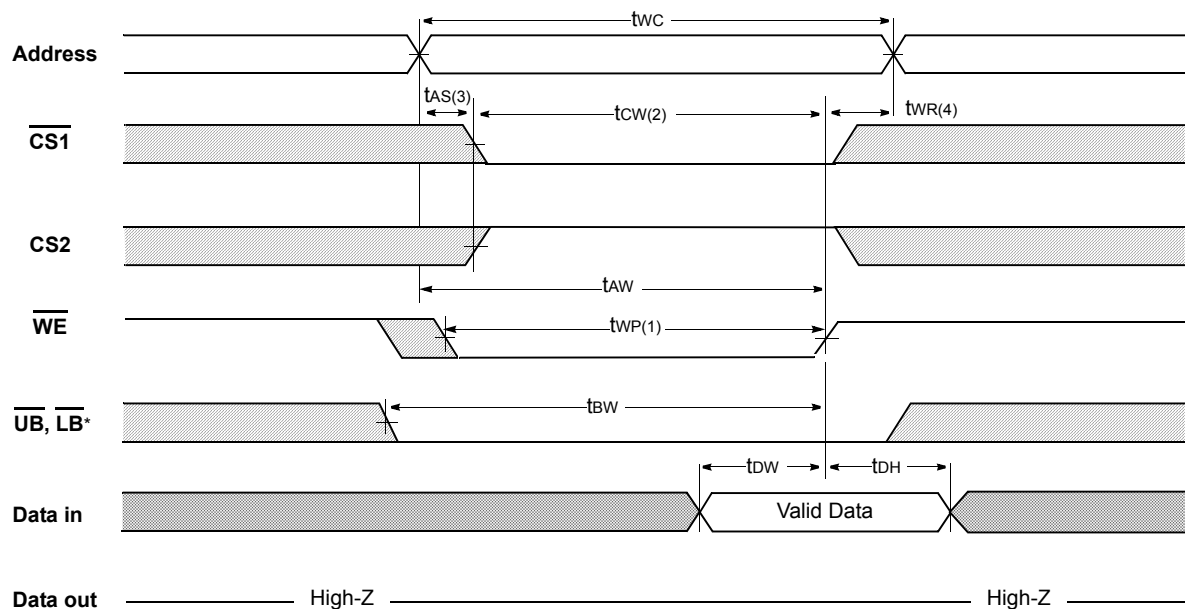
1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.

Timing Waveform Of Write Cycle(1) ( $\overline{WE}$  Controlled)



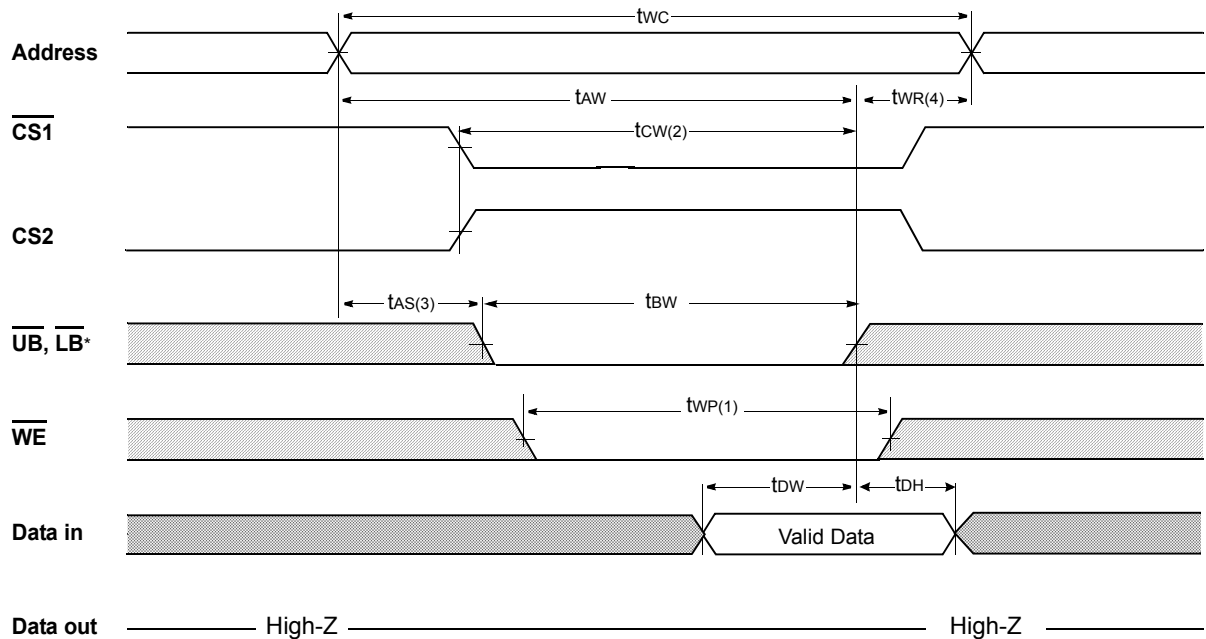
\* Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(2) ( $\overline{CS1}$ ,  $\overline{CS2}$  Controlled)



\* Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(3) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)



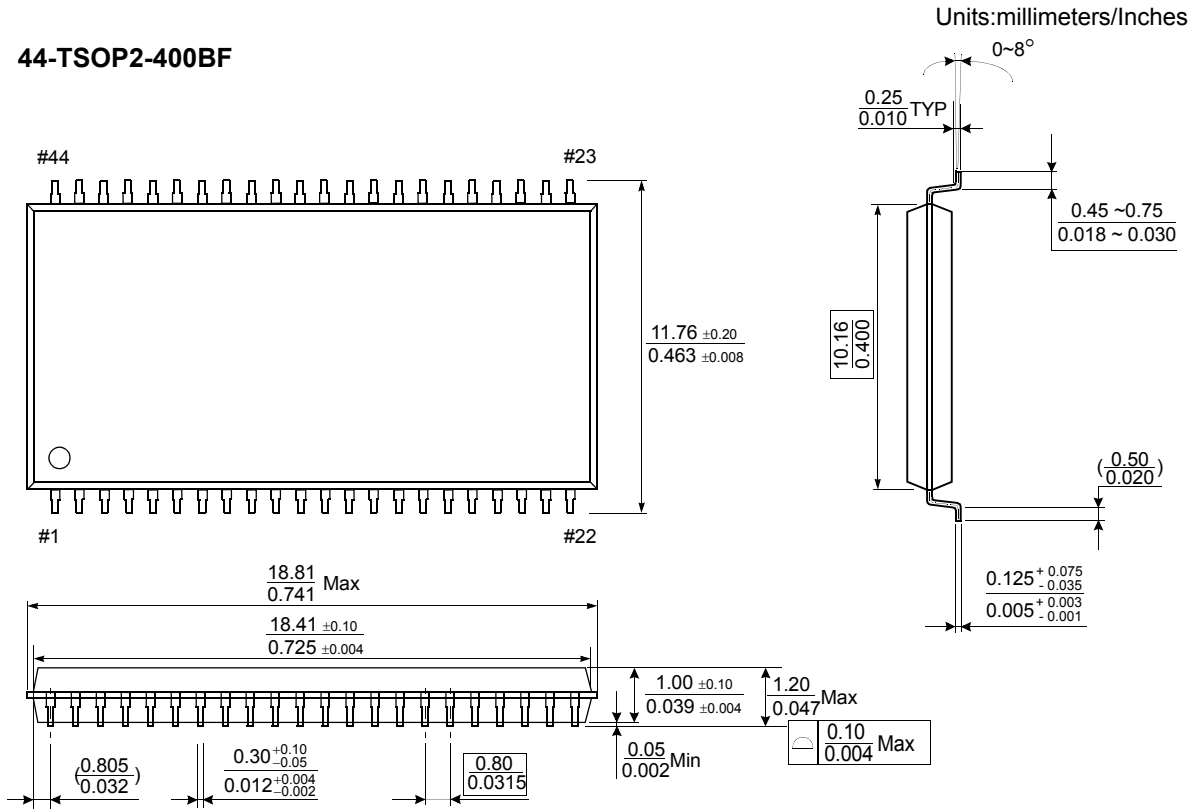
\* Those parameters are applied for x16 mode only.

NOTES (Write Cycle)

1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS1}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS1}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS1}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS1}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS1}$  or  $\overline{WE}$  going high.

Package Dimensions

44-TSOP2-400BF

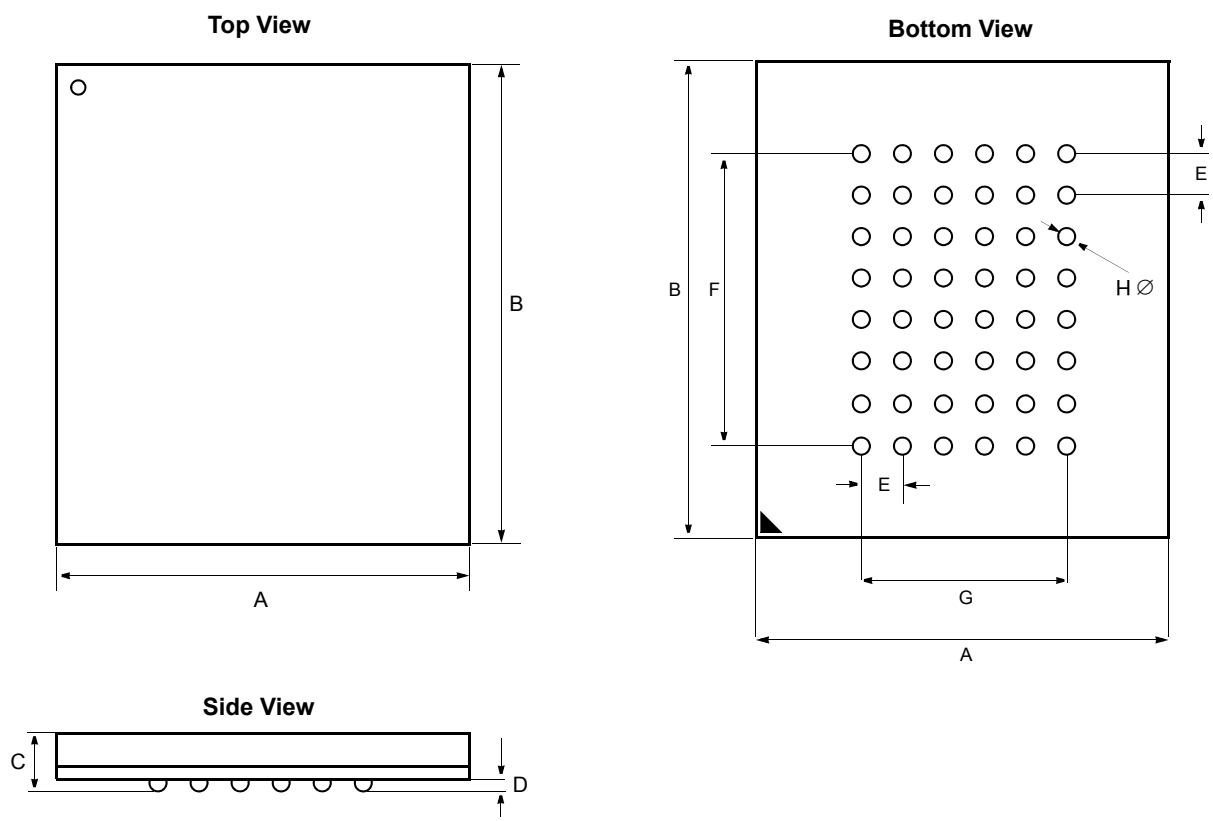




Package Dimensions

48-FBGA

6mm x 8mm Body, 0.75mm Bump Pitch, 6 x 8 Ball Grid Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
<b>A</b>	6 ± 0.1	mm		<b>E</b>	0.75	mm	
<b>B</b>	8 ± 0.1	mm		<b>F</b>	5.25	mm	
<b>C</b>	1.1 ± 0.1	mm		<b>G</b>	3.75	mm	
<b>D</b>	0.25 ± 0.05	mm		<b>H</b>	0.35 ± 0.05	mm	