Document Title

1Gb (128M x 8 / 64M x 16) DDRII SDRAM Datasheet

Revision History

Revision	Date	Page	Notes
0.1	March, 2010	—	Original
1.0	October, 2010	—	Added DDR2-1066
1.1	October, 2011	2	Added Part number list
1.2	April, 2012	—	Type corrections
1.3	April'2013	—	Modified operation temperature range description Modified tRAS

Features

- Density: 1G bits
- Organization
  - 8M words × 16 bits × 8 banks
  - 16M words × 8 bits × 8 banks
- Package: Lead-free (RoHS compliant)
  - 60ball BGA for x4/x8 component
  - 84ball BGA for x16 component
- Power supply: VDD, VDDQ = 1.8V ± 0.1V
- Page size
  - 1KB for x4/x8
  - 2KB for x16
- Four internal banks for concurrent operation
- Interface: JEDEC standard 1.8V I/O (SSTL_18 compatible)
- Burst lengths (BL): 4, 8
- Burst type (BT):
  - Sequential (4, 8)
  - Interleave (4, 8)
- /CAS Latency (CL): 3, 4, 5, 6, 7
- Precharge: auto precharge operation for each burst access
- Driver strength: normal/weak
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/64ms
  - Average refresh period
    7.8μs at 0°C ≤ TC ≤ +85°C
    3.9μs at +85°C < TC ≤ +95°C
- Operating case temperature range
  - Standard grade TC = 0°C to +95°C
  - Industrial grade TC = -40°C to +95°C
- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 4 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver Impedance Adjustment and On-Die-Termination for better signal quality
- /DQS can be disabled for single-ended Data Strobe operation

Ordering Information

Part No.	Data rate (MT/s)	Organization	Tc	Package
PME810808BBR-E6DN(C)	667 (5-5-5)	128Mx8	0-95°C	60ball
PME810808BBR-E7DN(C)	800 (5-5-5)	128Mx8		
PME810808BBR-G8DN	1066 (7-7-7)	128Mx8		
PME810816BBR-E6DN(C)	667 (5-5-5)	64Mx16		84-ball FBGA
PME810816BBR-E7DN(C)	800 (5-5-5)	64Mx16		
PME810816BBR-G8DN	1066 (7-7-7)	64Mx16		
PME810816BBR-F8DN	1066 (6-6-6)	64Mx16		
PME810808BBR-E6IN	667 (5-5-5)	128Mx8	-40-95°C	60-ball FBGA
PME810808BBR-E7IN	800 (5-5-5)	128Mx8		
PME810808BBR-G8IN	1066 (6-6-6)	128Mx8		
PME810816BBR-E6IN	667(5-5-5)	64Mx16		84-ball FBGA
PME810816BBR-E7IN	800 (5-5-5)	64Mx16		
PME810816BBR-G8IN	1066 (7-7-7)	64Mx16		

Descriptions

The 1giga bit (1Gb) Double-Data-Rate-2 (DDR2) DRAMs is a high-speed CMOS Double Data Rate 2 SDRAM containing 1,073,741,824 bits. It is internally configured a an octal-bank DRAM.

The 1Gb chip is organized as 32Mbit x 4 I/O x 8 bank, 16Mbit x 8 I/O x 8 bank or 8bit x 16 I/O x 8 bank device. These synchronous devices achieve high speed double-data-rate transfer rates of up to 800 Mb/sec/pin for general applications.

The chip is designed to comply with all DDR2 DRAM key features: (1) posted CS with additive latency, (2) write latency = read latency -1, (3) normal and weak strength data-output driver, (4) variable data-output impedance adjustment and (5) an ODT (On-Die Termination) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion. A 14 bit address bus for x4/x8 organized components and A 13 bit address bus for x16 component is used to convey row, column, and bank address devices.

These devices operate with a single 1.8V ± 0.1V power supply and are available in BGA packages.

Specifications

Speed	-E6		-E7		-G8		-F8		Units
	(DDR2-667-CL5)		(DDR2-800-CL5)		(DDR2-1066-CL7)		(DDR2-1066-CL6)		
Parameter	min	max	min	min	min	max	min	max	$tCK_{(Avg.)}$
Clock rate	125	333	125	400	125	533	125	533	MHz
tRCD	15	-	12.5	-	12.5	-	11.25	-	ns
tRP	15	-	12.5	-	12.5	-	11.25	-	ns
tRC	60	-	57.5	-	57.5	-	56.25	-	ns
tRAS	40	70K	40	70K	40	70K	40	70K	ns
tCK(Avg.)@CL3	5	8	5	8	5	8	5	8	ns
tCK(Avg.)@CL4	3.75	8	3.75	8	3.75	8	3.75	8	ns
tCK(Avg.)@CL5	3	8	2.5	8	2.5	8	2.5	8	ns
tCK(Avg.)@CL6	-	-	2.5	8	2.5	8	1.875	8	ns
tCK(Avg.)@CL7	-	-	-	-	1.875	8	1.875	8	ns

Pin Configurations – 60 balls BGA Package (x8)

< TOP View>

x 8

1	2	3		7	8	9
VDD	NU,/RDQS	VSS	A	VSSQ	DQS	VDDQ
DQ6	VSSQ	DM/RDQS	B	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	D	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	WE	F	RAS	CK	ODT
BA2	BA0	BA1	G	CAS	CS	
	A10/AP	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

Pin Configurations – 84 balls BGA Package (x16)

< TOP View>

x 16

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA 1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/ AP	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

Pin Functions

Symbol	Type	Function
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
/CS	Input	Chip Select: All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple memory ranks. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	/RAS, /CAS and /WE (along with /CS) define the command being entered.
DM, LDM, UDM	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS, /RDQS is enabled by EMRS command.
BA0 ~ BA2	Input	Bank Address Inputs: BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 ~ A13	Input	Address Inputs: Provides the row address for Activate commands and the column address and Auto Precharge or Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the precharge applies to one bank (A10=low) or all banks (A10=high). If only one bank is to be precharged, the bank is selected by BA0-BA2. The address inputs also provide the op-code during Mode Register Set commands.A13 Row address use on x8 components only.
DQ	Input/Output	Data Inputs/Output: Bi-directional data bus.
DQS, /DQS LDQS, /LDQS UDQS, /UDQS	Input/Output	Data Strobe: output with read data, input with write data. Edge aligned with read data, centered with write data. For the x16, LDQS corresponds to the data on DQ0 - DQ7; UDQS corresponds to the data on DQ8-DQ15. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with the optional complementary signals /DQS, /LDQS, /UDQS to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables the complementary data strobe signals.

Symbol	Type	Function
RDQS, /RDQS	Input/Output	Read Data Strobe: For x8 components a RDQS and /RDQS pair can be enabled via EMRS(1) for real timing. RDQS and /RDQS is not support x16 components. RDQS and /RDQS are edge-aligned with real data. If enable RDQS and /RDQS then DM function will be disabled.
ODT	Input	On Die Termination: ODT(registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, DQS, /DQS, RDQS, /RDQS, and DM signal for x8 configuration. For x16 configuration ODT is applied to each DQ, UDQS, /UDQS, LDQS, /LDQS, UDM and LDM signal. The ODT pin will be ignored if the EMRS (1) is programmed to disable ODT.
NC		No Connect: No internal electrical connection is present.
VDDQ/VSSQ	Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VDDL/VSSL	Supply	DLL power supply and ground
VDD/VSS	Supply	Power Supply Power and ground for the input buffers and core logic.
VREF	Supply	SSTL_1.8 reference voltage

Command Operations

Command Truth Table

The DDR2 SDRAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

Function	Symbol	CKEn-1	CKEn	BA0	BA1	BA2	A13-A11	A10	A0-A9	/CS	/RAS	/CAS	/WE	Notes
Mode register set	MRS	H	H	L	L	L	MRS OPCODE			L	L	L	L	1
Extended mode register set (1)	EMRS(1)	H	H	H	L	L	EMRS (1) OPCODE			L	L	L	L	1
Extended mode register set (2)	EMRS(2)	H	H	L	H	L	EMRS (2) OPCODE			L	L	L	L	1
Auto refresh	REF	H	H	X	X	X	X	X	X	L	L	L	H	1
Self refresh entry	SELF	H	L	X	X	X	X	X	X	L	L	L	H	1
Self refresh exit	SELFX	L	H	X	X	X	X	X	X	H	X	X	X	1,6
		L	H	X	X	X	X	X	X	L	H	H	H	
Single bank precharge	PRE	H	H	BA			X	L	X	L	L	H	L	1,2
Precharge all banks	PALL	H	H	X	X	X	X	H	X	L	L	H	L	1
Bank activate	ACT	H	H	BA			RA			L	L	H	H	1,2,7
Write	WRIT	H	H	BA			CA	L	CA	L	H	L	L	1,2,3
Write with auto precharge	WRITA	H	H	BA			CA	H	CA	L	H	L	L	1,2,3
Read	READ	H	H	BA			CA	L	CA	L	H	L	H	1,2,3
Read with auto precharge	READA	H	H	BA			CA	H	CA	L	H	L	H	1,2,3
No operation	NOP	H	X	X	X	X	X	X	X	L	H	H	H	1
Device deselect	DESL	H	X	X	X	X	X	X	X	H	X	X	X	1
Power down mode entry	PDEN	H	L	X	X	X	X	X	X	H	X	X	X	1,4
		H	L	X	X	X	X	X	X	L	H	H	H	
Power down mode exit	PDEX	L	H	X	X	X	X	X	X	H	X	X	X	1,4
		L	H	X	X	X	X	X	X	L	H	H	H	

Remark: H = VIH. L = VIL. · = VIH or VIL

Note:

1. All DDR2 commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the cock.

2. Bank select (BA0, BA1), determine which bank is to be operated upon.

3. Burst reads or writes should not be terminated other than specified as “Reads interrupted by a Read” in burst read command [READ] or “Writes interrupted by a Write” in burst write command [WRIT].

4. The power down mode does not perform any refresh operations. The duration of power down is therefore limited by the refresh requirements of the device. Once clock delay is required for mode entry and exit.

5. The state of ODT does not affect the states described in this table. The ODT function is no available during self-refresh.

6. Self-refresh exit is asynchronous.

7. 8-bank devise sequential bank activation restriction: No more than 4 banks may be activated in a rolling tFAW window.

Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if(tFAW/tCK) rounds up to 10 clocks, and an activate command is issue in clock N ,no more than three further activate commands may be issue in clock N+1through N+9.

CKE Truth Table

Current state [*2]	CKEn-1 [*1]	CKEn [*1]	/CS, /RAS, /CAS, /WE	Operation [*3]	Notes
Power down	L	L	X	Maintain power down	11,13,15
	L	H	DESL or NOP	Power down exit	4, 8, 11, 13
Self refresh	L	L	X	Maintain self refresh	11,15
	L	H	DESL or NOP	Self refresh exit	4, 5, 9
Bank Active	H	L	DESL or NOP	Active power down entry	4, 8, 10, 11, 13
All banks idle	H	L	DESL or NOP	Precharge power down entry	4, 8, 10, 11, 13
	H	L	SELF	Self refresh entry	6,9,11,13
Any state other than listed above	H	H	Refer to the Command Truth Table		7

Remark: H = VIH. L = VIL. X = Don't care

Note:

1. CKE (n) is the logic state of CKE at clock n; CKE (n-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. Command (n) is the command registered at clock edge n, and operation (n) is a result of Command (n).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On self-refresh exit, [DESL] or [NOP] commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.
6. Self refresh mode can only be entered from the all banks idle state.
7. Must be a legal command as defined in the command truth table.
8. Valid commands for power down entry and exit are [NOP] and [DESL] only.
9. Valid commands for self refresh exit are [NOP] and [DESL] only.
10. Power down and self-refresh can not be entered while read or write operations, (extended) mode register set operations or precharge operations are in progress. See section Power Down and Self Refresh Command for a detailed list of restrictions.
11. Minimum CKE high time is 3 clocks minimum CKE low time is 3 clocks.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh. See section ODT (On die Termination).
13. The power down does not perform any refresh operations. The duration of power down mode is therefore limited by the refresh requirements outlined in section automatic refresh command.
14. CKE must be maintained high while the SDRAM is in OCD calibration mode.
15. "x" means "don't care" (including floating around VREF) in self refresh and power down. However ODT must be driven high or low in power down if the ODT functions is enabled (bit A2 or A6 set to "1" in EMRS (1)).

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR SDRAM.

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Idle	L	H	L	H	x	DESL	Nop or Power down	
	L	H	L	H	x	NOP	Nop or Power down	
	L	H	L	L	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	L	H	H	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	L	H	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	L	BA, RA	ACT	Row activating	
	L	L	L	H	BA, A10 (AP)	PRE	Precharge	
	L	L	L	H	A10 (AP)	PALL	Precharge all banks	
	L	L	L	L	x	REF	Auto refresh	2
	L	L	L	L	x	SELF	Self refresh	2
	H	×	×	×	BA, MRS-OPCODE	MRS	Mode register accessing	2
	L	H	H	H	BA, EMRS-OPCODE	EMRS(1)(2)	Extended mode register accessing	2
Bank(s) active	L	H	L	H	x	DESL	Nop	
	L	H	L	H	x	NOP	Nop	
	L	H	L	L	BA, CA, A10 (AP)	READ	Begin Read	
	L	H	L	L	BA, CA, A10 (AP)	READA	Begin Read	
	L	L	H	H	BA, CA, A10 (AP)	WRIT	Begin Write	
	L	L	H	L	BA, CA, A10 (AP)	WRITA	Begin Write	
	L	L	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	L	H	BA, A10 (AP)	PRE	Precharge	
	L	L	L	H	A10 (AP)	PALL	Precharge all banks	
	L	L	L	L	x	REF	ILLEGAL	
	L	L	L	L	x	SELF	ILLEGAL	
	H	×	×	×	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	H	H	H	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	
Read	L	H	L	H	x	DESL	Continue burst to end -> Row active	
	L	H	L	H	x	NOP	Continue burst to end -> Row active	
	L	H	L	L	BA, CA, A10 (AP)	READ	Burst interrupt	1,4
	L	H	L	L	BA, CA, A10 (AP)	READA	Burst interrupt	1,4
	L	L	H	H	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	L	H	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	L	H	BA, A10 (AP)	PRE	ILLEGAL	1,8
	L	L	L	H	A10 (AP)	PALL	ILLEGAL	8
	L	L	L	L	x	REF	ILLEGAL	
	L	L	L	L	x	SELF	ILLEGAL	
	L	H	L	H	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	H	L	H	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Write	H	×	×	×	x	DESL	Continue burst to end -> Write recovering	
	L	H	H	H	x	NOP	Continue burst to end -> Write recovering	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	Burst interrupt	1,4
	L	H	L	L	BA, CA, A10 (AP)	WRITA	Burst interrupt	1,4
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1,8
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	8
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	
Read with auto precharge	H	×	×	×	x	DESL	Continue burst to end -> Precharging	
	L	H	H	H	x	NOP	Continue burst to end -> Precharging	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	1,7
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1,7
	L	L	H	H	BA, RA	ACT	ILLEGAL	1,7,8
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	7,8
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	
Write with auto precharge	H	×	×	×	x	DESL	Continue burst to end ->Write recovering with auto precharge	
	L	H	H	H	x	NOP	Continue burst to end ->Write recovering with auto precharge	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	1,7
	L	H	L	L	BA, CA, A10 (AP)	WRIT/WRITA	ILLEGAL	1,7
	L	L	H	H	BA, RA	ACT	ILLEGAL	1,7,8
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	7,8
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Precharging	H	×	×	×	x	DESL	Nop -> Enter idle after tRP	
	L	H	H	H	x	NOP	Nop -> Enter idle after tRP	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	Nop -> Enter idle after tRP	1,8
	L	L	H	L	A10 (AP)	PALL	Nop -> Enter idle after tRP	8
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	
Row activating	H	×	×	×	x	DESL	Nop -> Enter bank active after tRCD	
	L	H	H	H	x	NOP	Nop -> Enter bank active after tRCD	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	1,5
	L	H	L	L	BA, CA, A10 (AP)	WRIT/WRITA	ILLEGAL	1,5
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	
Write recovering	H	×	×	×	x	DESL	Nop -> Enter bank active after tWR	
	L	H	H	H	x	NOP	Nop -> Enter bank active after tWR	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	1,6
	L	H	L	L	BA, CA, A10 (AP)	WRIT/WRITA	New write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Write recovering with auto precharge	H	×	×	×	x	DESL	Nop -> Enter bank active after tWR	
	L	H	H	H	x	NOP	Nop -> Enter bank active after tWR	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT/ERITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	
Refresh	H	×	×	×	x	DESL	Nop -> Enter idle after tRFC	
	L	H	H	H	x	NOP	Nop -> Enter idle after tRFC	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT/ERITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	
Mode register accessing	H	×	×	×	x	DESL	Nop -> Enter idle after tMRD	
	L	H	H	H	x	NOP	Nop -> Enter idle after tMRD	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT/ERITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Extended Mode register accessing	H	×	×	×	x	DESL	Nop -> Enter idle after tMRD	
	L	H	H	H	x	NOP	Nop -> Enter idle after tMRD	
	L	H	L	H	BA, CA, A10 (AP)	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	x	REF	ILLEGAL	
	L	L	L	H	x	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS(1)(2)	ILLEGAL	

Remark: H = VIH. L = VIL. × = VIH or VIL

Note:

1. This command may be issued for other banks, depending on the state of the banks.
2. All banks must be in "IDLE".
3. All AC timing specs must be met.
4. Only allowed at the boundary of 4 bits burst. Burst interruptions at other timings are illegal.
5. Available in case tRCD is satisfied by AL setting.
6. Available in case tWTR is satisfied.
7. The DDR2 SDRAM supports the concurrent auto-precharge feature, a read with auto-precharge enabled,or a write with auto-precharge enabled, may be followed by any column command to other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply. (E.g. Conflict between READ data and WRITE data must be avoided.)

The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank, is summarized below.

From command	To command (different bank, noninterrupting command)	Minimum delay (Concurrent AP supported)	Units
Read w/AP	Read or Read w/AP	BL/2	tCK
	Write or Write w/AP	(BL/2) + 2	tCK
	Precharge or Activate	1	tCK
Write w/AP	Read or Read w/AP	(CL − 1) + (BL/2) + tWTR	tCK
	Write or Write w/AP	BL/2	tCK
	Precharge or Activate	1	tCK

8. The minimum delay from the read, write and precharge command to the precharge command to the same bank is summarized below.

Absolute Maximum Rating

Symbol	Parameters	Rating	Unit	Note
VDD	Voltage on VDD pin relative to VSS	-1.0 ~ 2.3	V	1,3
VDDQ	Voltage on VDDQ pin relative to VSS	-0.5 ~ 2.3	V	1,3
VDDL	Voltage on VDDL pin relative to VSS	-0.5 ~ 2.3	V	1
VIN, VOUT	Voltage on input/output pin relative to VSS	-0.5 ~ 2.3	V	1,2
TSTG	Storage Temperature	- 55 ~ +100	°C	1,3

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6VDDQ, when VDD and VDDQ are less than 500mV; Vref may be equal to or less than 300mV.

Temperature Range

Symbol	Parameters	Rating	Unit	Note
Toper	Normal Operating Temperature Range	0 to 95	°C	1,2
	Industrial Temperature Range	-40 to 95	°C	1

Note:

1. Operating temperature is the case surface temperature (Tcase) on the center/top side of the DRAM.
2. When TOPER exceeds 85℃, it is required to set 3.9us tREFI in auto refresh mode or to set '1' for EMRS(2) bit A7 in self refresh mode.

AC & DC Operating Conditions

DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
VDD	Power Supply Voltage	1.7	1.8	1.9	V	1
VDDQ	Output Supply Voltage	1.7	1.8	1.9	V	5
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	1,5
VREF	Reference Voltage	0.49* VDDQ	0.5* VDDQ	0.51* VDDQ	V	2,3
VTT	Termination Voltage	VREF -0.04	VREF	VREF +0.04	V	4

Note:

1. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak ac noise on VREF may not exceed +/- 2% VREF (dc).
4. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors is expected to be set equal to VREF and must track variations in die dc level of VREF.
5. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ, and VDDL tied together.

ODT DC Electrical Characteristic

Parameter / Condition	Symbol	Min.	Nom.	Max.	Units	Notes
Rtt eff. impedance value for EMRS(1)(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohms	1
Rtt eff. impedance value for EMRS(1)(A6,A2)=0,1; 150 ohm	Rtt2(eff)	120	150	180	ohms	1
Rtt eff. impedance value for EMRS(1)(A6,A2)=1,1; 50 ohm	Rtt3(eff)	40	50	60	ohms	1
Deviation of VM with respect to VDDQ / 2	delta VM	-6		6	%	2

1) Measurement Definition for Rtt (eff):

Apply VIHac and VILac to test pin separately, then measure current I (VIHac) and I (VILac) respectively.

$$Rtt(eff) = \frac{(VIHac - VILac)}{I(VIHac) - I(VILac)}$$

2) Measurement Definition for VM:

Measure voltage (VM) at test pin (midpoint) with no load:

$$\text{delta VM} = \left(\frac{2 * VM}{VDDQ} - 1\right) \times 100\%$$

DC & AC Logic Input Levels

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing is measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the cross point of DQS and its complement, DQS. This distinction in timing methods is guaranteed by design and characterization. In single ended mode, the DQS (and RDQS) signals are internally disabled and don't care.

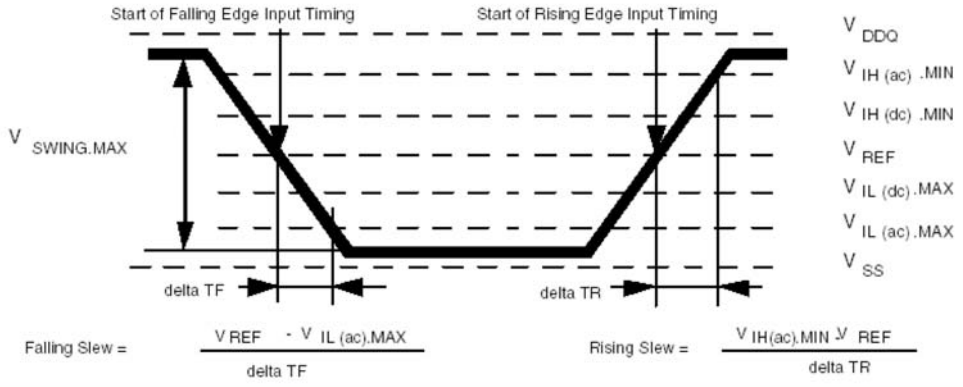
Single-ended DC & AC Logic Input Levels

Symbol	Parameter	DDR2-667/800/1066		Units
		Min.	Max.	
$V_{IH\ (dc)}$	DC input logic high	VREF + 0.125	VDDQ + 0.3	V
$V_{IL\ (dc)}$	DC input low	-0.3	VREF - 0.125	V
$V_{IH\ (ac)}$	AC input logic high	VREF + 0.200	VDDQ+Vpeak	V
$V_{IL\ (ac)}$	AC input low	VSSQ-Vpeak	VREF - 0.200	V

Single-ended AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1, 2
$V_{SWING(max)}$	Input signal maximum peak to peak swing	1	V	1, 2
SLEW	Input signal minimum slew rate	1	V / ns	3, 4

1. This timing and slew rate definition is valid for all single-ended signals except tIS, tIH, tDS, and tDH.
2. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
3. The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)max}$ to $V_{IH(ac)min}$ for rising edges and the range from $V_{IH(dc)min}$ to $V_{IL(ac)max}$ for falling edges as shown in the below figure.
4. AC timings are referenced with input waveforms switching from $V_{IL\ (ac)}$ to $V_{IH\ (ac)}$ on the positive transitions and $V_{IH\ (ac)}$ to $V_{IL\ (ac)}$ on the negative transitions.



Differential DC and AC Input and Output Logic Levels

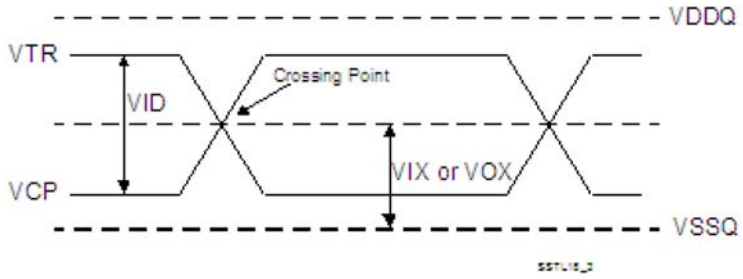
Symbol	Parameter	Min.	Max.	Units	Notes
$V_{ID(ac)}$	AC differential input voltage	0.5	VDDQ	V	1
$V_{IX(ac)}$	AC differential cross point input voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2
$V_{OX(ac)}$	AC differential cross point output voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	3

Notes:

1) $V_{ID\ (ac)}$ specifics the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$.

2) $V_{IX\ (ac)}$ specifices the input differential voltage IVTR-VCPI required for switching, where VTR is the true input (such as CK, DQS, LDQS, or UDQS) level and VCP is the complementary input (such $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$, or $\overline{UDQS}$) level. The minimum value is equal to $V_{IH\ (DC)}$ - $V_{IL\ (DC)}$.

3) The typical value of $V_{OX\ (AC)}$ is expected to be about 0.5V_{DDQ} of the transmitting device and $V_{OX\ (AC)}$ is expected to track variations in V_{DDQ}. $V_{OX\ (AC)}$ indicates the voltage at which differential signals must cross.



Output Buffer Levels

Output AC Test Conditions

Symbol	Parameter	SSTL-18 Class II	Units	Notes
V_{OTR}	Output Timing Measurement Reference Level	0.5 * VDDQ	V	1
1. The VDDQ of the device under test is referenced.				

Output DC Current Drive

Symbol	Parameter	SSTL-18	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current, nominal	-13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current, nominal	13.4	mA	2, 3, 4

1. V_{DDQ} = 1.7 V; V_{OUT} = 1.42 V. (V_{OUT}-V_{DDQ}) / I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.

2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT} / I_{OL} must be less than 21 ohm for values of V_{OUT} between 0V and 280 mV.

3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}

4. The values of $I_{OH\ (dc)}$ and $I_{OL\ (dc)}$ are based on the conditions given in note 1 and 2. They are used to test drive current capability to ensure $V_{IHmin.}$ Plus a noise margin and $V_{ILmax.}$ Minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 ohm load line to define a convenient current for measurement.

OCD Default Setting Table

Symbol	Description	Min.	Nominal	Max.	Unit	Notes
-	Pull-up / Pull down mismatch	0	-	4	Ohms	6
-	Output Impedance step size for OCD calibration	0	-	1.5	Ohms	1,2,3
S_{OUT}	Output Slew Rate	1.5	-	5	V / ns	1,4,5,7,8

1) Absolute Specification: T_{OPER}; V_{DDQ} = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V.

2) Impedance measurement condition for output source dc current: V_{DDQ} = 1.7V, V_{OUT} = 1420 mV; (V_{OUT}-V_{DDQ})/I_{OH} must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and V_{DDQ}-280mV. Impedance measurement condition for output sink dc current: V_{DDQ} = 1.7 V; V_{OUT} = -280mV; V_{OUT} / I_{OL} must be less than 23.4 ohms for values of V_{OUT} between 0V and 280 mV.

3) Mismatch is absolute value between pull-up and pull-down; both are measured at same temperature and voltage.

4) Slew rates measured from $V_{IL\ (AC)}$ to $V_{IH\ (AC)}$ with the load specified in Section 8.2.

5) The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

6) This represents the step size when the OCD is near 18 ohms at nominal conditions across all process parameters and represents only the DRAM uncertainty. A 0 Ohm value (no calibration) can only be achieved if the OCD impedance is 18 ± 0.75 ohms under nominal conditions.

7) DRAM output slew rate specification applies to 533Mb/s, 667Mb/s, and 800Mb/s speed pin.

8) Timing skew due to DRAM output slew rate mis-match between DQS / $\overline{DQS}$ and associated DQ's is included in tDQSQ and tQHS specification.

Default Output V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS (1) bits A7~A9 = '111'. The driver characteristics evaluation conditions area) Nominal Default 25℃ (Tcase), VDDQ=1.8V, typical process. B) Minimum $T_{OPER(max)}$, VDDQ=1.7V, slow-slow process. C) Maximum 0℃ (Tcase), VDDQ=1.9V, fast-fast process.

Full Strength Default Pull up Driver Characteristics

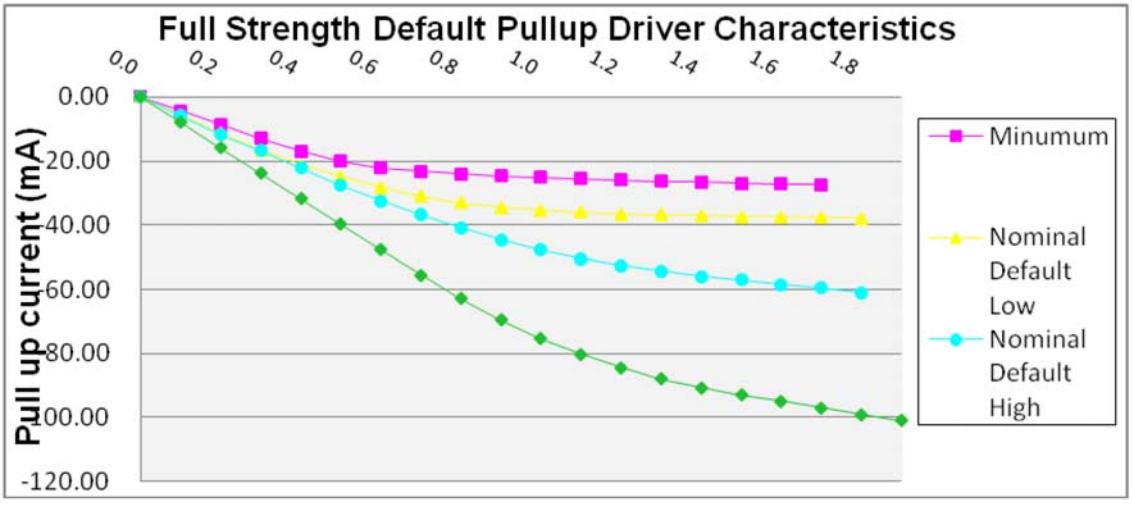
Voltage (V)	Minimum (23.4 Ohms)	Normal Default low (18 Ohms)	Normal Default high (18 Ohms)	Maximum (12.6 Ohms)
0.0	0.00	0.00	0.00	0.00
0.1	-4.30	-5.65	-5.90	-7.95
0.2	-8.60	-11.30	-11.80	-15.90
0.3	-12.90	-16.50	-16.80	-23.85
0.4	-16.90	-21.20	-22.10	-31.80
0.5	-20.05	-25.00	-27.60	-39.75
0.6	-22.10	-28.30	-32.40	-47.70
0.7	-23.27	-30.90	-36.90	-55.55
0.8	-24.10	-33.00	-40.90	-62.95
0.9	-24.73	-34.50	-44.60	-69.55
1.0	-25.23	-35.50	-47.70	-75.35
1.1	-25.65	-36.10	-50.40	-80.35
1.2	-26.02	-36.60	-52.60	-84.55
1.3	-26.35	-36.90	-54.20	-87.95
1.4	-26.65	-37.10	-55.90	-90.70
1.5	-26.93	-37.40	-57.10	-93.00
1.6	-27.20	-37.60	-58.40	-95.05
1.7	-27.46	-37.70	-59.60	-97.05
1.8	-	-37.90	-60.90	-99.05
1.9	-	-	-	-101.05

The driver characteristics evaluation conditions are:

Nominal Default 25℃ (Tcase) , VDDQ = 1.8 V, typical process

Minimum Toper(max.), VDDQ = 1.7V, slow-slow process

Maximum 0 ℃ (Tcase). VDDQ = 1.9 V, fast-fast process



Full Strength Default Pull down Driver Characteristics

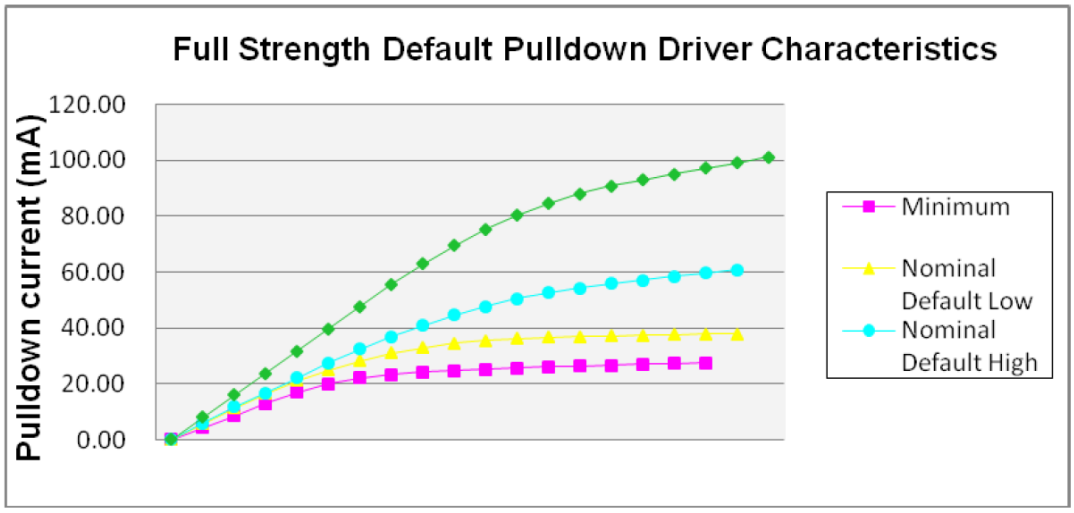
Voltage (V)	Minimum (23.4 Ohms)	Normal Default low (18 Ohms)	Normal Default high (18 Ohms)	Maximum (12.6 Ohms)
0.0	0.00	0.00	0.00	0.00
0.1	4.30	5.65	5.90	7.95
0.2	8.60	11.30	11.80	15.90
0.3	12.90	16.50	16.80	23.85
0.4	16.90	21.20	22.10	31.80
0.5	20.05	25.00	27.60	39.75
0.6	22.10	28.30	32.40	47.70
0.7	23.27	30.90	36.90	55.55
0.8	24.10	33.00	40.90	62.95
0.9	24.73	34.50	44.60	69.55
1.0	25.23	35.50	47.70	75.35
1.1	25.65	36.10	50.40	80.35
1.2	26.02	36.60	52.60	84.55
1.3	26.35	36.90	54.20	87.95
1.4	26.65	37.10	55.90	90.70
1.5	26.93	37.40	57.10	93.00
1.6	27.20	37.60	58.40	95.05
1.7	27.46	37.70	59.60	97.05
1.8	-	37.90	60.90	99.05
1.9	-	-	-	101.05

The driver characteristics evaluation conditions are:

Nominal Default 25℃ (Tcase) , VDDQ = 1.8 V, typical process

Minimum Toper(max.), VDDQ = 1.7V, slow-slow process

Maximum 0 ℃ (Tcase). VDDQ = 1.9 V, fast-fast process



Calibrated Output Driver V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in the Off-Chip Driver (OCD) Impedance Adjustment. The following tables show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohms step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves are represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figure. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy and uncertainty with DQ to DQ variation, it is recommend that only the default values to be used. The nominal maximum ad minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa.

Full Strength Calibrated Pull down Driver Characteristics

Voltage (V)	Nominal Minimum (21 Ohms)	Normal Low (18.75 Ohms)	Nominal (18 ohms)	Normal High (17.25 Ohms)	Nominal Maximum (15 Ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

The driver characteristics evaluation conditions are:

Nominal 25℃ (Tcase) , VDDQ = 1.8 V, typical process

Nominal Low and Nominal High 25℃ (Tcase), VDDQ = 1.8V, any process

Nominal Minimum Toper(max), VDDQ = 1.7 V, any process

Nominal Maximum 0℃(Tcase), VDDQ = 1.9 V, any process

Full Strength Calibrated Pull up Driver Characteristics

Voltage (V)	Nominal Minimum (21 Ohms)	Normal Low (18.75 Ohms)	Nominal (18 ohms)	Normal High (17.25 Ohms)	Nominal Maximum (15 Ohms)
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.6	-17.4	-20.0
0.4	-18.7	-21.0	-21.6	-23.0	-27.0

The driver characteristics evaluation conditions are:

Nominal 25℃ (Tcase) , VDDQ = 1.8 V, typical process

Nominal Low and Nominal High 25℃(Tcase), VDDQ = 1.8V, any process

Nominal Minimum Toper(max), VDDQ = 1.7 V, any process

Nominal Maximum 0℃ (Tcase), VDDQ = 1.9 V, any process

Capacitance (V_{DD} = 1.8V ± 0.1V, T_A = 25°C)

Symbol	Parameter	-3C/3CI		-AC/ACI/-ACL		-BE		-BD		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CCK	Input capacitance, CK and $\overline{CK}$	1.0	2.0	1.0	2.0	1.0	2.0	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	-	0.25	-	0.25	-	0.25	-	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	2.0	1.0	1.75	1.0	1.75	1.0	1.75	pF
CDI	Input capacitance delta, all other input-only pins	-	0.25	-	0.25	-	0.25	-	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	2.5	3.5	2.5	3.5	2.5	3.5	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	-	0.5	-	0.5	-	0.5	-	0.5	pF

Power & Ground Clamp V-I Characteristics

Power and Ground clamps are provided on address (A0~A13, BA0, BA1, BA2), /RAS, /CAS, /CS, WE, CKE and ODT pins. The V-I characteristics for pins with clamps is shown in the following table

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0.0	0.0
0.1	0.0	0.0
0.2	0.0	0.0
0.3	0.0	0.0
0.4	0.0	0.0
0.5	0.0	0.0
0.6	0.0	0.0
0.7	0.0	0.0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

DC Characteristics 1 (V_{DD} / V_{DDQ} = 1.8V ± 0.1V, V_{SS} / V_{SSQ} = 0V)

Parameter/Test condition		Symbol	Max.			Unit
			E6	E7	F8/G8	
OPERATING CURRENT: One bank; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS min.(IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	x4/x8	IDD0	70	75	90	mA
	x16		110	120	140	
OPERATING CURRENT: One bank; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS min.(IDD); tRCD = tRCD (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	x4/x8	IDD1	80	90	110	
	x16		130	140	160	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2P	10	10	10	
PRECHARGE QUIET STANDBY CURRENT: All banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	x4/x8	IDD2Q	30	35	45	
	x16		50	60	75	
IDLE STANDBY CURRENT: All banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	x4/x8	IDD2N	35	40	50	
	x16		55	65	80	
ACTIVE POWER DOWN STANDBY CURRENT: All banks open; tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	IDD3P-F	25	30	40	
	Fast PDN Exit MRS(12) = 1	IDD3P-S	10	10	15	
ACTIVE STANDBY CURRENT: All banks open; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	x4/x8	IDD3N	50	55	65	
	x16		70	80	95	
OPERATING CURRENT: All banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	x4/x8	IDD4R	120	140	160	
	x16		170	250	300	

Parameter/Test condition		Symbol	Max.			Unit
			E6	E7	F8/G8	
OPERATING CURRENT: All banks open, continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	x4/x8	IDD4W	120	140	160	mA
	x16		170	250	300	
BURST AUTO REFRESH CURRENT: tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	x4/x8	IDD5B	180	195	230	
	x16		220	230	280	
Distributed AUTO REFRESH CURRENT		IDD5D	20	20	20	
SELF REFRESH CURRENT: Self Refresh Mode; CK and /CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		IDD6	10	10	10	
Operating current (Bank interleaving): All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD (IDD) −1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD(IDD), tRCD = 1 × tCK (IDD); CKE is H, CS is H between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4W	x4/x8	IDD7	230	270	320	
	x16		280	350	420	

Note:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Input Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, /DQS, RDQS, /RDQS, LDQS, /LDQS, UDQS and /UDQS. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD

   L is defined as VIN ≤ VIL (AC) (max.)

   H is defined as VIN ≥ VIH (AC) (min.)

   STABLE is defined as inputs stable at an H or L level

   FLOATING is defined as inputs at VREF = VDDQ/2

   SWITCHING is defined as:

   inputs changing between H and L every other clock cycle (once per two clocks) for address and control signals, and inputs changing between H and L every other data transfer (once per clock) for DQ signals not including masks or strobes.
6. Refer to AC Timing for IDD Test Conditions.

DC Characteristics 2 (V_{DD} / V_{DDQ} = 1.8V ± 0.1V, V_{SS} / V_{SSQ} = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
VOTR	Output timing measurement reference level	–	0.5 x VDDQ	–		5
IOH	Output High Current	-13.4	–	–	mA	1,3,4
IOL	Output Low Current	13.4	–	–	mA	2,3,4

Note:

1. VDDQ = 1.7 V; VOUT = 1.42 V. (VOUT-VDDQ) / IOH must be less than 21 ohm for values of VOUT between VDDQ and VDDQ - 280 mV.
2. VDDQ = 1.7 V; VOUT = 280 mV. VOUT / IOL must be less than 21 ohm for values of VOUT between 0V and 280 mV.
3. The dc value of VREF applied to the receiving device is set to VTT.
4. The values of IOH(dc) and IOL(dc) are based on the conditions given in note 1 and 2. They are used to test drive current capability to ensure VIHmin. plus a noise margin and VILmax. minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21ohm load line to define a convenient current for measurement.

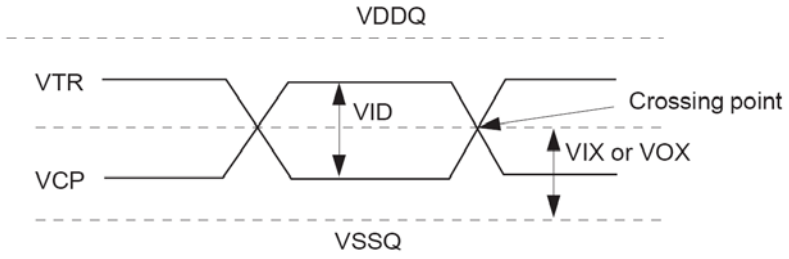
DC Characteristics 3

(V_{DD} / V_{DDQ} = 1.8V ± 0.1V, V_{SS} / V_{SSQ} = 0V)

Symbol	Parameter	Min	Max	Unit	Note
VID	AC differential input voltage	0.5	VDDQ	V	1
VIX	AC differential cross point voltage	0.5 × VDDQ − 0.175	0.5 × VDDQ + 0.175	V	2
VOX	AC differential cross point voltage	0.5 × VDDQ − 0.125	0.5 × VDDQ + 0.125	V	3

Note:

1. VID(ac) specify the allowable DC execution of each input of differential pair such as CK, /CK, DQS, /DQS, LDQS, /LDQS, UDQS, and /UDQS
2. VIX(ac) specify the input differential voltage IVTR-VCPI required for switching, where VTR is the true input (such as CK, DQS, LDQS, or UDQS) level and VCP is the complementary input (such /CK, /DQS, /LDQS, or /UDQS) level. The minimum value is equal to VIH(DC) - VIL(DC).
3. The typical value of VOX(AC) is expected to be about 0.5VDDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ. VOX(AC) indicates the voltage at which differential signals must cross.



Differential Signal Levels*[1, 2]

ODT DC Electrical Characteristics

(V_{DD} / V_{DDQ} = 1.8V ± 0.1V, V_{SS} / V_{SSQ} = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
Rtt1(eff)	Rtt effective impedance value for EMRS (A6, A2) = 0, 1; 75 Ω	60	75	90	Ω	1
Rtt2(eff)	Rtt effective impedance value for EMRS (A6, A2) = 1, 0; 150 Ω	120	150	180	Ω	1
Rtt3(eff)	Rtt effective impedance value for EMRS (A6, A2) = 1, 1; 50 Ω	40	50	60	Ω	1
ΔVM	Deviation of VM with respect to VDDQ/2	- 6	–	+ 6	%	1

Note:

1. Test condition for Rtt measurements

Measurement Definition for Rtt(eff)

Apply VIH (AC) and VIL (AC) to test pin separately, then measure current I(VIH(AC)) and I(VIL(AC)) respectively. VIH(AC), and VDDQ values defined in SSTL_18.

$$Rtt(eff) = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

Measurement Definition for ΔVM

Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1 \right) \times 100\%$$

ODT Default Characteristics

(V_{DD} / V_{DDQ} = 1.8V ± 0.1V, V_{SS} / V_{SSQ} = 0V)

Parameter	Min.	Typ.	Max.	Unit	Note
Pull-up / Pull down mismatch	0	–	4	Ω	6
Output Impedance step size for OCD calibration	0	–	1.5	Ω	1,2,3
Output Slew Rate	1.5	–	5	V/ns	1,4,5,7,8

Note:

1. Absolute Specification: TOPEN; VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V.
2. Impedance measurement condition for output source dc current: VDDQ = 1.7V, VOUT = 1420 mV; (VOUT-VDDQ)/IOH must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7 V; VOUT = -280mV; VOUT / IOL must be less than 23.4 ohms for values of VOUT between 0V and 280 mV.
3. Mismatch is absolute value between pull-up and pull-down; both are measured at same temperature and voltage.
4. Slew rates measured from VIL(AC) to VIH(AC) with the load specified in Section 8.2.
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

6. This represents the step size when the OCD is near 18 ohms at nominal conditions across all process parameters and represents only the DRAM uncertainty. A 0 Ohm value (no calibration) can only be achieved if the OCD impedance is 18 ± 0.75 ohms under nominal conditions.
7. DRAM output slew rate specification applies to 533MT/s, 667MT/s, and 800MT/s speed pin.
8. Timing skew due to DRAM output slew rate mis-match between DQS, /DQS and associated DQ's is included in tDQSQ and tQHS specification.

AC Timing for IDD Test Conditions

For purposes of IDD testing, the following parameters are to be utilized.

Parameter	DDR2-667	DDR2-800	DDR2-1066	DDR2-1066	Unit
CL	5	5	7	6	ns
tRCD	15	12.5	13.125	11.25	ns
tRC	60	57.5	58.125	56.25	ns
tRRD (x8)	7.5	7.5	7.5	7.5	ns
tRRD (x16)	10	10	10	10	ns
tCK	3	2.5	1.875	1.875	ns
tRAS (min.)	45	45	45	45	ns
tRAS (max.)	70000	70000	70000	70000	ns
tRP	15	12.5	13.125	11.25	ns
tRFC	127.5	127.5	127.5	127.5	ns

Refresh Parameters

Parameter	Symbol	Component Type		1Gb	Unit
Auto-Refresh to Active / Auto-Refresh command period	tRFC	All		127.5	ns
Average periodic Refresh interval	tREFI	Standard Grade	(0℃ ≦ Tcase ≦ 85℃)	7.8	μs
			(85℃ ≦ Tcase ≦ 95℃)	3.9	
		Industry Grade	(-40℃ ≦ Tcase ≦ 95℃)	7.8	μs

AC Characteristics

(V_{DD} / V_{DDQ} = 1.8V ± 0.1V, V_{SS} / V_{SSQ} = 0V)

Symbol	Parameter	E6		E7		F8/G8		Unit
		Min	Max	Min	Max	Min	Max	
tCK(avg.)	Clock cycle time, (Average)	3000	8000	2500	8000	1875	8000	ps
tCH	Clock high level width	0.48	0.52	0.48	0.52	0.48	0.52	tCK
tCL	Clock low level width	0.48	0.52	0.48	0.52	0.48	0.52	tCK
WL	Write command to DQS associated clock edge	RL – 1						nCK
tDSS	DQS falling edge to CK setup time	0.2	–	0.2	–	0.2	–	tCK
tDSH	DQS falling edge hold time from CK	0.2	–	0.2	–	0.2	–	tCK
tDQSH	DQS input high pulse width	0.35	–	0.35	–	0.35	–	tCK
tDQSL	DQS input low pulse width	0.35	–	0.35	–	0.35	–	tCK
tWPRE	Write preamble	0.35	–	0.35	–	0.35	–	tCK
tWPST	Write postamble	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tIH	Address and control input hold time	275	–	250	–	200	–	ps
tIS	Address and control input setup time	200	–	175	–	125	–	ps
tIPW	Control and Address input pulse width for each input	0.6	–	0.6	–	0.6	–	tCK
tDH	DQ and DM input hold time	175	–	125	–	75	–	ps
tDS	DQ and DM input setup time	100	–	50	–	50	–	ps
tDIPW	DQ and DM input pulse width for each input	0.35	–	0.35	–	0.35	–	tCK
tAC	DQ output access time from CK, /CK	-450	+450	-400	+400	-350	+350	ps
tDQSCK	DQS output access time from CK, /CK	-400	+400	-350	+350	-350	+350	ps
tHZ	Data-out high-impedance time from CK,/CK	–	tAC max.	–	tAC max.	–	tAC max.	ps
tLZ(DQS)	Data-out low-impedance time from CK,/CK	tAC min.	tAC max.	tAC min.	tAC max.	tAC min.	tAC max.	ps

Symbol	Parameter		E6		E7		F8/G8		Unit
			Min	Max	Min	Max	Min	Max	
tLZ(DQ)	DQ low-impedance time form CK, /CK		2×tAC min	tAC max.	2×tAC min	tAC max.	2×tAC min	tAC max.	ps
tDQSQ	DQS-DQ skew for DQS and associated DQ signals		–	240	–	200	–	175	ps
tHP	CK half period		tCLmin or tCHmin	–	tCLmin or tCHmin	–	tCLmin or tCHmin	–	ps
tQHS	DQ hold skew factor		–	340	–	300	–	250	ps
tQH	DQ/DQS output hold time from DQS		tHP – tQHS	–	tHP – tQHS	–	tHP – tQHS	–	ps
tRPRE	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	tCK
tRPST	Read postamble		0.4	0.6	0.4	0.6	0.4	0.6	tCK
tRRD	Active bank A to active bank B command period	x4/x8	7.5	–	7.5	–	7.5	–	ns
		x16	10	–	10	–	10	–	ns
tFAW	Four active window period	x4/x8	37.5	–	35	–	35	–	ns
		x16	50	–	45	–	35	–	ns
tRAS	Active-to-Precharge delay		40	70K	40	70K	40	70K	ns
tCCD	/CAS to /CAS command delay		2	–	2	–	2	–	nCK
tWR	Write recovery time		15	–	15	–	15	–	ns
tDAL	Auto precharge write recovery + precharge time		WR + tnRP	–	WR + tnRP	–	WR + tnRP	–	nCK
tWTR	Internal write to read command delay		7.5	–	7.5	–	7.5	–	ns
tRTP	Internal read to precharge command delay		7.5	–	7.5	–	7.5	–	ns
tCKE	CKE minimum pulse width (high and low pulse width)		3	–	3	–	3	–	nCK
tXSNR	Exit self refresh to a non-read command		tRFC + 10	–	tRFC + 10	–	tRFC + 10	–	ns

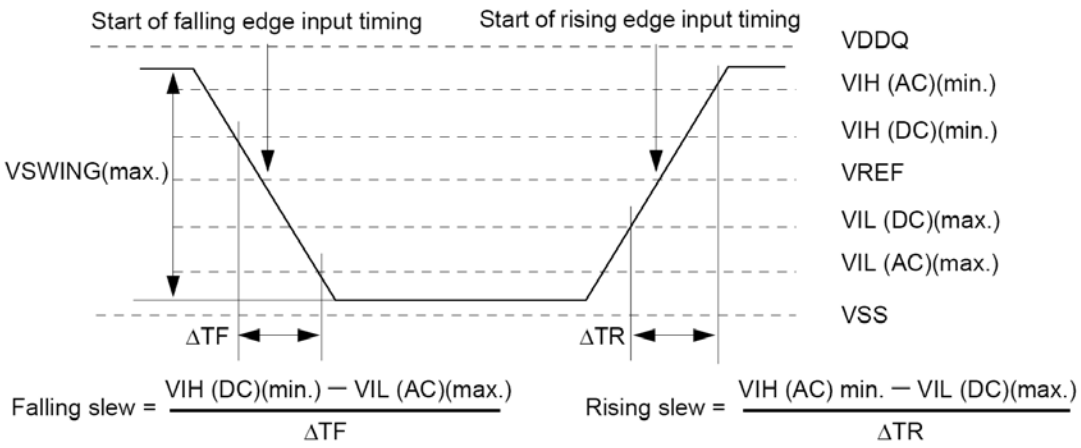
Symbol	Parameter	E6		E7		F8/G8		Unit
		Min	Max	Min	Max	Min	Max	
tXSRD	Exit self refresh to a read command	200	–	200	–	200	–	nCK
tXP	Exit precharge power down to any non-read command	2	–	2	–	3	–	nCK
tXARD	Exit active power down to read command	2	–	2	–	3	–	nCK
tXARDS	Exit active power down to read command (slow exit/low power mode)	7–AL	–	8–AL	–	10–AL	–	nCK
tAON	ODT turn-on	tACmin	tACmax + 0.7	tACmin	tACmax + 0.7	tACmin	tACmax + 2.575	ns
tAONPD	ODT turn-on (Power-Down mode)	tACmin + 2	2 x tCK + tACmax + 1	tACmin + 2	2 x tCK + tACmax + 1	tACmin + 2	2 x tCK + tACmax + 1	ns
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	nCK
tAOF	ODT turn-off	tACmin	tACmax + 0.6	tACmin	tACmax + 0.6	tACmin	tACmax + 0.6	ns
tAOFPD	ODT turn-off (Power-Down mode)	tACmin + 2	2.5 x tCK + tACmax + 1	tACmin + 2	2.5 x tCK + tACmax + 1	tACmin + 2	2.5 x tCK + tACmax + 1	ns
tANPD	ODT to power down entry latency	3	–	3	–	2.5	–	nCK
tAXPD	ODT power down exit latency	8	–	8	–	11	–	nCK
tMRD	Mode register set command cycle time	2	–	2	–	2	–	nCK
tMOD	MRS command to ODT update delay	0	12	0	12	0	12	ns
tOIT	Output impedance test driver delay	0	12	0	12	0	12	ns
tDELAY	Minimum time clocks remains ON after CKE asynchronously drops low	tIS + tCK + tIH	–	tIS + tCK + tIH	–	tIS + tCK + tIH	–	ns

AC Input Test Conditions

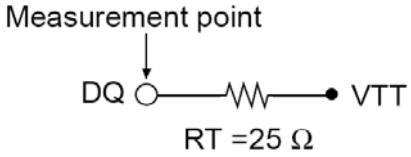
Symbol	Parameter	Value	Unit	Note
VREF	Input reference voltage	0.5 × VDDQ	V	1,2
VSWING(max.)	Input signal maximum peak to peak swing	1.0	V	1,2
SLEW	Input signal maximum slew rate	1.0	V/ns	3,4

Note:

1. This timing and slew rate definition is valid for all single-ended signals except tis, tih, tds, tdh.
2. Input waveform timing is referenced to the input signal crossing through the VREF level applied to the device under test.
3. The input signal minimum slew rate is to be maintained over the range from VIL(dc)max to VIH(ac)min for rising edges and the range from VIH(dc)min to VIL(ac)max for falling edges as shown in the below figure.
4. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



AC Input Test Signal Wave forms



Output Load

Functional Description

The 1Gb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. The 1Gb DDR SDRAM is internally configured as a octal-bank DRAM.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Activate command, which is followed by a Read or Write command. The address bits registered coincident with the activate command are used to select the bank and row to be accesses (BA0, BA1, & BA2 select the banks, A0-A13 select the row for x4 and x8 components, A0-A12 select the row for x16 components). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the Auto-Precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

Power-up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence is required for POWER UP and Initialization.

1. Either one of the following sequence is required for Power-up.

While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT at a Low state (all other inputs may be unde-fined) The VDD voltage ramp time must be no greater than 200ms from when VDD ramps from 300mV to VDD min; and during the VDD voltage ramp up, IVDD-VDDQI $\leqq$ 0.3 volts. Once the ramping of the supply voltages is complete (when VDDQ crosses VDDQ min), the supply voltage specifications in Re-commanded DC operating conditions table.

- VDD, VDDL, and VDDQ are driven from a signal power converter output, AND

- VTT is limited to 0.95V max, AND

- Vref tracks VDDQ/2; Vref must be within ±300mV with respect to VDDQ/2 during supply ramp time.

- VDDQ>=VREF must be met at all times.

While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT at a Low state, all other inputs may be undefined, voltage levels at I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, VDD $\geqq$ VDDL $\geqq$ VDDQ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete, which is when VDDQ crosses VDDQ min. Once the ramping of the supply voltages is complete, the supply voltage specifications provided in Re-commanded DC operating conditions table.

- Apply VDD/VDDL before or at the same time as VDDQ.

- VDD/VDDL voltage ramp time must be no greater than 200ms from when VDD ramps from 300mV to VDDmin.

- Apply VDDQ before or at the same time as VTT.

- The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500ms. (Note: While VDD is ramping, current may be supplied from VDD through the DRAM to VDDQ.)

- Vref must track VDDQ/2; Vref must be within ±300mV with respect to VDDQ/2 during supply ramp time.

- VDDQ $\geqq$ VREF must be met at all time.

- Apply VTT.

2. Start clock (CK, /CK) and maintain stable condition.

3. For the minimum of 200us after stable power (VDD, VDDL, VDDQ, VREF, and VTT are between their minimum and maximum values as stated in Re-commanded DC operating conditions table, and stable clock,

then apply NOP or Deselect & take CKE HIGH.

4. Waiting minimum of 400ns then issue pre-charge all command. NOP or Deselect applied during 400ns period.

5. Issue an EMRS command to EMR (2). (Provide LOW to BA0 and BA2, and HIGH to BA1).

6. Issue an EMRS command to EMR (3). (Provide LOW to BA2 and HIGH to BA0 and BA1).

7. Issue EMRS to enable DLL. (Provide Low to A0, HIGH to BA0 and LOW to BA1-BA2 and A13-A15. And A9=A8=A7=LOW must be used when issuing this command.)

8. Issue a Mode Register Set command for DLL reset. (Provide HIGH to A8 and LOW to BA0-BA2, and A13-A15.)

9. Issue a precharge all command.

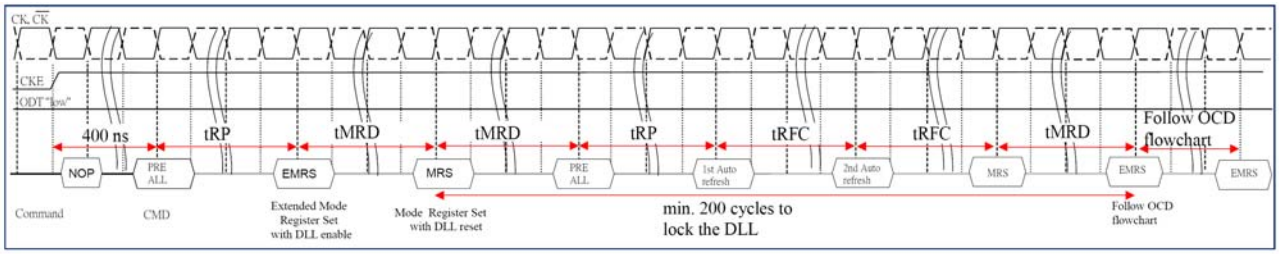
10. Issue 2 more auto-refresh commands.

11. Issue a MRS command with LOW to A8 to initialize device operation (i.e. to program operating parameters without resetting the DLL.)

12. At least 200 clocks after step 7, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRs to EMR (1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR (1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).

13. The DDR2 DRAM is now ready for normal operation.

* To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.



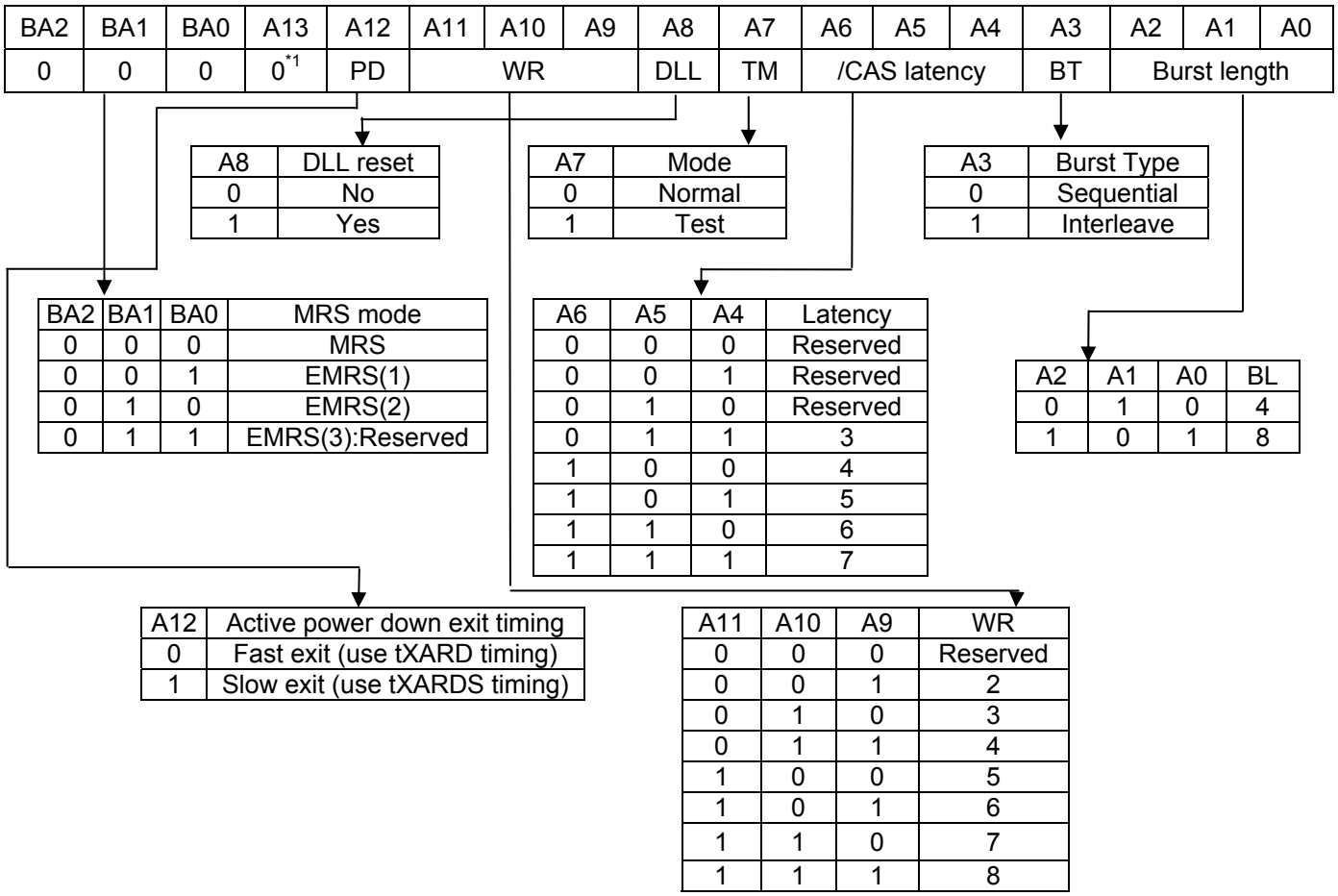
Programming the Mode Registration and Extended Mode Registers

For application flexibility, burst length, burst type, /CAS latency, DLL reset function, write recovery time (tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive /CAS latency, driver impedance, ODT (On Die Termination), single-ended strobe and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) and Extended Mode Registers (EMR (#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued. MRS, EMRS and DLL Reset do not affect array contents, which mean re-initialization including those can be executed any time after power-up without affecting array contents.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls /CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0 and BA1, while controlling the state of address pins A0 ~ A13. The DDR2 SDRAM should be in all banks precharged (idle) mode with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharged state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst length. Burst address sequence type is defined by A3 and /CAS latency is defined by A4 ~ A6. A7 is used for test mode and must be set to low for normal MRS operation. A8 is used for DLL reset. A9 ~ A11 are used for write recovery time (WR) definition for Auto-Precharge mode.

MRS Mode Register Operation Table



BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0*1	PD	WR			DLL	TM	/CAS latency			BT	Burst length		

A8	DLL reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

BA2	BA1	BA0	MRS mode
0	0	0	MRS
0	0	1	EMRS(1)
0	1	0	EMRS(2)
0	1	1	EMRS(3):Reserved

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

A2	A1	A0	BL
0	1	0	4
1	0	1	8

A12	Active power down exit timing
0	Fast exit (use tXARD timing)
1	Slow exit (use tXARDS timing)

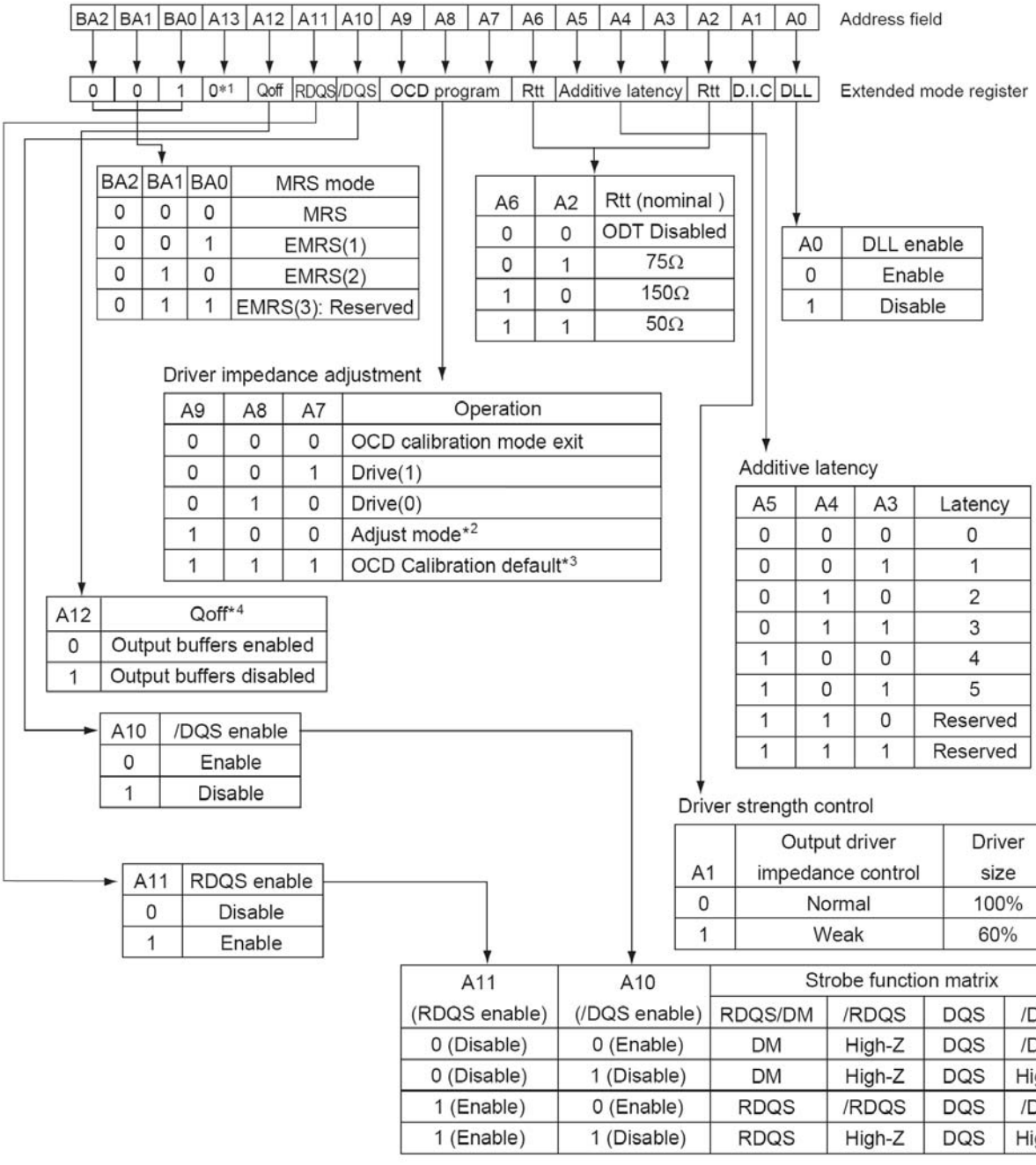
A11	A10	A9	WR
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Note:

1. A13 are reserved for future use and must be programmed to 0 when setting the mode register.
2. WR (min.) (Write Recovery for autoprecharge) is determined by tCK (max.) and WR (max.) is determined by tCK (min.).
   WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR [cycles] = tWR (ns) / tCK (ns)).
   The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Extended Mode Register Set -EMRS (1)

The extended mode register EMRS(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, /DQS disable, OCD program, RQDS enable. The default value of the extended mode register EMRS(1) is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA1 and high on BA0, while controlling the state of the address pins. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the EMRS (1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3-A5 determines the additive latency, A7-A9 are used for OCD control, A10 is used for /DQS disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.



Note:

1. A13 are reserved for future use, and must be programmed to 0 when setting the extended mode register.
2 When adjust mode is issued, AL from previously set value must be applied.
3. After setting to default, OCD mode needs to be exited by setting A9 to A7 to 000.
   Refer to the chapter Off-Chip Driver (OCD)Impedance Adjustment for detailed information.
4. Output disabled - DQ, DQS, /DQS, RDQS, /RDQS. This feature is used in conjunction with DIMM.
   IDD measurements when IDDQ is not desired to be included.

Single-ended and Differential Data Strobe Signals

The following table lists all possible combinations for DQS, /DQS, RDQS, /RDQS which can be programmed by A10 & A11 address bits in EMRS(1). RDQS and /RDQS are available in x8 components only. If RDQS is enabled in x8 components, the DM function is disabled. RDQS is active for reads and don" t care for writes.

EMRS (1)		Strobe Function Matrix				
A11 (RDQS Enable)	**A10 (/DQS Enable)**	**RDQS/DM**	**/RDQS**	**DQS**	**/DQS**	**Signaling**
0 (Disable)	0 (Enable)	DM	Hi-Z	DQS	/DQS	differential DQS signals
0 (Disable)	1 (Disable)	DM	Hi-Z	DQS	Hi-Z	single-ended DQS signals
1 (Enable)	0 (Enable)	RDQS	/RDQS	DQS	/DQS	differential DQS signals
1 (Enable)	1 (Disable)	RDQS	Hi-Z	DQS	Hi-Z	single-ended DQS signals

DLL Enable/Disable

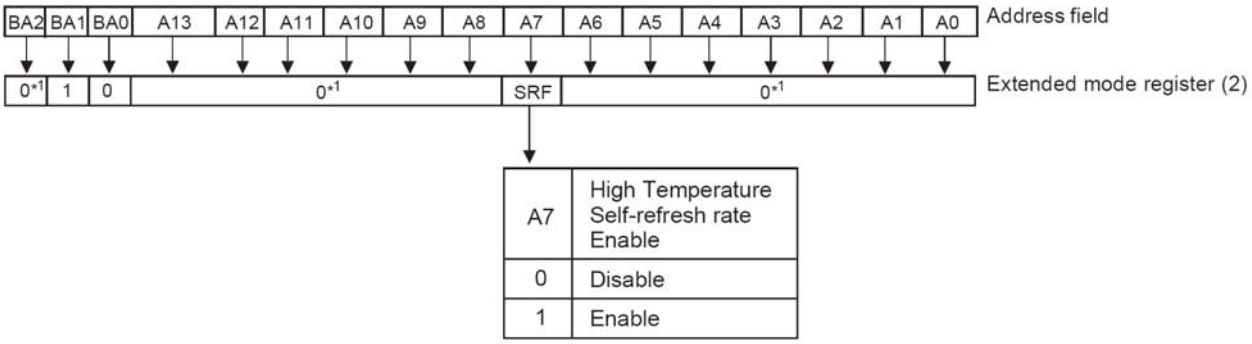
The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is reset, 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Less clock cycles may result in a violation of the tAC or tDQSCK parameters.

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Qoff bit in the EMRS (1) is set to 0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current and external load currents.

Extended Mode Register Set -EMRS (2)

The Extended Mode Registers (2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) is written by asserting low on CS, RAS, CAS, WE, BA0, high on BA1, while controlling the states of address pin A0-A13. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register (2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

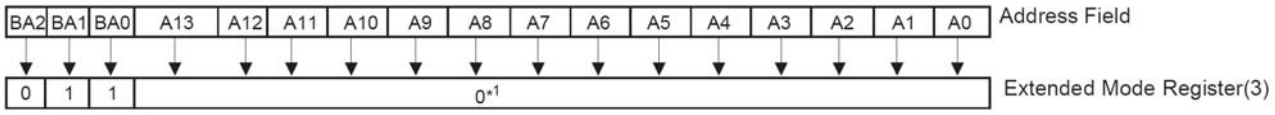


Note:

1. The rest bits in EMRS (2) is reserved for future use and all bits in EMRS (2) except A7, BA0 and BA1 must be programmed to 0 when setting the extended mode register (2) during initialization.

Extended Mode Register Set -EMRS (3)

All bits in EMRS(3) expect BA0 and BA1 are reserved for future use and must be programmed to 0 when setting the mode register during initialization.

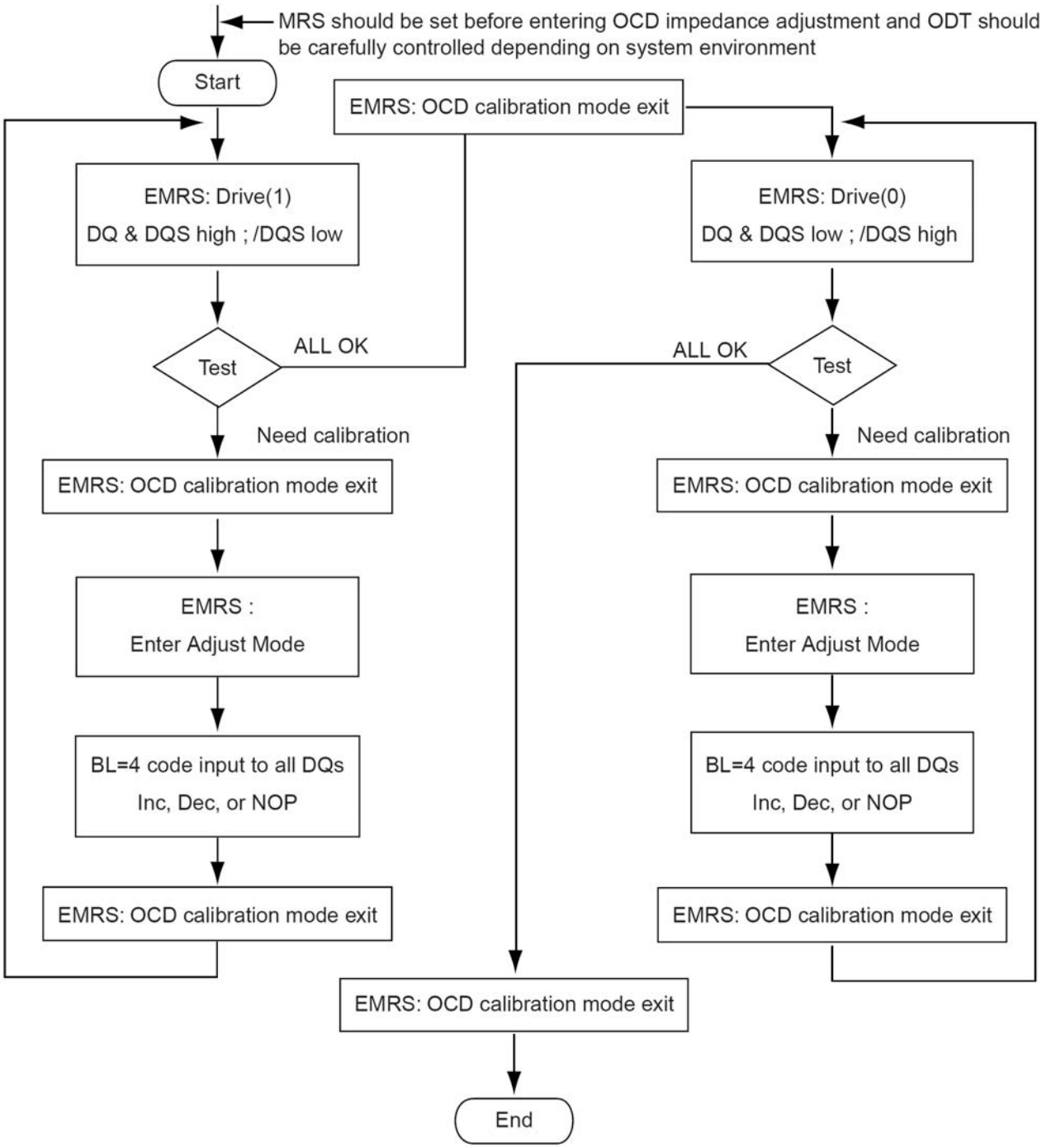


Note:

1. EMRS (3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the OCD Flow Chart is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



Extended Mode Register Set for OCD Impedance Adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM. In Drive (1) mode, all DQ, DQS signals are driven high and all /DQS signals are driven low. In drive (0) mode, all DQ, DQS signals are driven low and all /DQS signals are driven high.

In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics follow approximate nominal V/I curve for 18Ω output drivers, but are not guaranteed. If tighter control is required, which is controlled within 18Ω ± 3Ω driver impedance range, OCD must be used.

OCD applies only to normal full strength output drive setting defined by EMRS (1) and if reduced strength is set, OCD default output driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable.

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive (1) DQ, DQS high and /DQS low
0	1	0	Drive (0) DQ, DQS low and /DQS high
1	0	0	Adjust mode
1	1	1	OCD calibration default

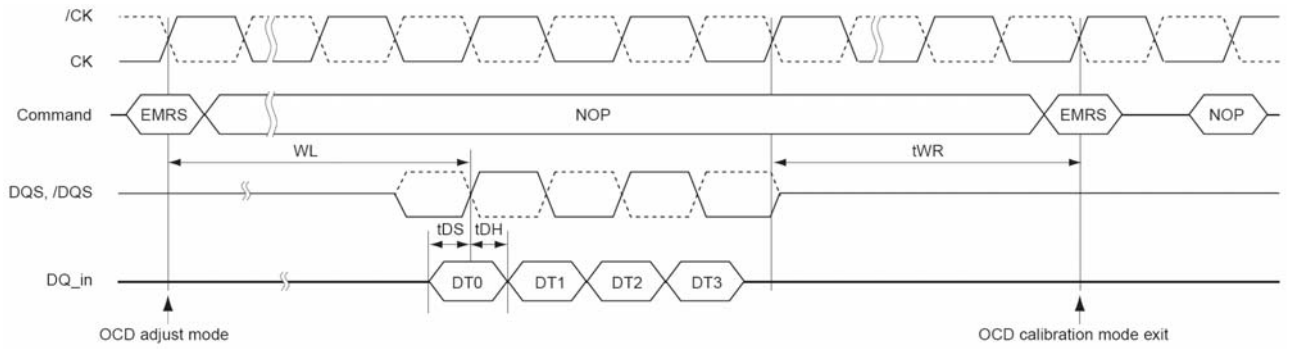
OCD Impedance Adjustment

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in OCD Adjustment Program table. For this operation, burst length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in OCD Adjustment Program table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs and DQS's of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16- step range. When Adjust mode command is issued, AL from previously set value must be applied.

[OCD Adjustment Program]

4bits burst data inputs to all DQs				Operation	
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP	NOP
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other combinations				Reserved	

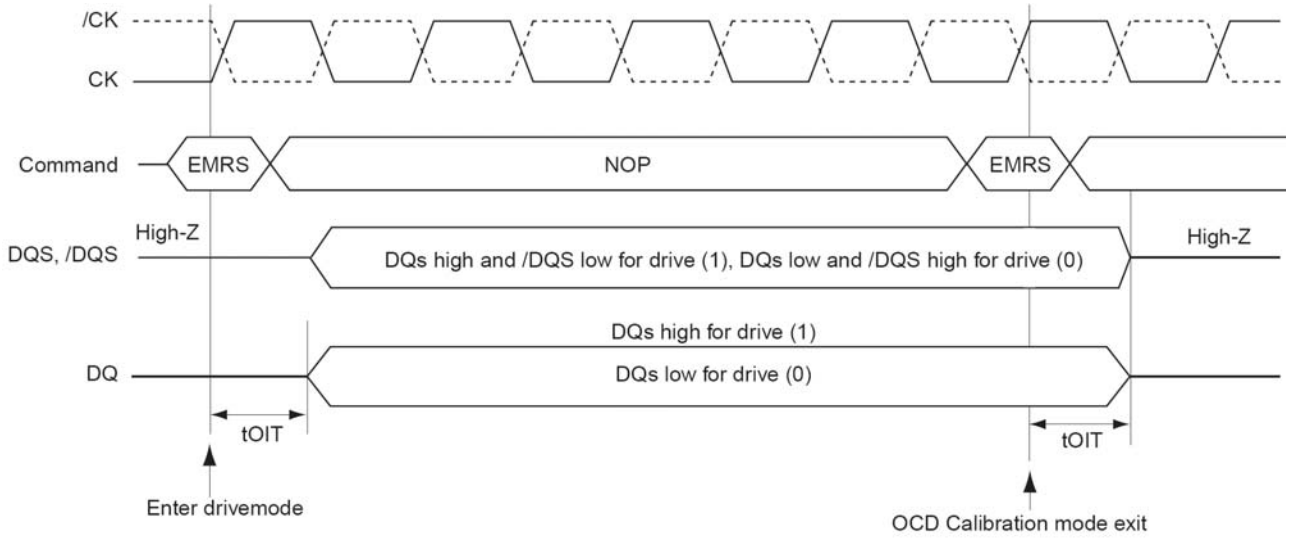
For proper operation of adjust mode, WL = RL − 1 = AL + CL − 1 clocks and tDS/tDH should be met as the Output Impedance Control Register Set Cycle. For input data pattern for adjustment, DT0 to DT3 is a fixed order and not affected by MRS addressing mode (i.e. sequential or interleave).



Output Impedance Control Register Set Cycle

Drive Mode

Drive mode, both drive (1) and drive (0), is used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out tOIT after “Enter drive mode” command and all output drivers are turned-off tOIT after “OCD calibration mode exit” command as the ”Output Impedance Measurement/Verify Cycle”.

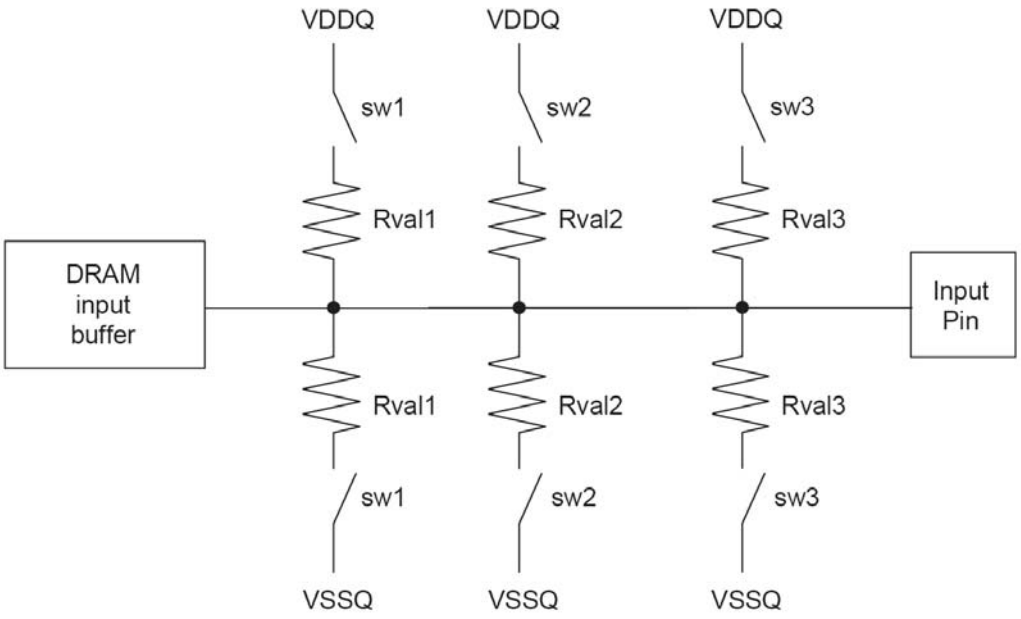


Output Impedance Measurement/Verify Cycle

ODT(On Die Termination)

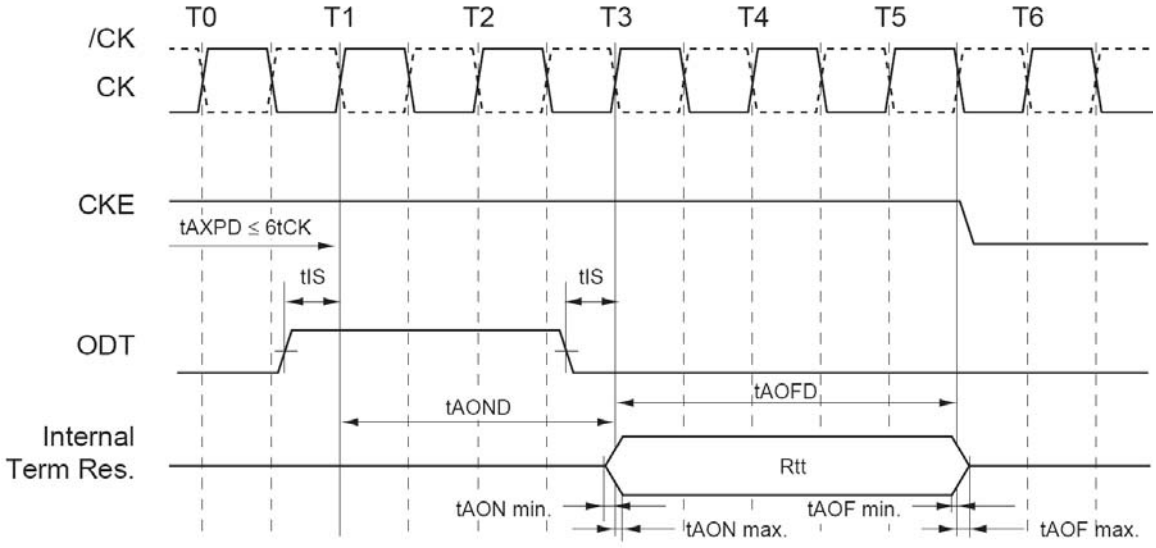
On Die Termination (ODT), is a feature that allows a DRAM to turn on/off termination resistance for each DQ, UDQS, LDQS, /UDQS, /LDQS, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is turned off and not supported in self-refresh mode.



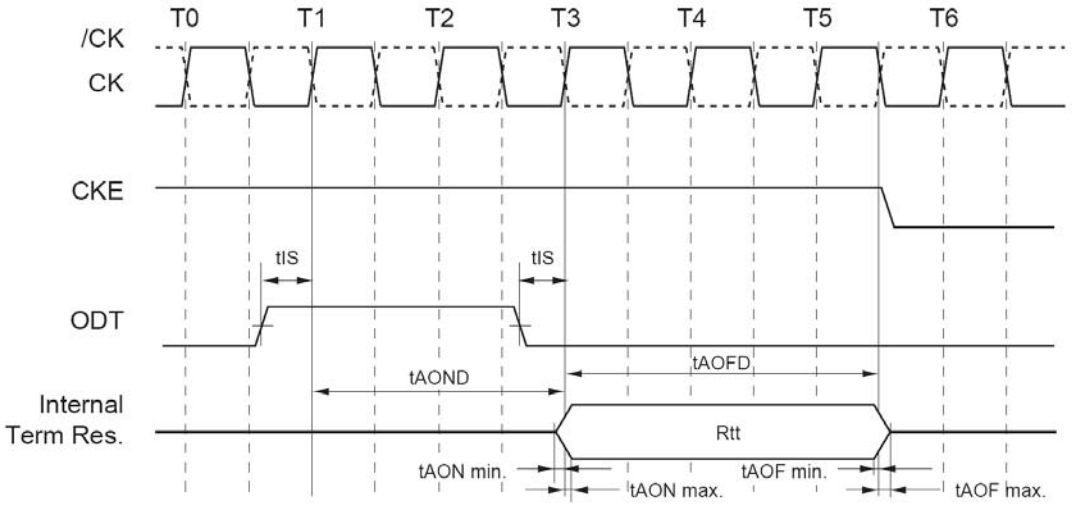
Switch sw1, sw2 or sw3 is enabled by ODT pin.
Selection between sw1, sw2 or sw3 is determined by Rtt (nominal) in EMRS
Termination included on all DQs, UDM, LDM, UDQS, LDQS, /UDQS and /LDQS pins.
Target Rtt (Ω) = (Rval1) / 2, (Rval2) / 2 or (Rval3) / 2

Functional Representation of ODT

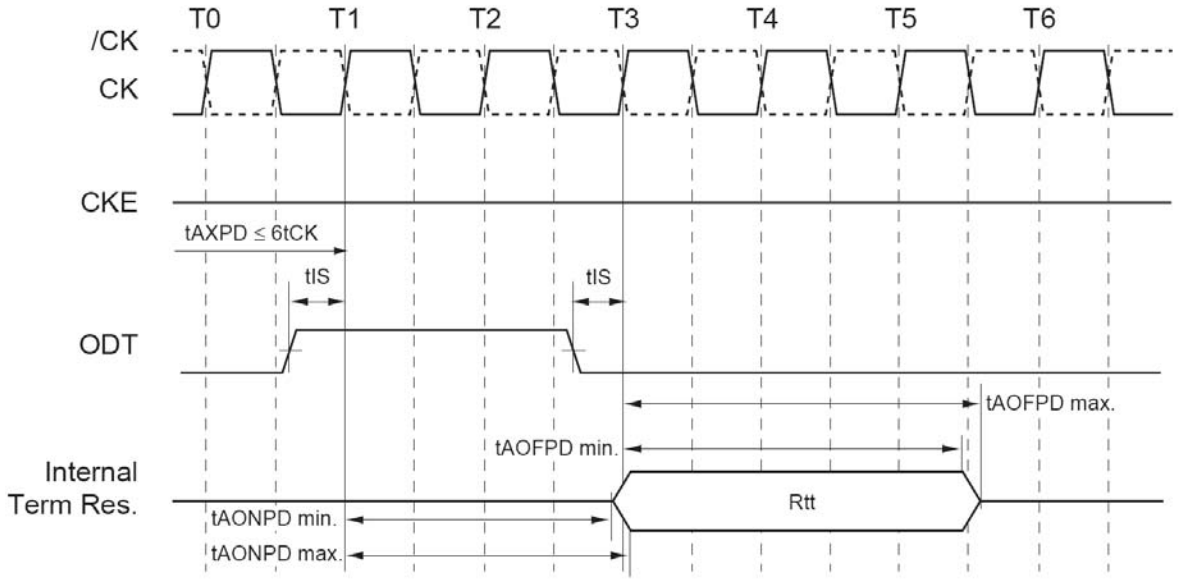


Note: tAOFD must be met before issuing EMRS command. ODT must remain low for the entire duration of tMOD window.

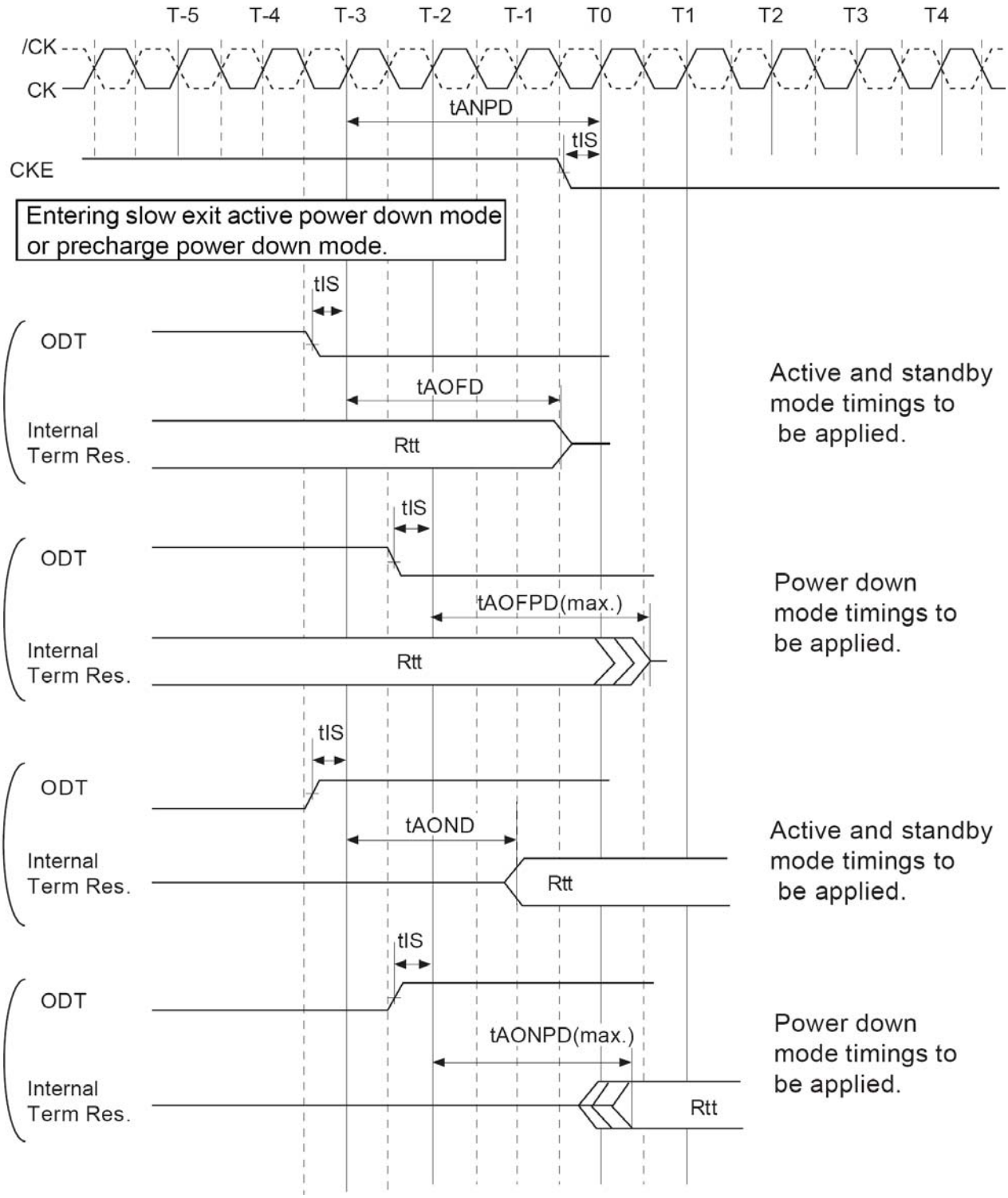
ODT update Delay Timing



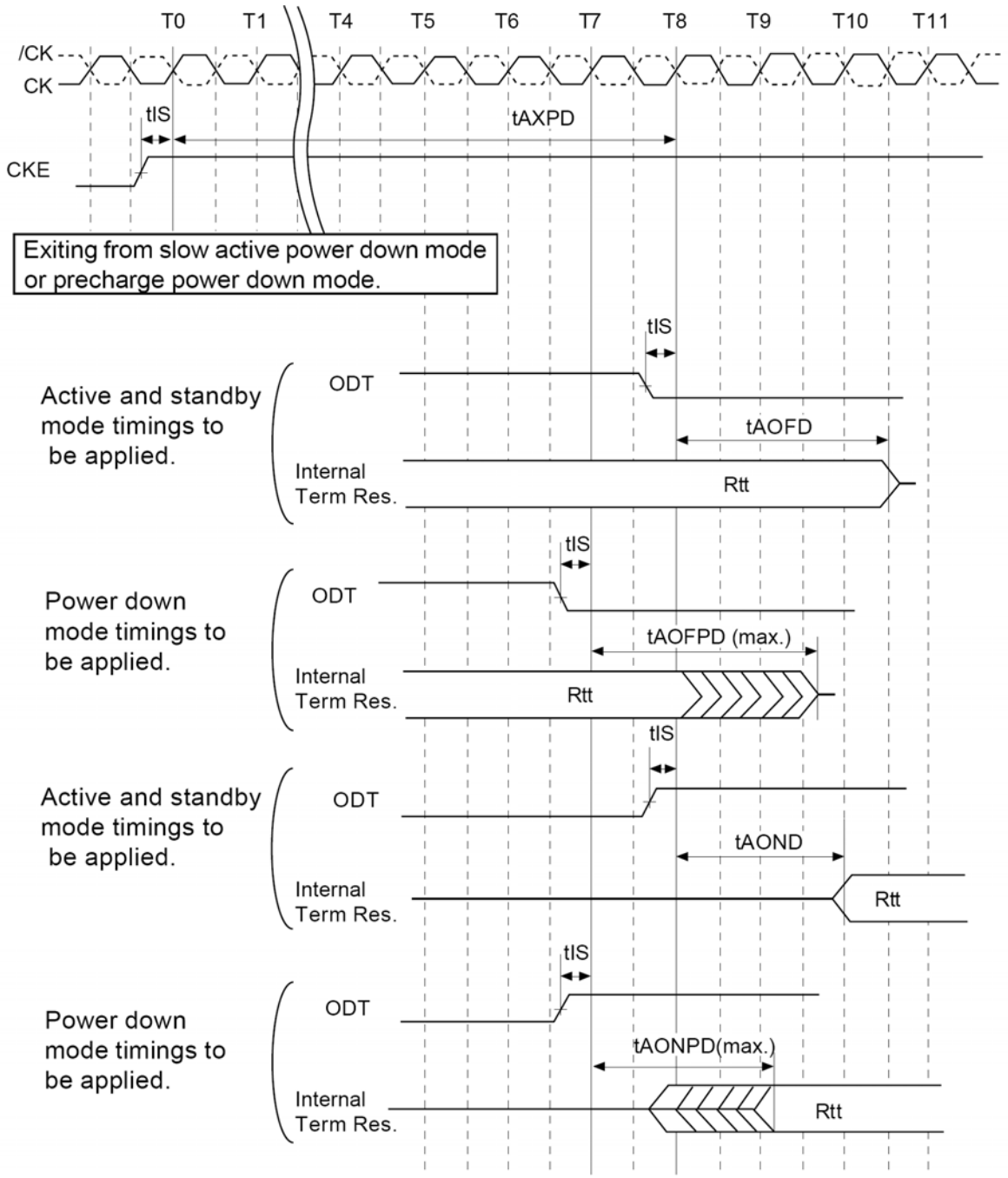
ODT Timing for Active and Standby Mode



ODT Timing for Power down Mode



ODT Timing Mode Switch at Entering Power Down Mode



ODT Timing Mode Switch at Exiting Power Down Mode

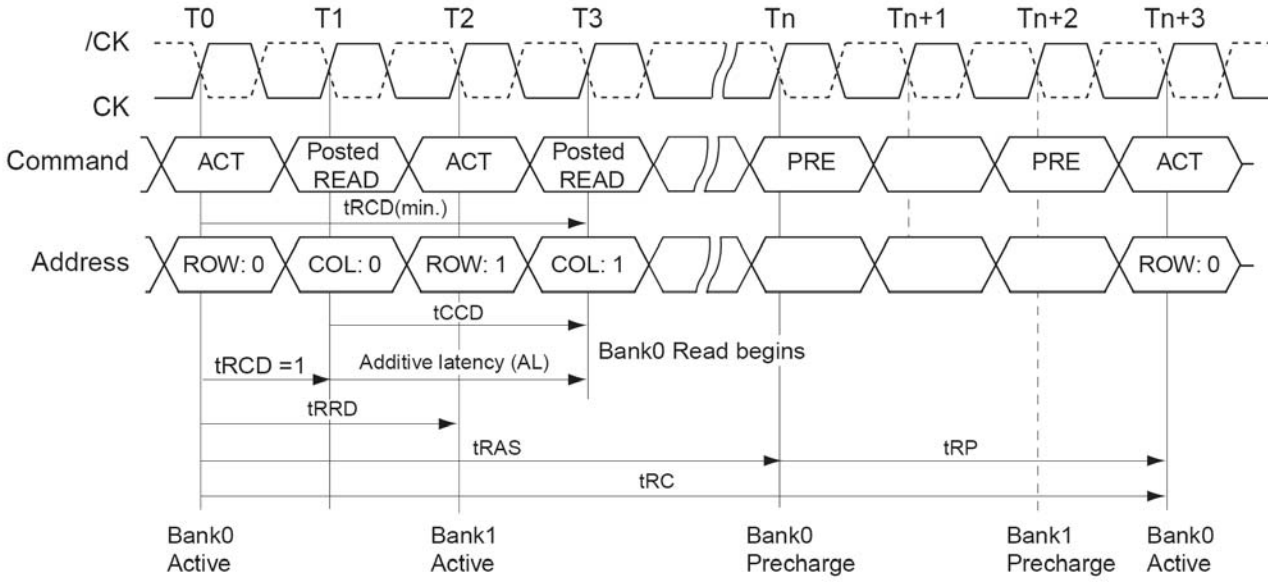
Bank Activate Command

The Bank Activate command is issued by holding /CAS and /WE high plus /CS and /RAS low at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row addresses A0 through A13 are used to determine which row to activate in the selected bank for and x8 organized components. For x16 components row addresses A0 through A12 have to be applied. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If an R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3, 4, 5, and 6 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (tRC). The minimum time interval between Bank Active commands, to other bank, is the Bank A to Bank B delay time (tRRD).

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential ACTcommands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are list as follow:

* 8 bank device sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling tFAW window. Conveting to clocks is done by dividing tFAW by tCK and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

*8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will equal to tRP+tCK, where tRP is the value for a single bank precharge.



Bank Activate Command Cycle (tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2)

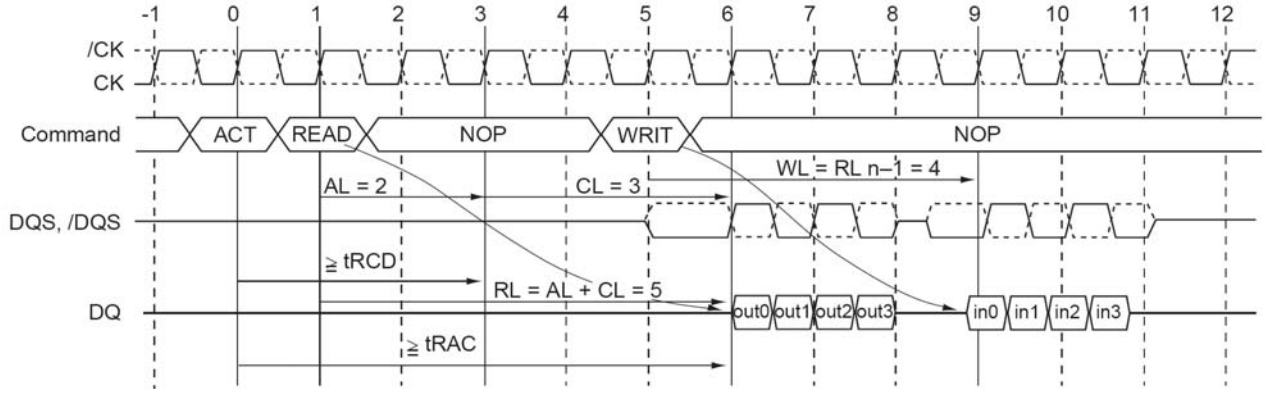
Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting /RAS high, /CS and /CAS low at the clock" s rising edge. /WE must also be defined at this time to determine whether the access cycle is a read operation (/WE high) or a write operation (/WE low). The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is restricted to specific segments of the page length.

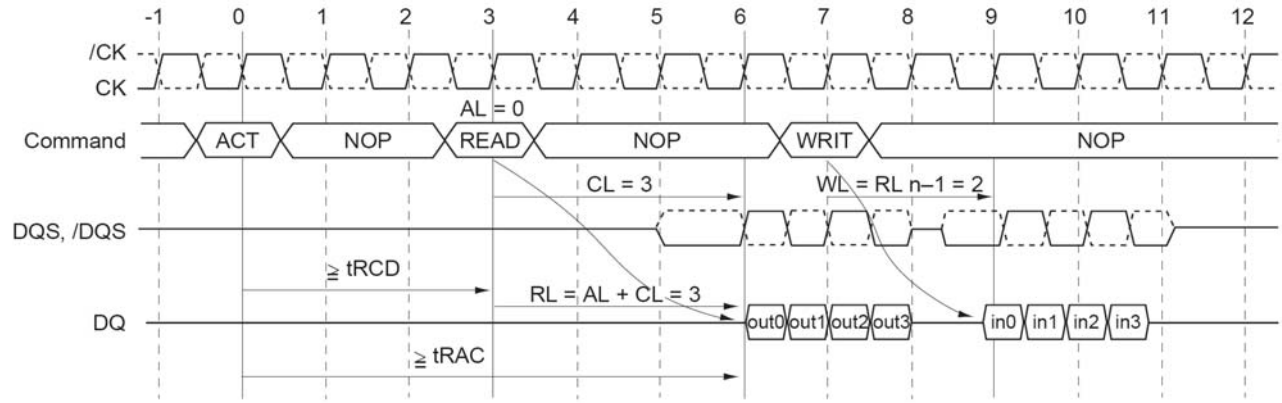
A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL=8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively, and the minimum /CAS to /CAS delay (tCCD) is minimum 2 clocks for read or write cycles.

Posted /CAS

Posted /CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the /RAS bank activate command (or any time during the /RAS to /CAS delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the /CAS latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL greater than 0 must be written into the EMRS (1). The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus /CAS latency (RL=AL+CL). If a user chooses to issue a Read command after the tRCDmin period, the Read Latency is also defined as RL = AL + CL.



Read Followed by a Write to the Same Bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4]



Read Followed by a Write to the Same Bank

[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2]

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the “Burst Interruption “section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

Bust Length and Sequence

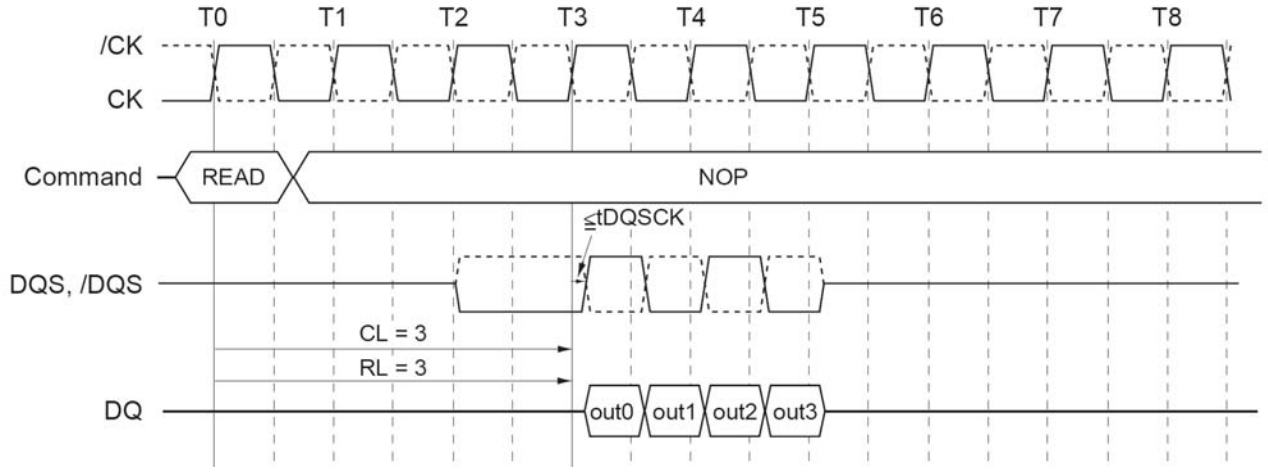
Burst length	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4	000	0, 1, 2, 3	0, 1, 2, 3
	001	1, 2, 3, 0	1, 0, 3, 2
	010	2, 3, 0, 1	2, 3, 0, 1
	011	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Note:

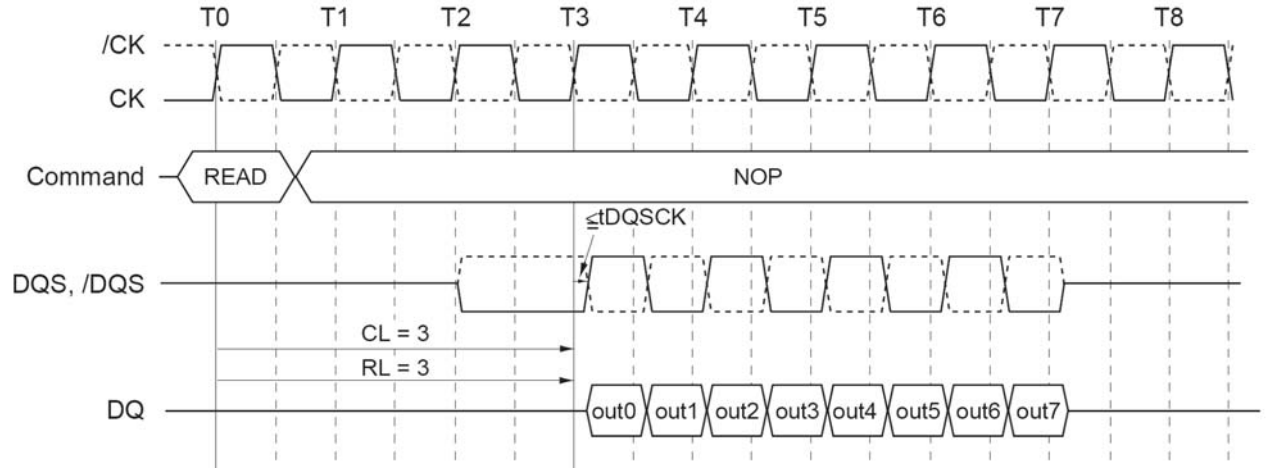
1. Page length is a function of I/O organization
   64Mb X 16 organization (CA0-CA9); Page Size = 2K Byte; Page Length = 1024
   128Mb X 8 organization (CA0-CA9); Page Size = 1K Byte; Page Length = 1024
   256Mb x 4 organization (CA0-CA9, CA11); Page Size = 1K Byte; Page Length = 2048
2. Order of burst access for sequential addressing is "nibble-based" and therefore different from SDR or DDR components.

Burst Read Command

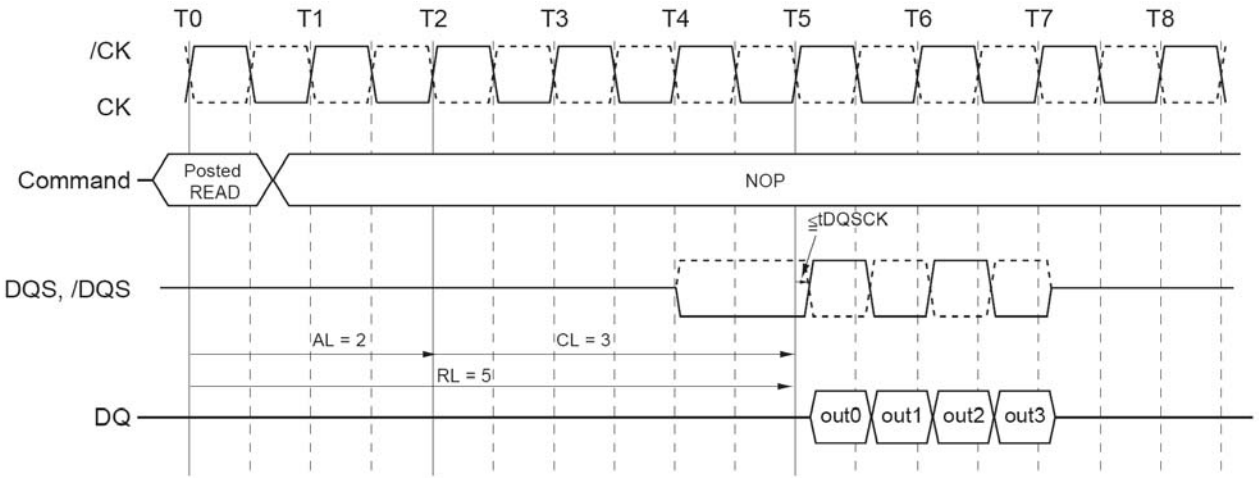
The Burst Read command is initiated by having /CS and /CAS low while holding /RAS and /WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus /CAS latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS (1)).



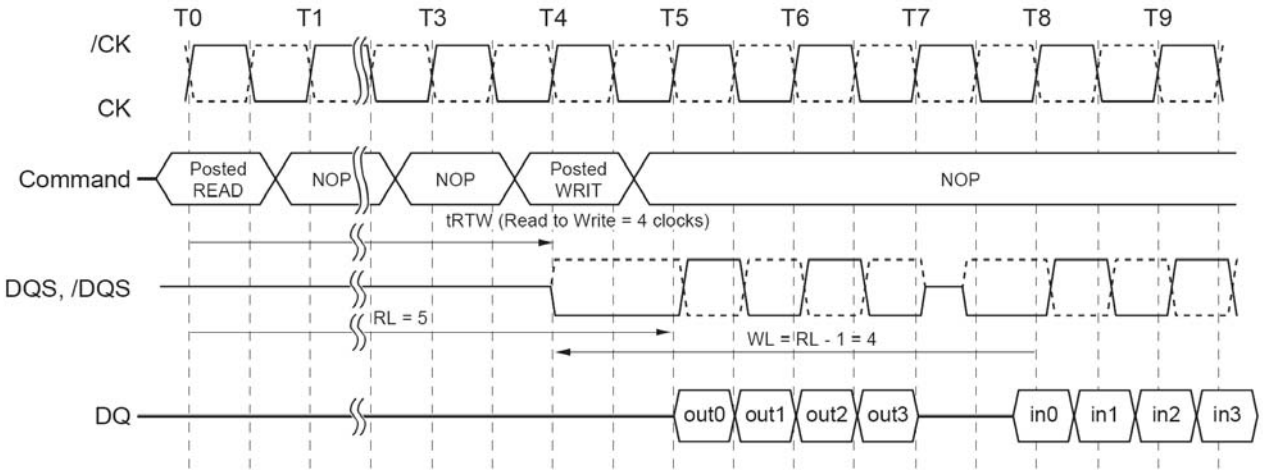
Burst Read Operation (RL = 3, BL = 4 (AL = 0 and CL = 3))



Burst Read Operation (RL = 3, BL = 8 (AL = 0 and CL = 3))

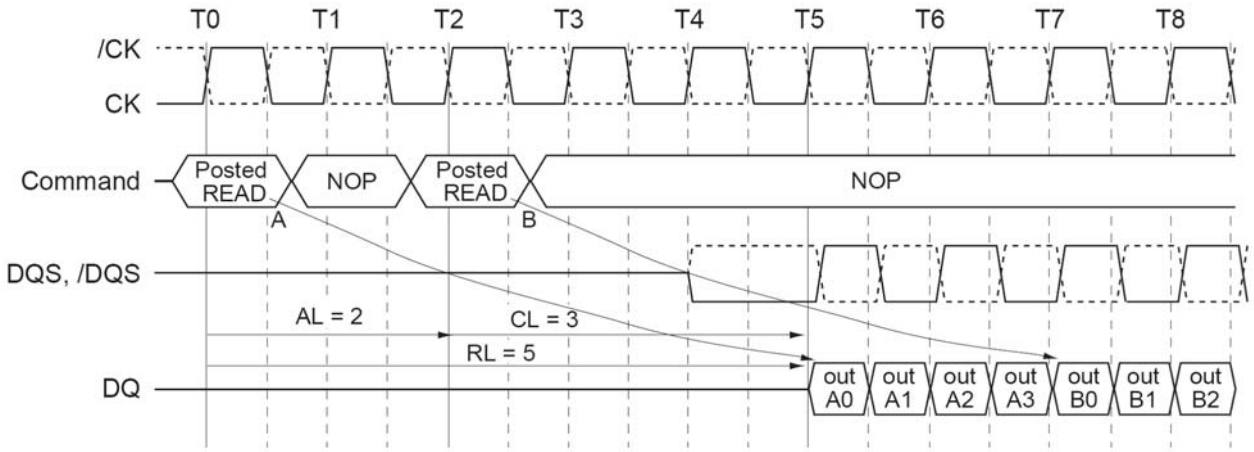


Burst Read Operation (RL = 5, BL = 4 (AL = 2, CL = 3))



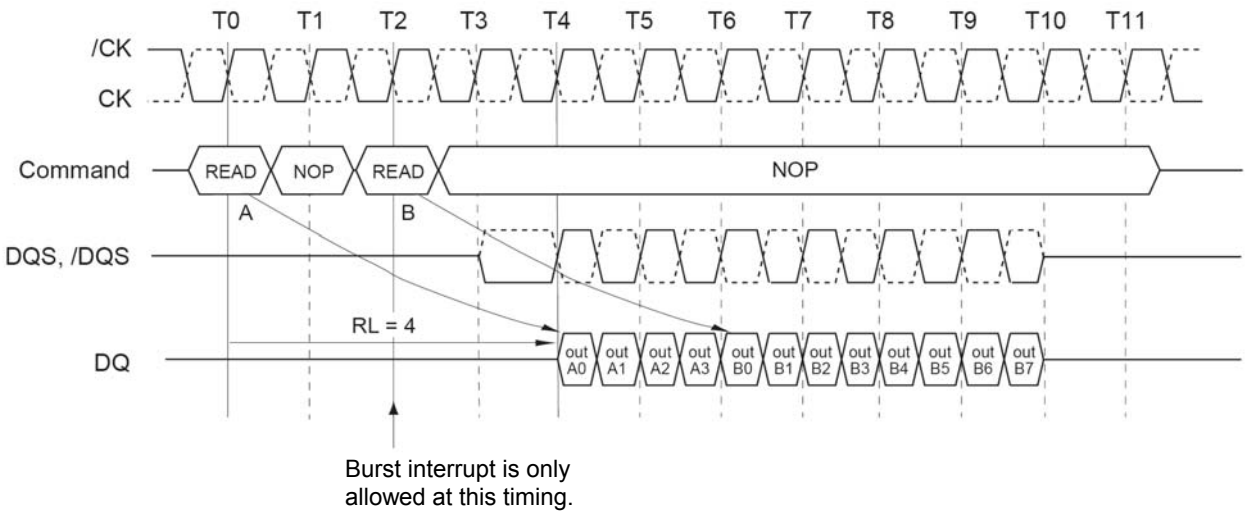
Burst Read Followed by Burst Write (RL = 5, WL = RL-1 = 4, BL = 4)

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turnaround-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.



Seamless Burst Read Operation (RL = 5, AL = 2, and CL = 3)

Enabling a read command at every other clock supports the seamless burst read operation. This operation is allowed regardless of same or different banks as long as the banks are activated.



Burst Read Interrupt by Read

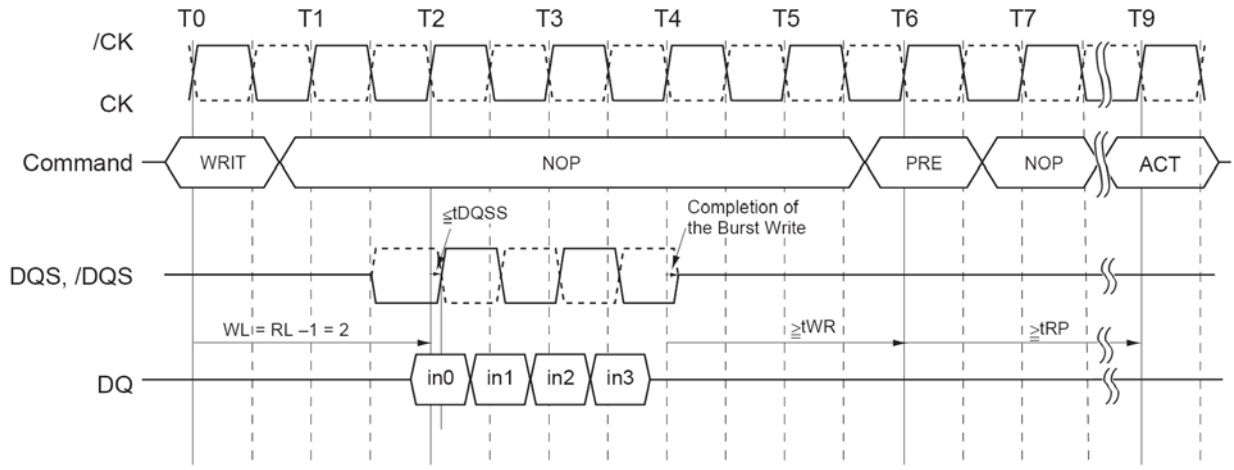
Notes :

1. Read burst interrupt function is only allowed on burst of 8. burst interrupt of 4 is prohibited.
2. Read burst of 8 can only be interrupted by another read command. Read burst interruption by write command or precharge command is prohibited.
3. Read burst interrupt must occur exactly two clocks after previous read command. any other read burst interrupt timings are prohibited.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with auto precharge enabled is not allowed to interrupt.
6. Read burst interruption is allowed by another read with auto precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum read to precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

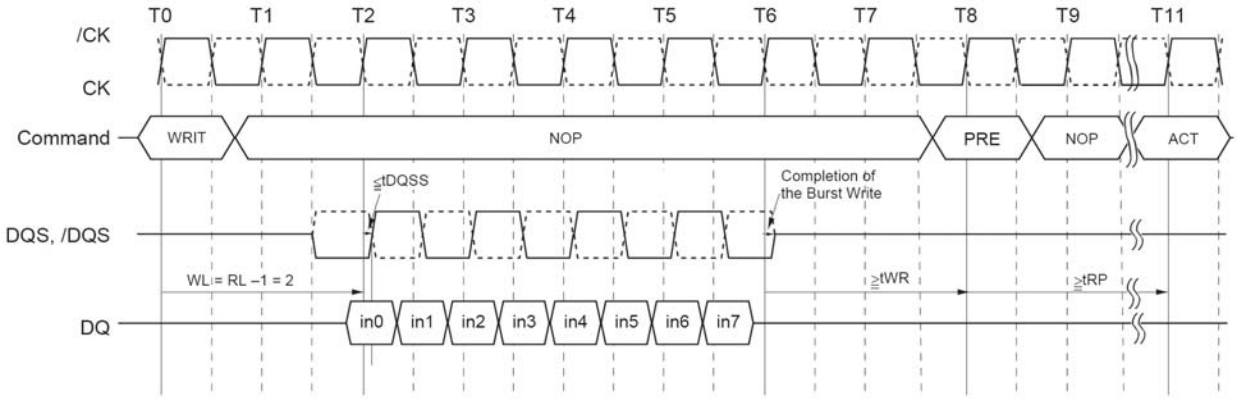
Burst Write Command

The Burst Write command is initiated by having CS, CAS and WE low while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) has to be driven low (preamble) a time tWPRE prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named “write recovery time” (WR).

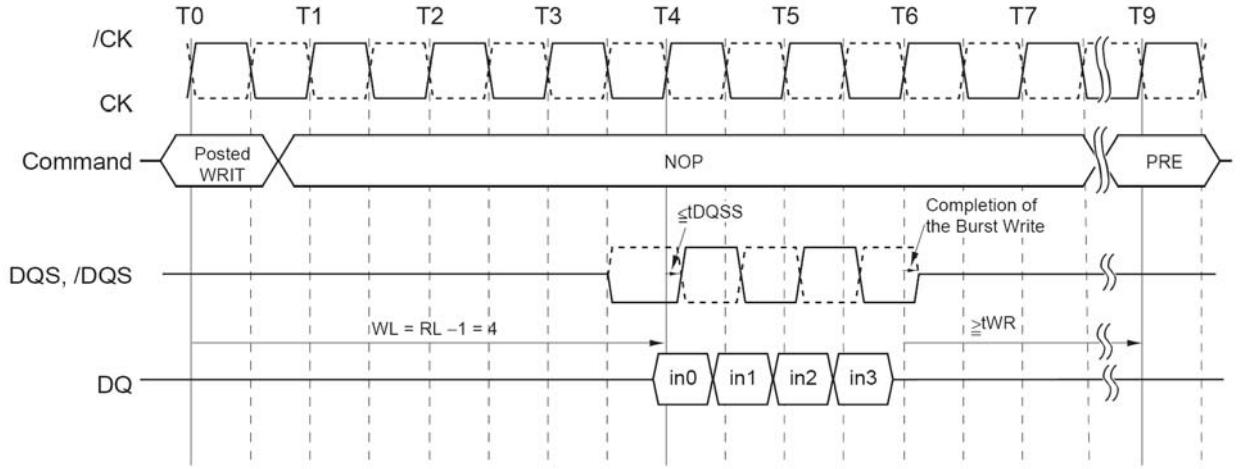
DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing measured is mode dependent.



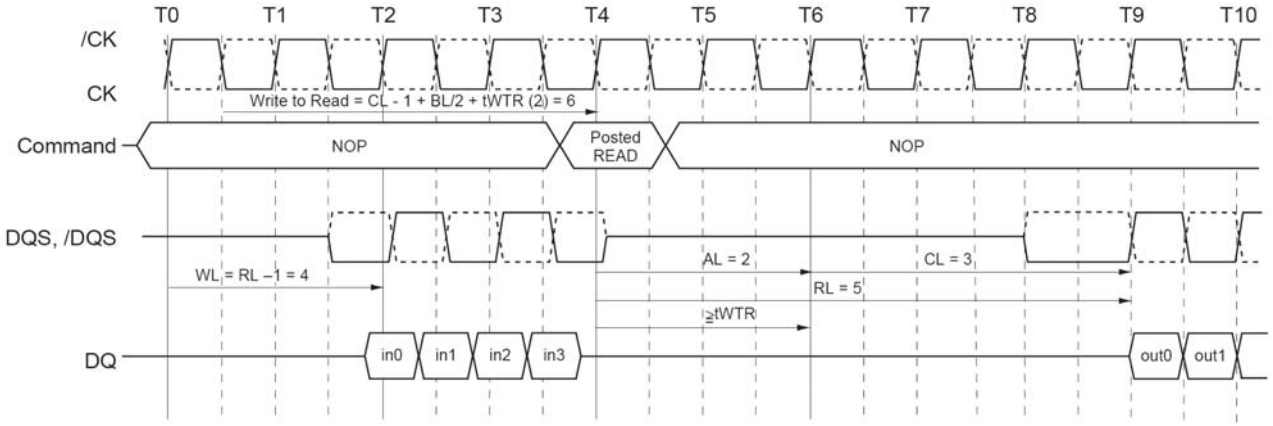
Burst Write Operation (RL = 3, WL = 2, BL = 4 tWR = 2 (AL=0, CL=3))



Burst Write Operation (RL = 3, WL = 2, BL = 8 (AL=0, CL=3))

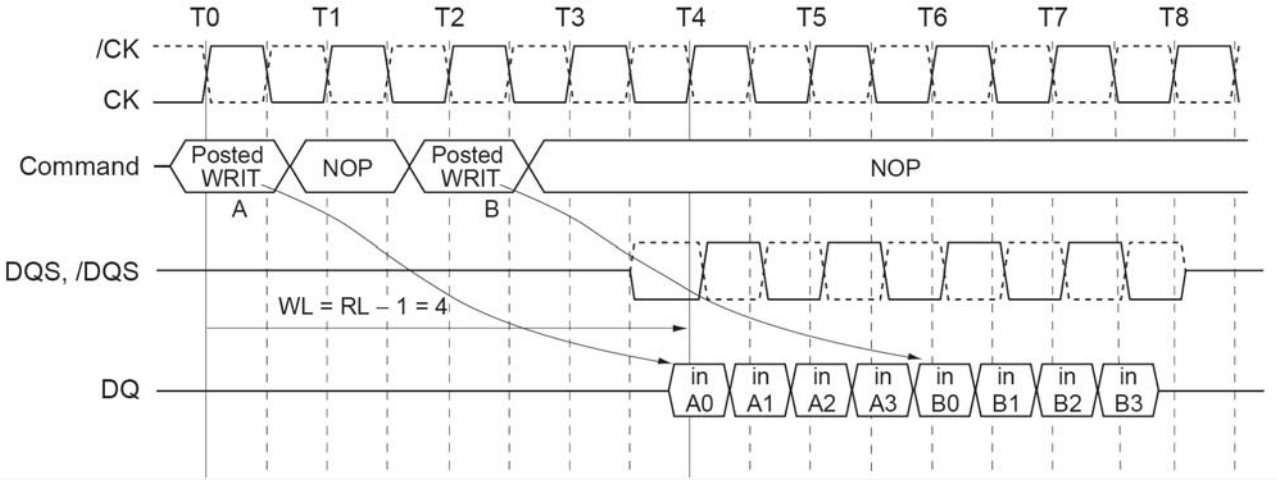


Burst Write Operation (RL = 5, WL = 4, BL = 4 tWR = 3 (AL=2, CL=3))



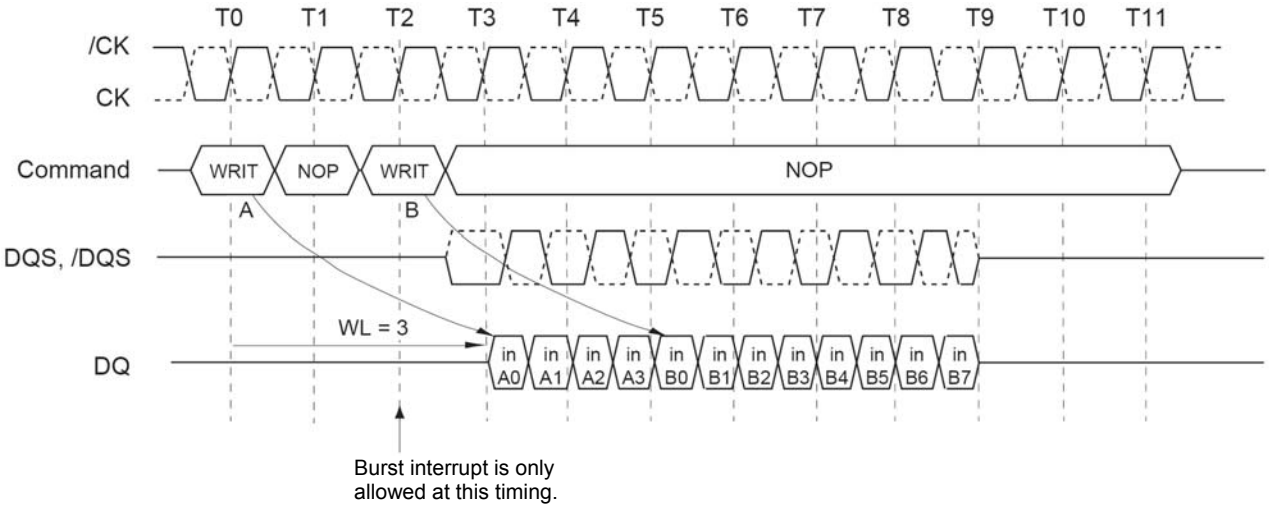
Burst Write Followed by Burst Read (RL = 5, BL = 4, WL = 4, tWTR = 2 (AL=2, CL=3))

The minimum number of clock from the burst write command to the burst read command is CL - 1 + BL/2 + a write to-read-turn-around-time (tWTR). This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array.



Seamless Burst Write Operation (RL = 5, WL = 4, BL = 4)

Enabling a write command every other clock supports the seamless burst write operation. This operation is allowed regardless of same or different banks as long as the banks are activated.



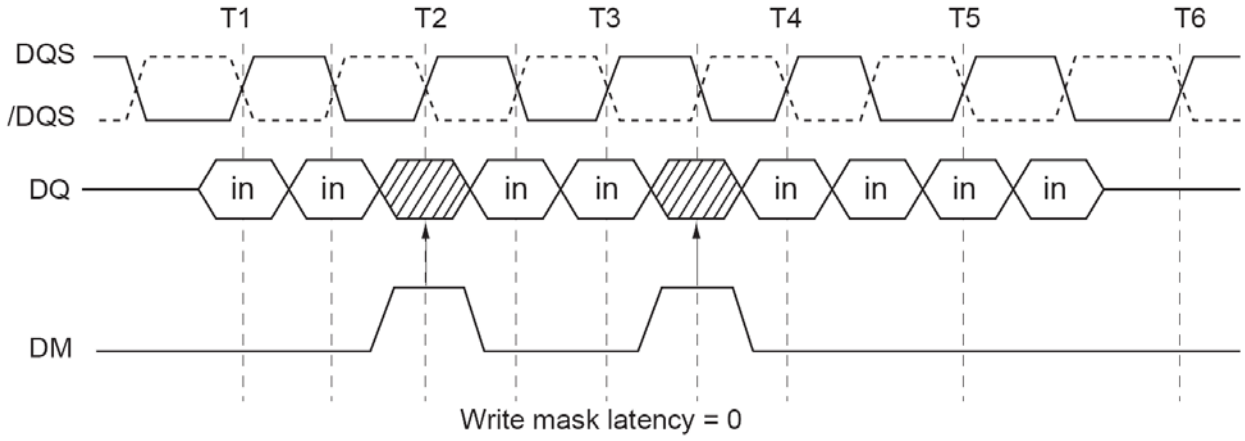
Write Interrupt by Write (WL = 3, BL = 8)

Notes :

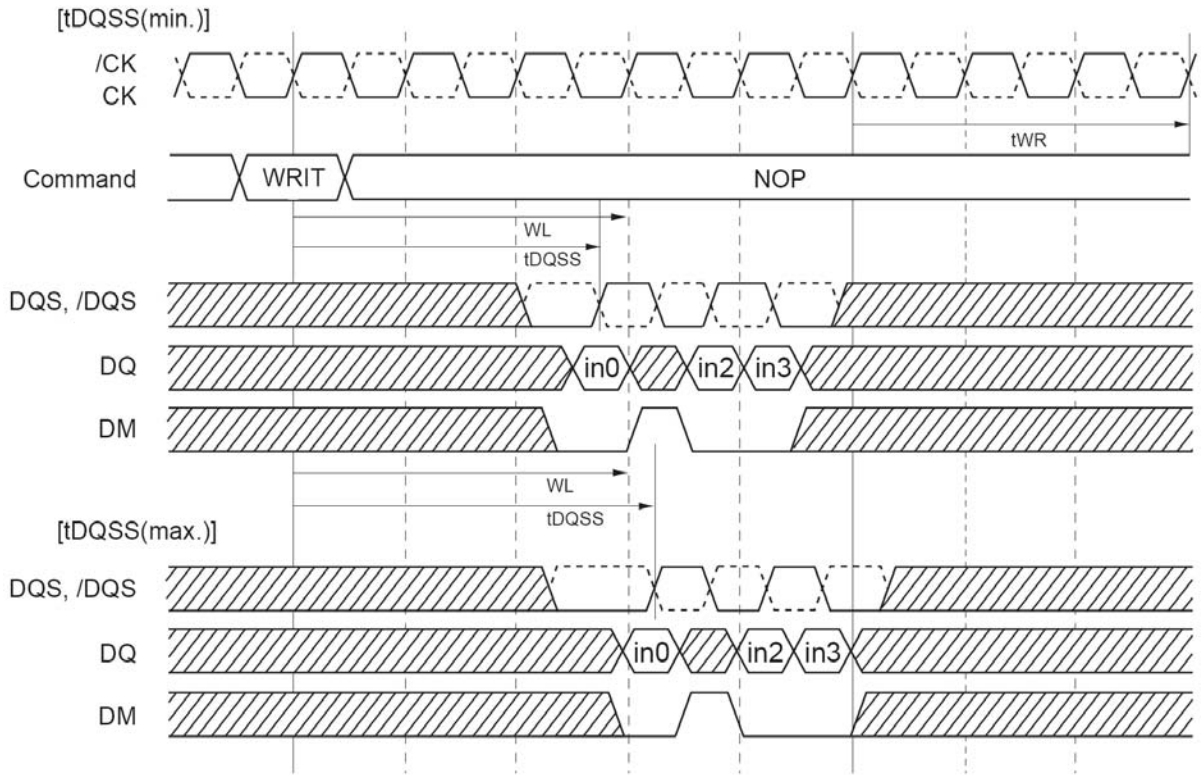
1. Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Write burst of 8 can only be interrupted by another write command. Write burst interruption by read command or precharge command is prohibited.
3. Write burst interrupt must occur exactly two clocks after previous write command. Any other write burst interrupt timings are prohibited.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with auto precharge enabled is not allowed to interrupt.
6. Write burst interruption is allowed by another write with auto precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum write to precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

Write Data Mask

One write data mask input (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However, DM of x8 bit organization can be used as RDQS during read cycles by EMRS (1) setting.



Data Mask Timing



Data Mask Function, WL = 3, AL = 0 shown

Burst Interruption

Interruption of a read or write burst is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

1. A Read Burst of 8 can only be interrupted by another Read command. Read burst interruption by a Write or Precharge Command is prohibited.

2. A Write Burst of 8 can only be interrupted by another Write command. Write burst interruption by a Read or Precharge Command is prohibited.

3. Read burst interrupt occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.

4. Write burst interrupt occur exactly two clocks after the previous Write command. Any other Read burst interrupt timings are prohibited.

5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.

6. Read or Write burst with Auto-Precharge enabled is not allowed to be interrupted.

7. Read burst interruption is allowed by a Read with Auto-Precharge command.

8. Write burst interruption is allowed by a Write with Auto-Precharge command.

9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt). Minimum Write to Precharge timing is WL + BL/ 2 + tWR, where tWR starts with the rising clock after the un-interrupted burst end and not form the end of the actual burst end.

Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The Pre-charge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0, BA1, and BA2 are used to define which bank to precharge when the command is issued.

[Bank Selection for Precharge by Address Bits

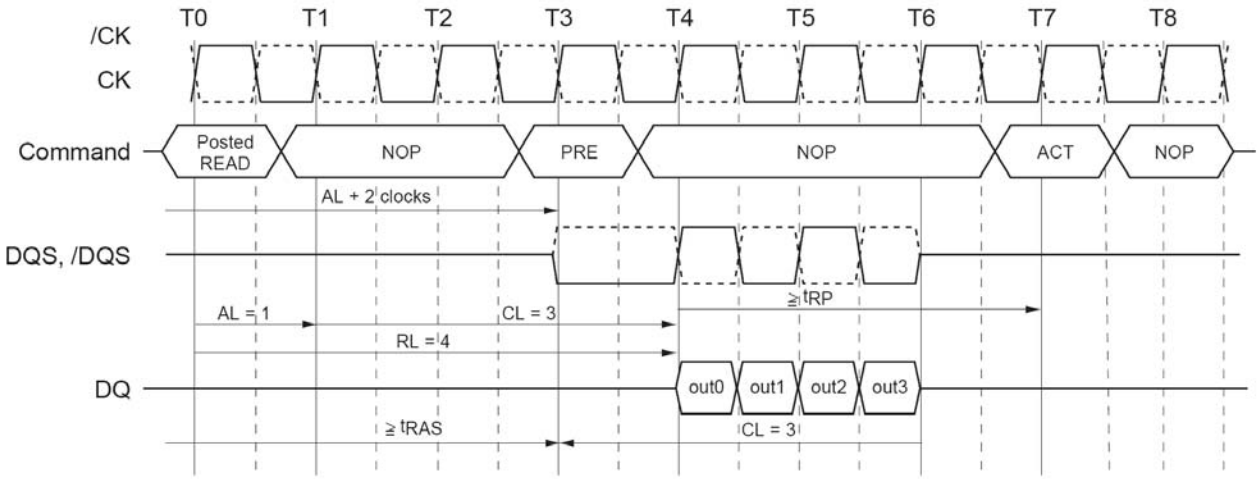
A10	BA0	BA1	BA2	Precharged Bank(s)
L	L	L	L	Bank 0 only
L	H	L	L	Bank 1 only
L	L	H	L	Bank 2 only
L	H	H	L	Bank 3 only
L	L	L	H	Bank 4 only
L	H	L	H	Bank 5 only
L	L	H	H	Bank 6 only
L	H	H	H	Bank 7 only
H	x	x	x	All banks 0 to 7

Remark: H: VIH, L: VIL, ·: VIH or VIL

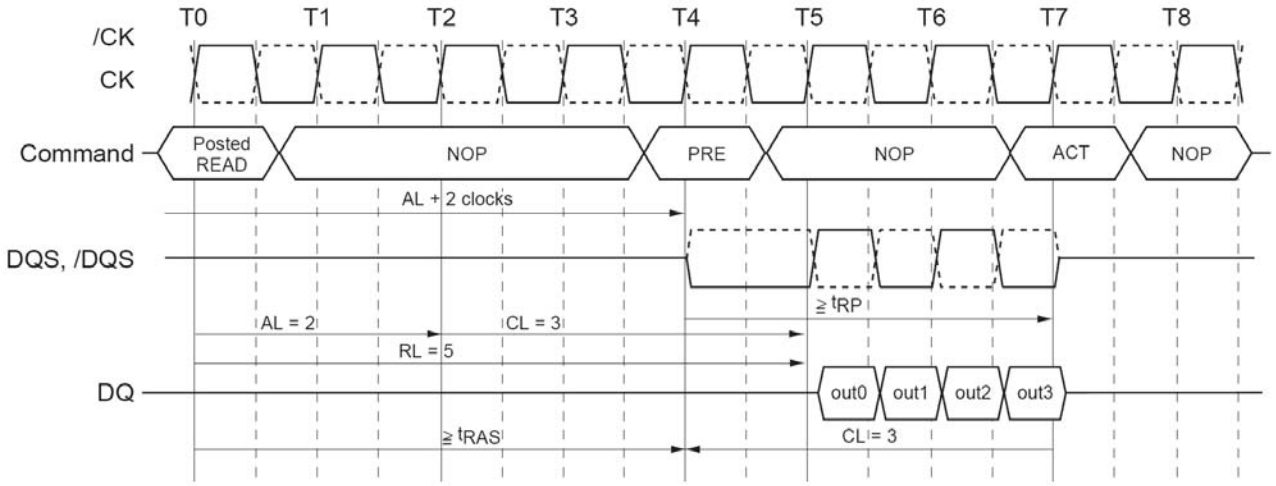
Burst Read Operation Followed by Precharge

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 + max (RTP, 2) - 2 clocks.
For the earliest possible precharge, the Precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2 clocks" after a Read Command, as long as the minimum tRAS timing is satisfied.

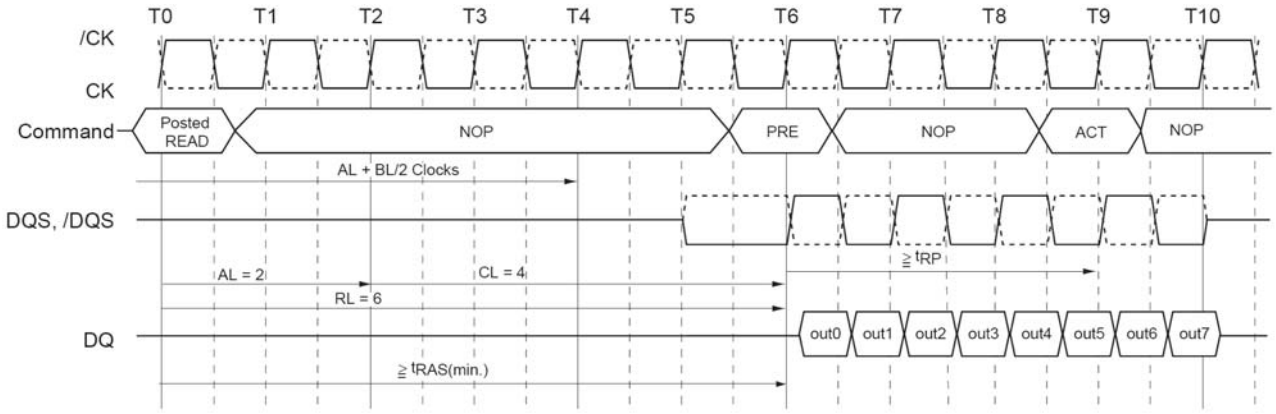
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is call tRTP (Read to Precharge). For BL=4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL=8 this is the time from AL + 2 clocks after the Read to the Precharge command.



Burst Read Operation Followed by Precharge (RL = 4, BL = 4 (AL=1, CL=3))



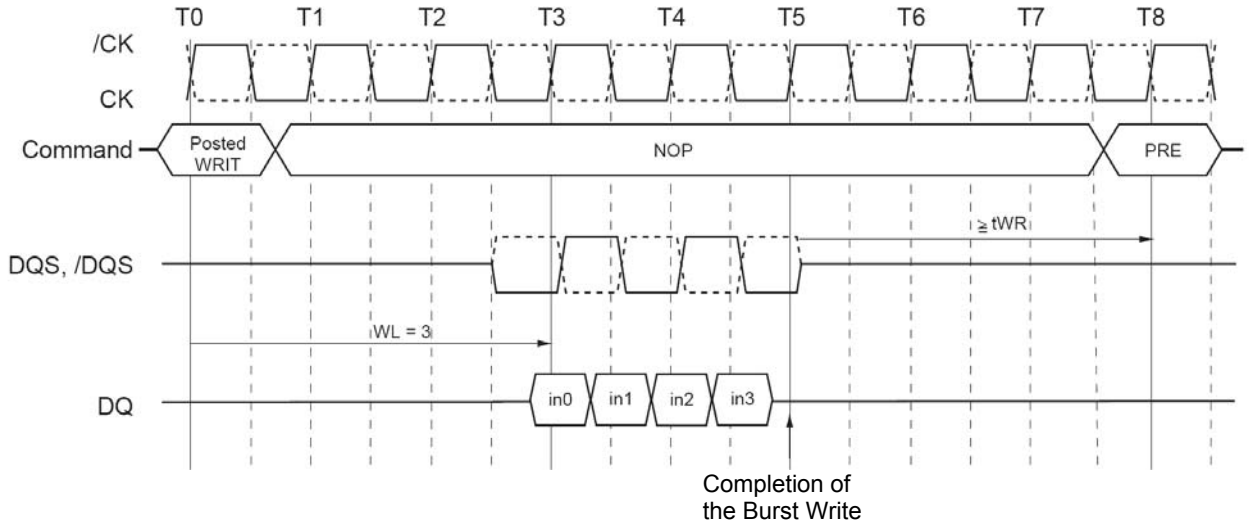
Burst Read Operation Followed by Precharge (RL = 5, BL = 4 (AL=2, CL=3))



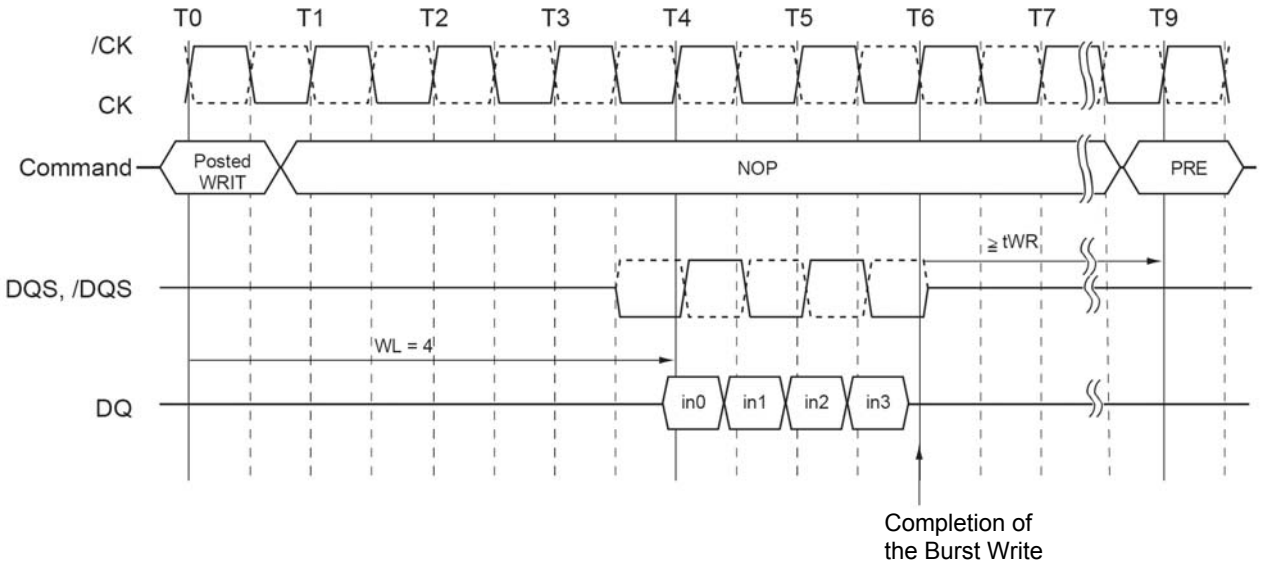
Burst Read Operation Followed by Precharge (RL = 6 (AL=2, CL=4, BL=8))

Burst Write followed by Precharge

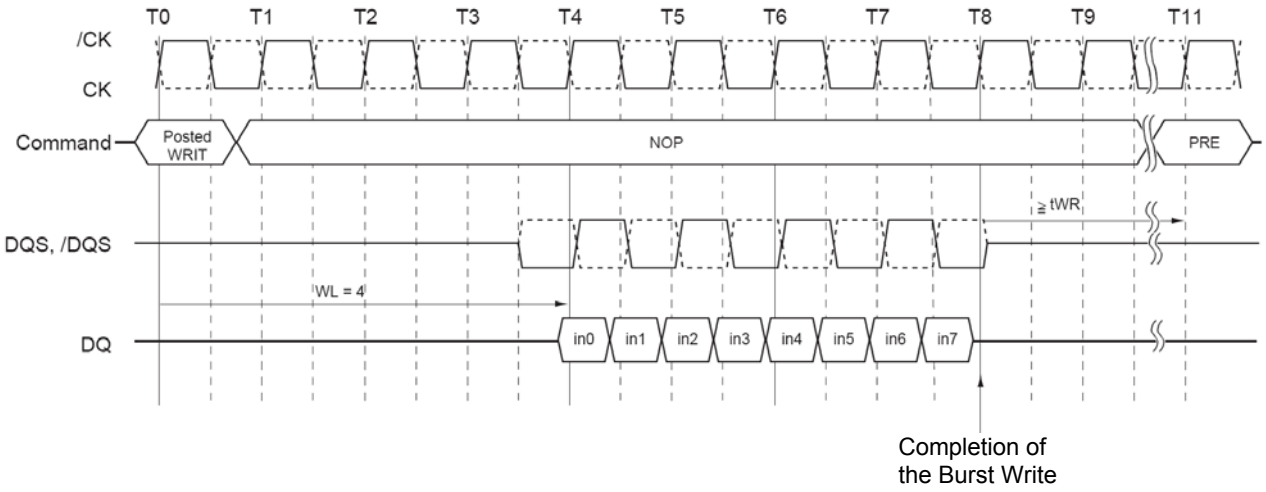
Minimum Write to Precharge command spacing to the same bank = WL + BL/2 + tWR. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the tWR delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. tWR is an analog timing parameter (see the AC table in this datasheet) and is not the programmed value for tWR in the MRS.



Burst Write Followed by Precharge (WL = (RL-1) =3)



Burst Write Followed by Precharge (WL = (RL-1) = 4)



Burst Write Followed by Precharge (WL = (RL-1) = 4,BL= 8)

Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Pre-charge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the Auto-Precharge function is enabled. During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge internally on the rising edge which is /CAS Latency (CL) clock cycles before the end of the read burst. Auto-Precharge is also implemented for Write Commands. The precharge operation engaged by the Auto-Precharge command will not begin until the last data of the write burst sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon /CAS Latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed so that the Auto-Precharge command may be issued with any read or write command.

Burst Read with Auto-Precharge

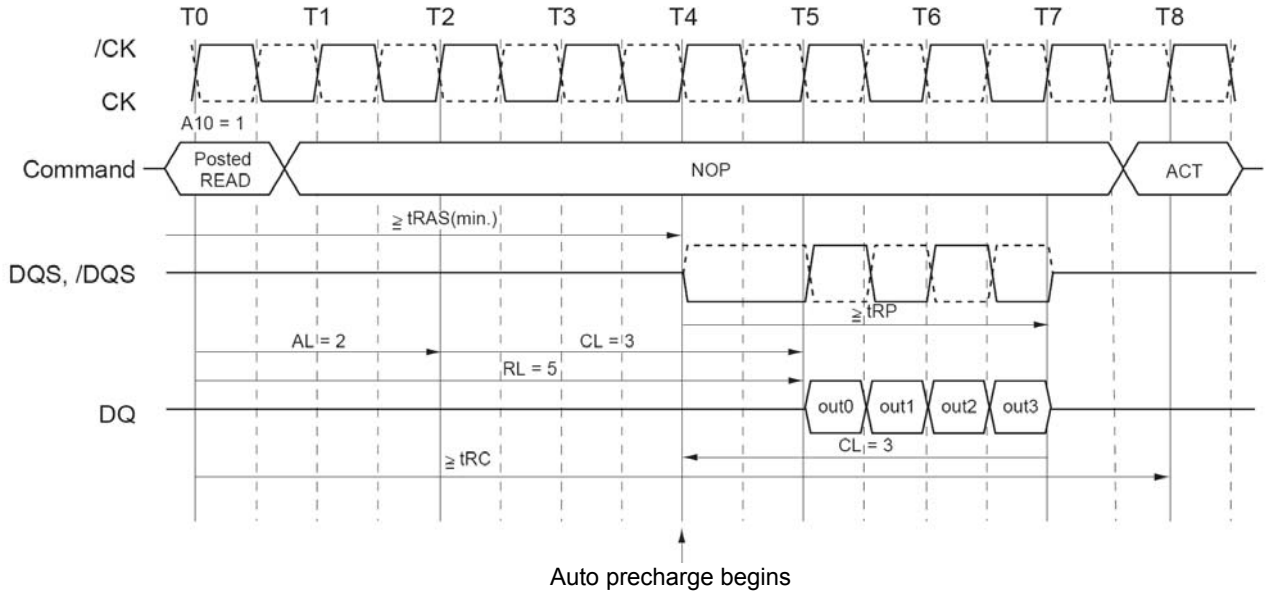
If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if tRAS(min) and tRTP are satisfied. If tRAS(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until tRAS(min) is satisfied. If tRTP(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until tRTP(min) is satisfied.

In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + tRTP + tRP. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + tRTP + tRP. Note that both parameters tRTP and tRP have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

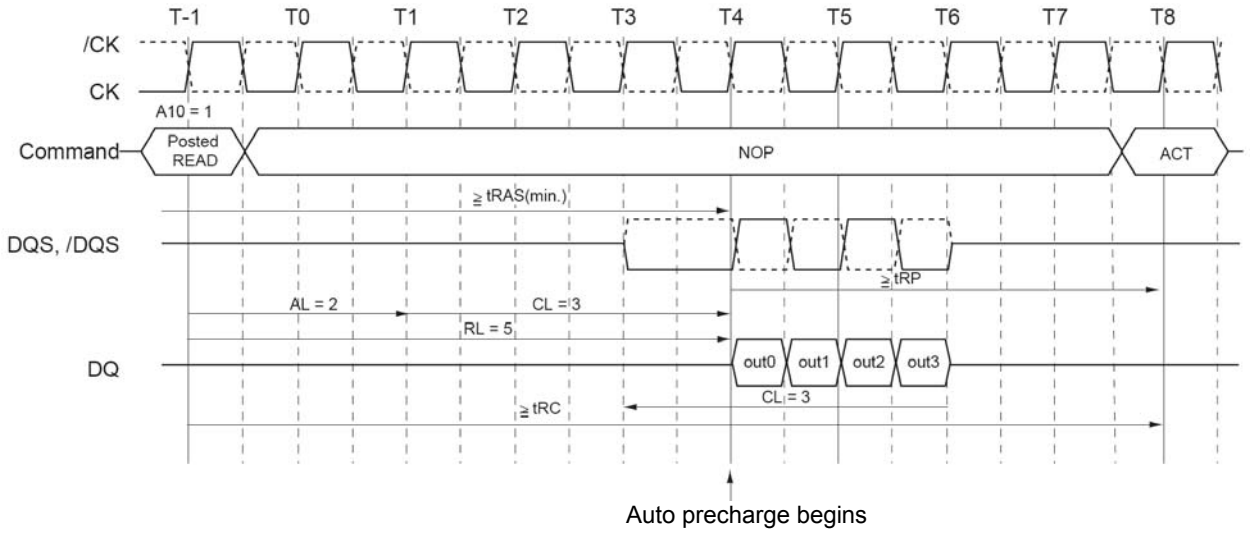
(1) The /RAS precharge time (tRP) has been satisfied from the clock at which the Auto-Precharge begins.

(2) The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

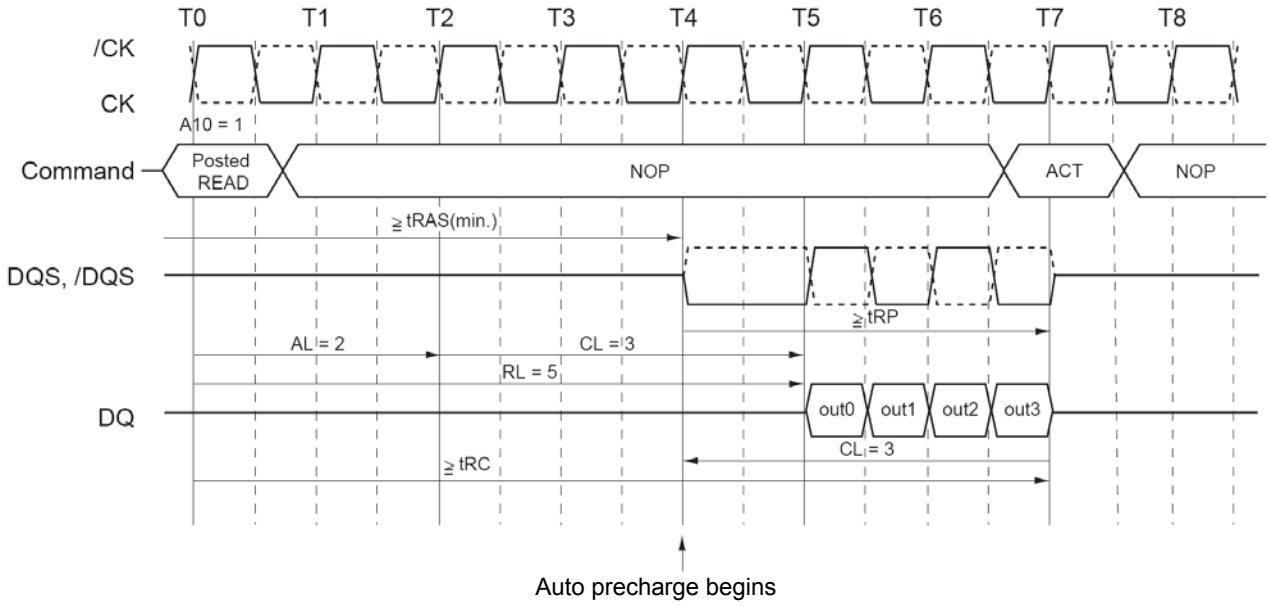


Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRC limit)

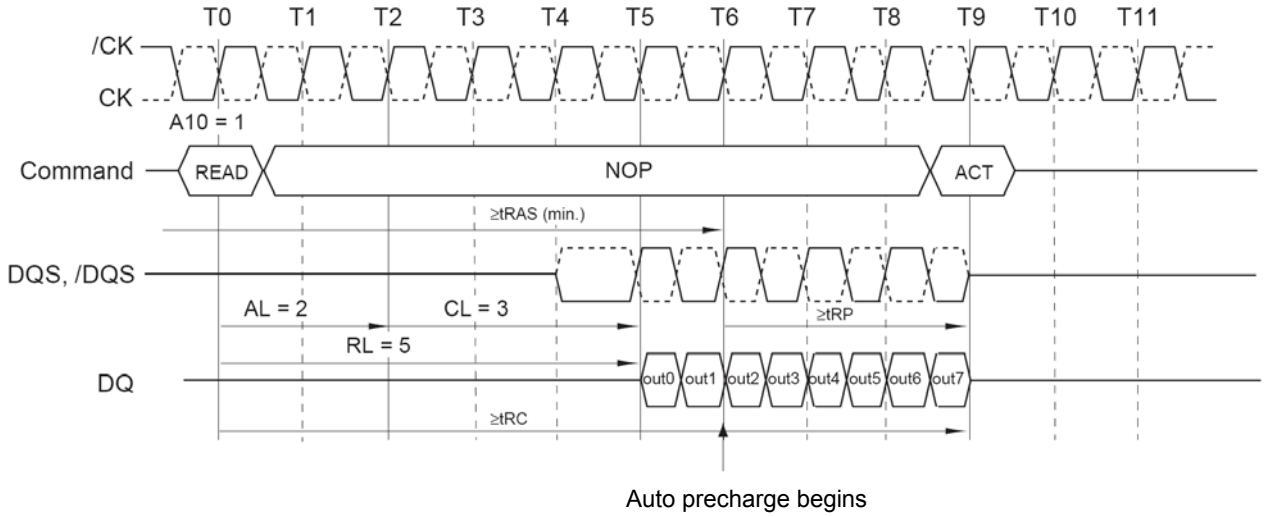
(RL = 5, BL = 4 (AL = 2, CL = 3, internal tRCD = 3))



Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRAS lockout case)
(RL = 5, BL = 4 (AL = 2, CL = 3, internal tRCD = 3))



Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRP limit)
(RL = 5, BL = 4 (AL = 2, CL = 3, internal tRCD = 3)



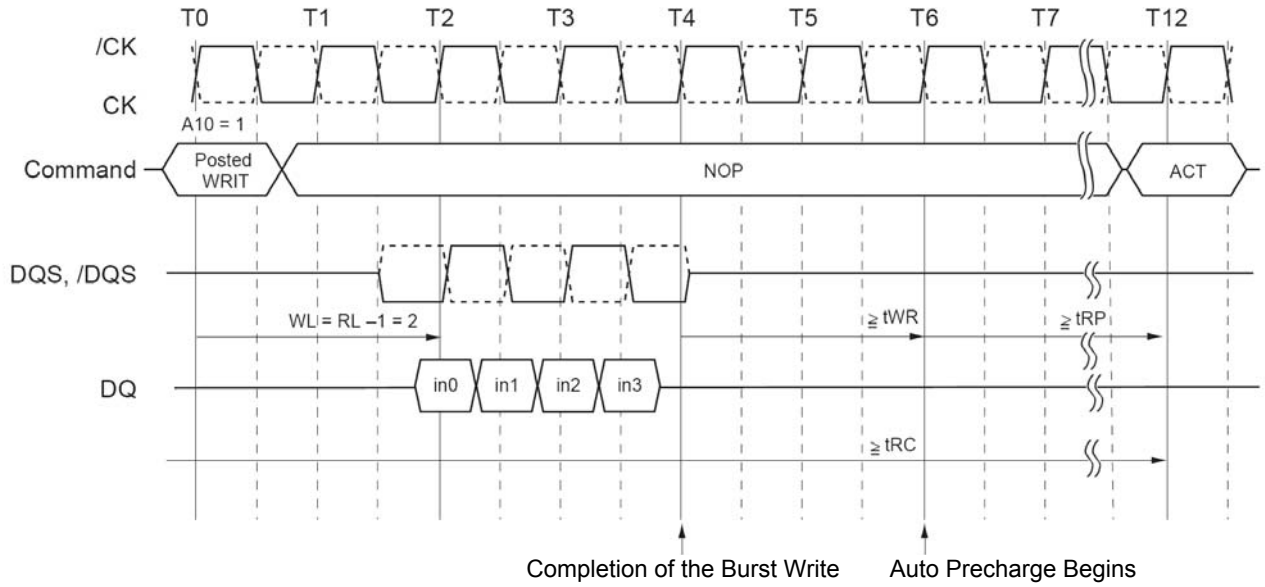
Burst Read with Auto Precharge Followed by an Activation to the Same Bank (RL = 5, BL = 8 (AL = 2, CL = 3)

Burst Write with Auto-Precharge

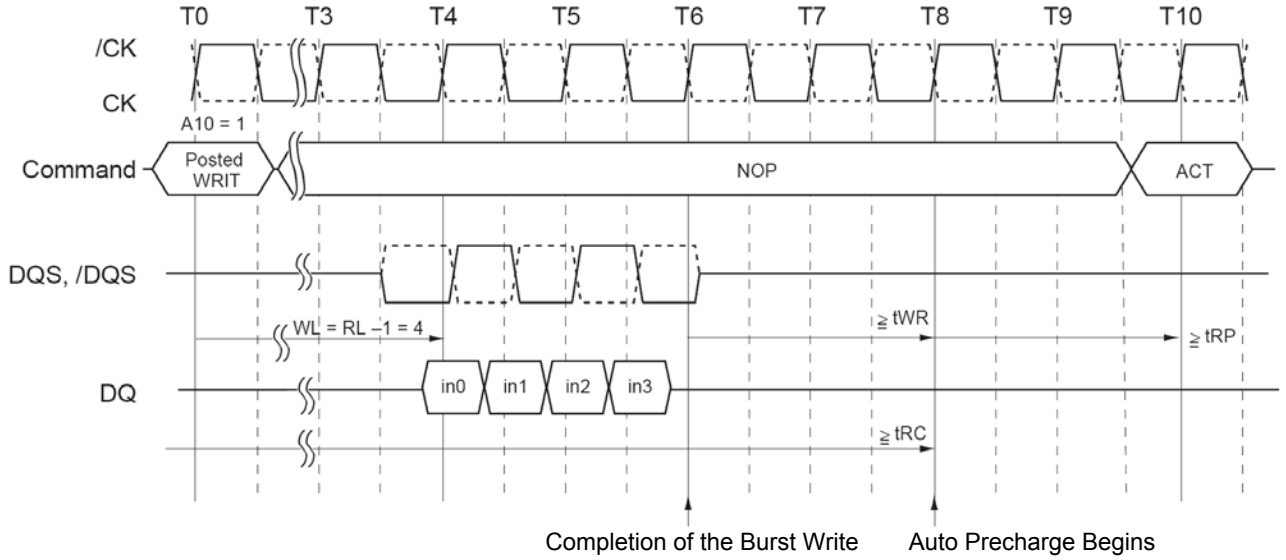
If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the write burst plus the write recovery time delay (WR), programmed in the MRS register, as long as tRAS is satisfied. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The last data-in to bank activate delay time (tDAL = WR + tRP) has been satisfied.

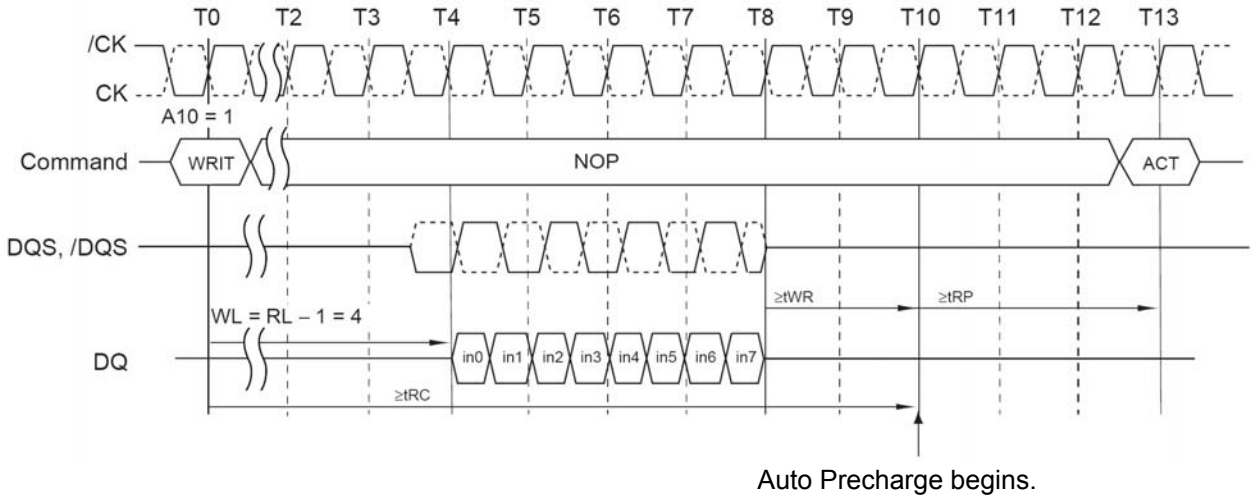
(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.



Burst Write with Auto-Precharge (tRC Limit) (WL = 2, tWR =2, tRP=3)



Burst Write with Auto-Precharge (tWR + tRP) (WL = 4, tWR =2, tRP=3)



Burst Write with Auto Precharge Followed by an Activation to the Same Bank (WL = 4, BL = 8, tWR = 2, tRP = 3)

Precharge & Auto Precharge clarification

From Command	To Command	Minimum Delay between "From command" to "to command"	Units	Note
Read	Precharge (to same Bank as Read)	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
	Precharge All	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
Read w/AP	Precharge (to same Bank as Read wAP)	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
	Precharge All	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
Write	Precharge (to same Bank as Write)	WL + BL/2 + tWR	tCK	2
	Precharge All	WL + BL/2 + tWR	tCK	2
Write w/AP	Precharge (to same bank as Write w/AP)	WL + BL/2 + WR	tCK	2
	Precharge All	WL + BL/2 + WR	tCK	2
Precharge	Precharge (to same bank as Precharge)	1	tCK	2
	Precharge All	1	tCK	2
Precharge All	Precharge	1	tCK	2
	Precharge All	1	tCK	2

Note:

1. RTP [cycles] = RU {tRTP(ns)/tCK(ns)}, where RI stands for round up.
2. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP or tRPa depending on the latest precharge command issued to that bank.

Refresh

SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit Auto-Refresh command, or by an internally timed event in Self-Refresh mode. Dividing the number of device rows into the rolling 64 ms interval defined the average refresh interval tREFI, which is a guideline to controlles for distributed refresh timing. For example, a 1Gbit DDR2 SDRAM has 8392 rows resulting in a tREFI of 7.8 µs.

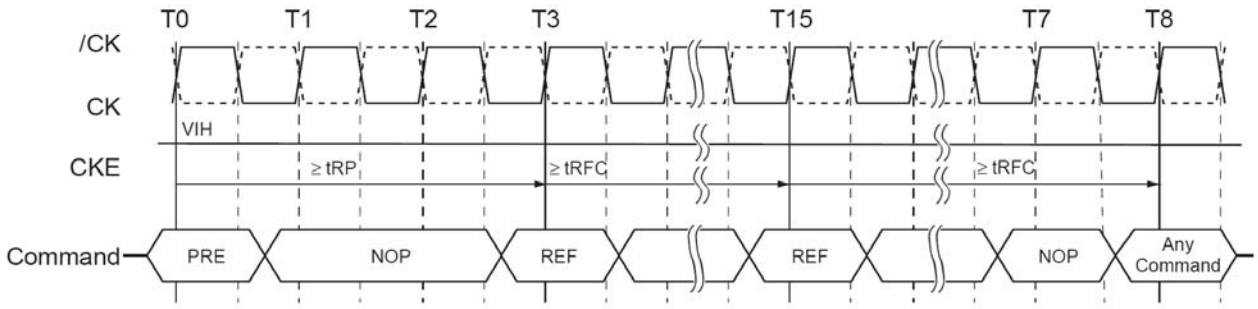
Auto-Refresh Command

Auto-Refresh is used during normal operation of the DDR2 SDRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don" t Care" during an Auto-Refresh command. The DDR2 SDRAM requires Auto-Refresh cycles at an average periodic interval of tREFI (maximum).

When /CS, /RAS and /CAS are held low and /WE high at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time (tRP) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is 9 * tREFI.



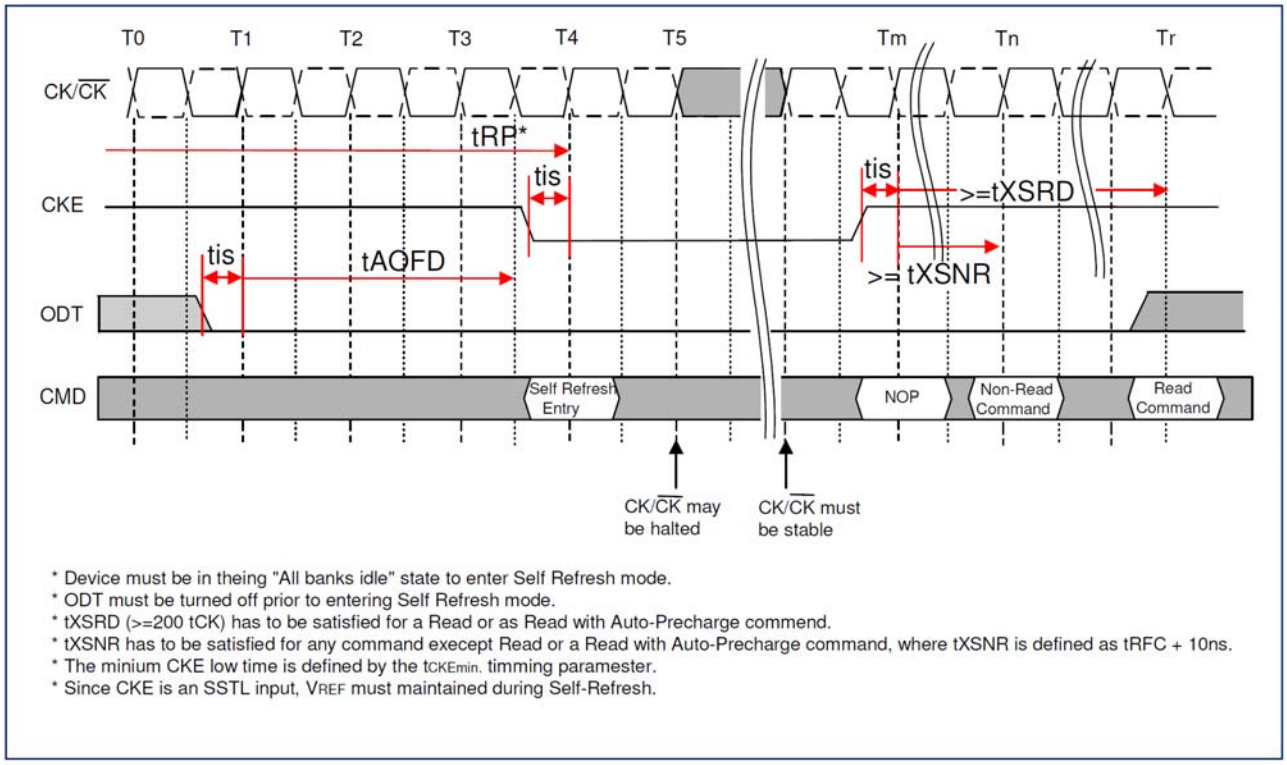
Auto Refresh Command

Self-Refresh Command

The Self-Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking.

The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having /CS, /RAS, /CAS and /CKE held low with /WE high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS (1) command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR2 SDRAM has entered Self-Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation. Once Self-Refresh Exit command is registered, a delay equal or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self-Refresh exit period (tXSNR or tXSRD) for proper operation. NOP or DESELECT commands must be registered on each positive clock edge during the Self-Refresh exit interval. Since the ODT function is not

supported during Self-Refresh operation, ODT has to be turned off tAOFD before entering Self-Refresh Mode and can be turned on again when the tXSRD timing is satisfied.



Notes:

1. Device must be in the “All banks idle” state prior to entering self refresh mode.
2. ODT must be turned off prior to entering Self Refresh mode.
3. tXSRD (>=200 tCK) has to be satisfied for a Read or as Read with Auto-Precharge commend.
4. tXSNR has to be satisfied for any command execept Read or a Read with Auto-Precharge command, where tXSNR is defined as tRFC + 10ns.
5. The minimum CKE low time is defined by the tCKEmin. timing parameter.
6. Since CKE is an SSTL input, VREF must maintained during Self-Refresh.

Power-Down

Power-down is synchronously entered when CKE is registered low, along with NOP or Deselect command. CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any other operation such as row activation, Precharge, Auto-Precharge or Auto-Refresh is in progress, but power-down IDD specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as Precharge Power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as Active Power-down. For Active Power-down two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to “low” this mode is referred as “standard active power-down mode” and a fast power-down exit timing defined by the tXARD timing parameter can be used. When A12 is set to “high” this mode is referred as a power saving “low power active power-down mode”. This mode takes longer to exit from the power-down mode and the tXARDS timing parameter has to be satisfied.

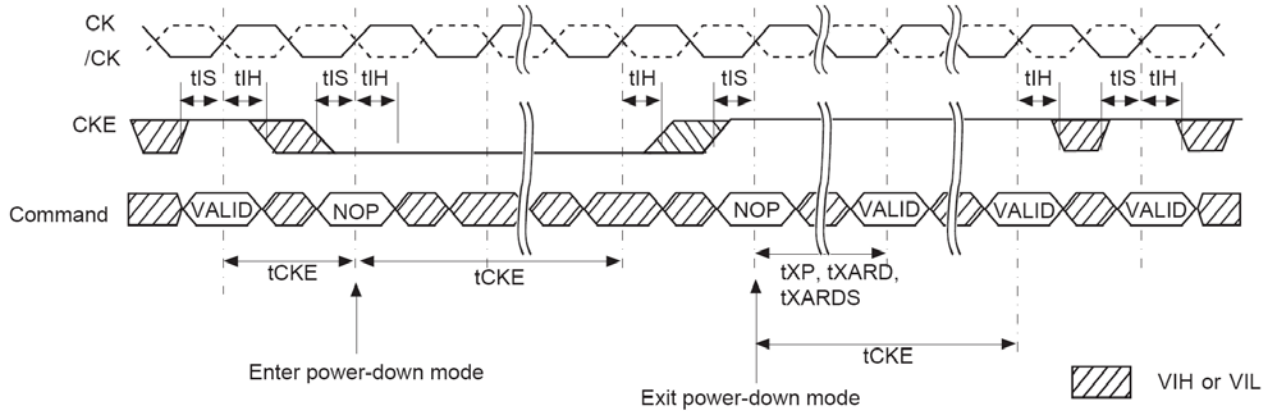
Entering power-down deactivates the input and output buffers, excluding CK, CK, ODT and CKE. Also the DLL is disabled upon entering Precharge Power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are “Don‟t Care”. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, tXP, tXARD or tXARDS, after CKE goes high. Power-down exit latencies are defined in the AC spec table of this data sheet.

Power-Down Entry

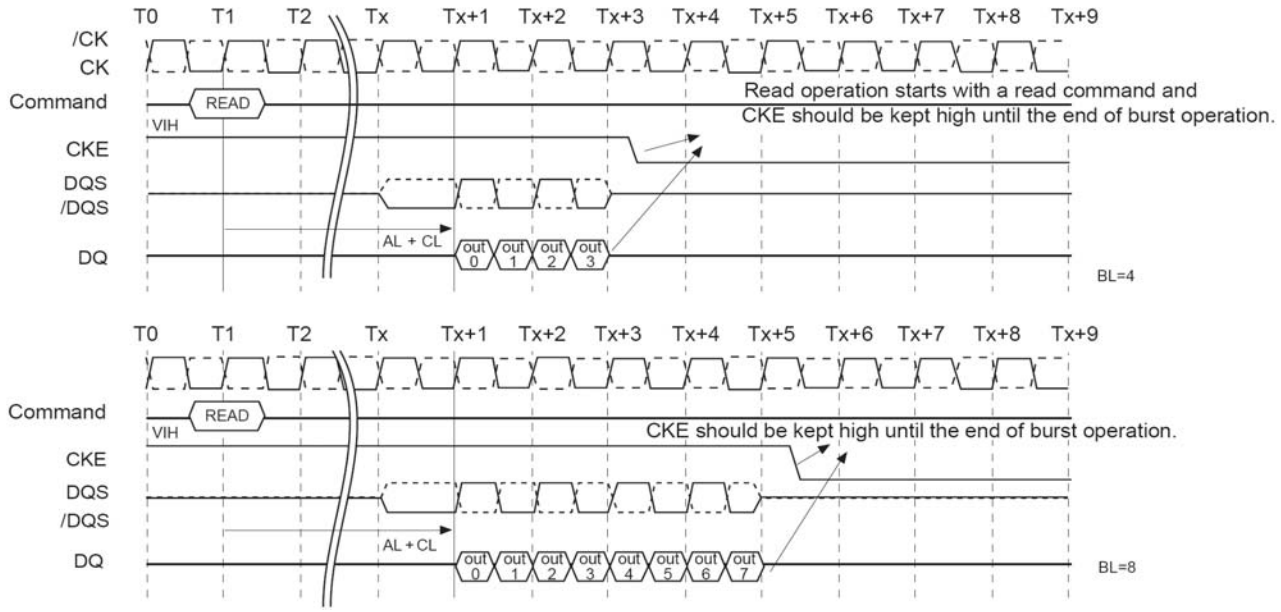
Active Power-down mode can be entered after an activate command. Precharge Power-down mode can be entered after a precharge, Precharge-All or internal precharge command. It is also allowed to enter power-mode after an Auto-Refresh command or MRS / EMRS(1) command when tMRD is satisfied. Active Power-down mode entry is prohibited as long as a Read Burst is in progress, meaning CKE should be kept high until the burst operation is finished. Therefore Active Power-Down mode entry after a Read or Read with Auto-Precharge command is allowed after RL + BL/2 is satisfied. Active Power-down mode entry is prohibited as long as a Write Burst and the internal write recovery is in progress. In case of a write command, active power-down mode entry is allowed then WL + BL/2 + tWTR is satisfied.

In case of a write command with Auto-Precharge, Power-down mode entry is allowed after the internal precharge command has been executed, which WL + BL/2 + WR is starting from the write with Auto-Precharge command. In case the DDR2 SDRAM enters the Precharge Power-down mode.

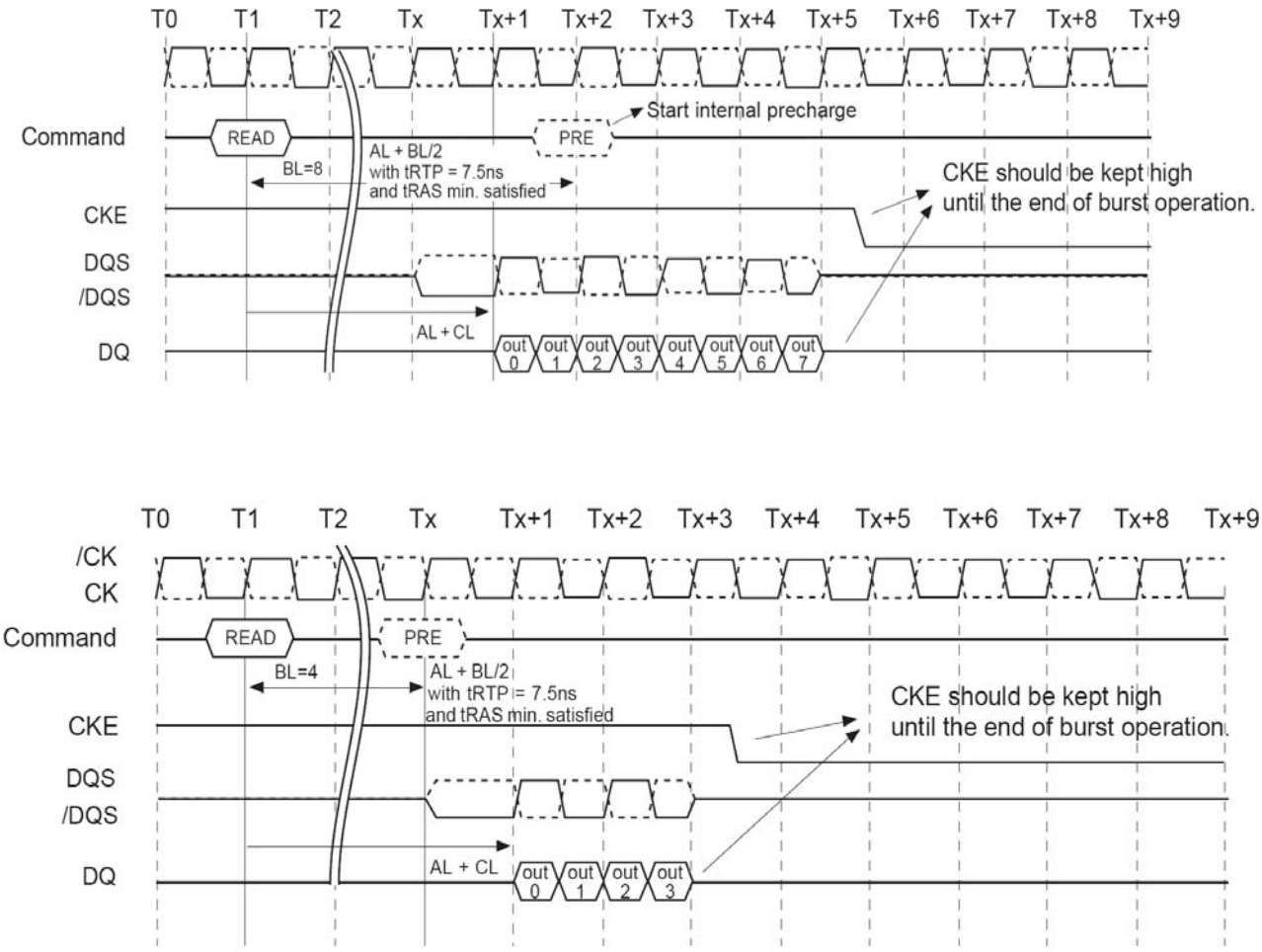


Power Down

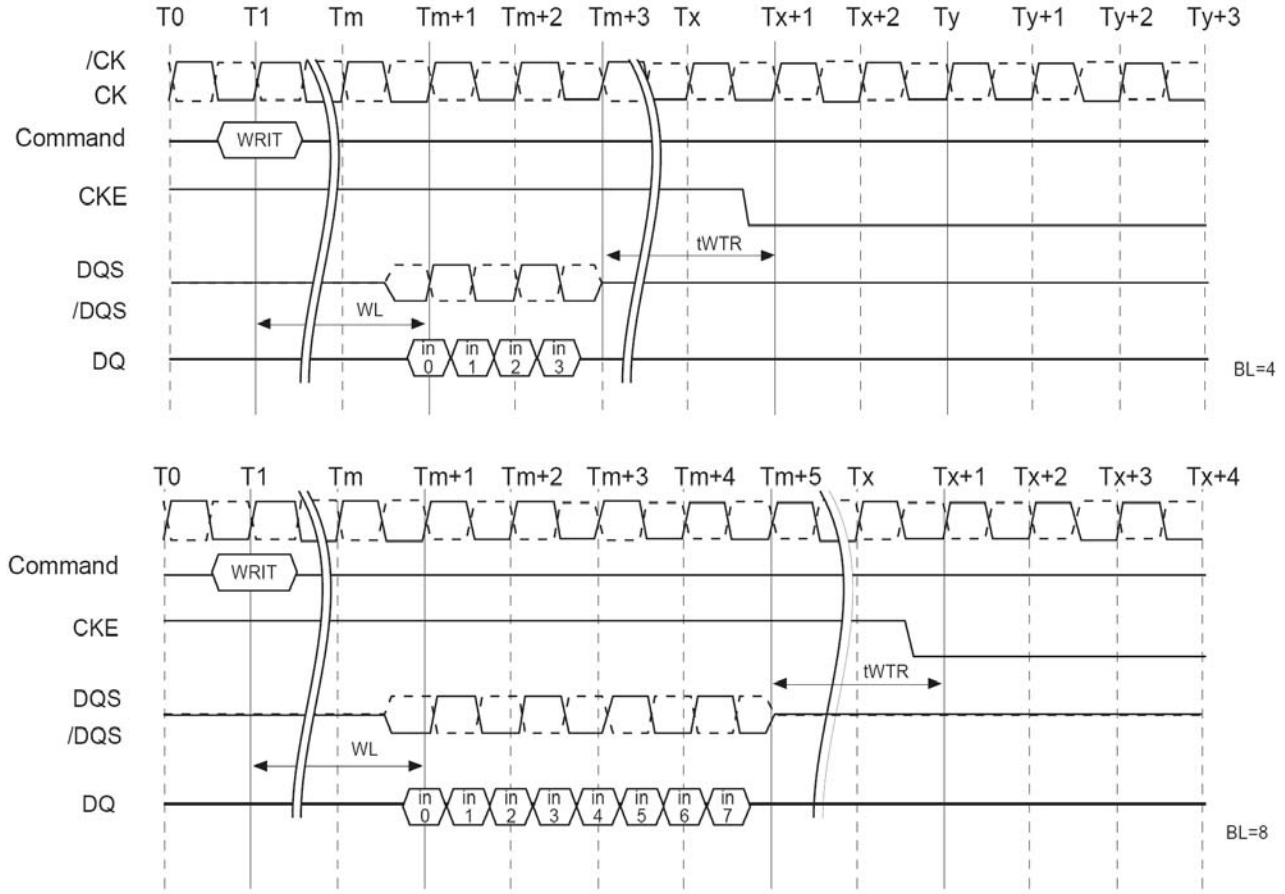
Read to Power-Down Entry



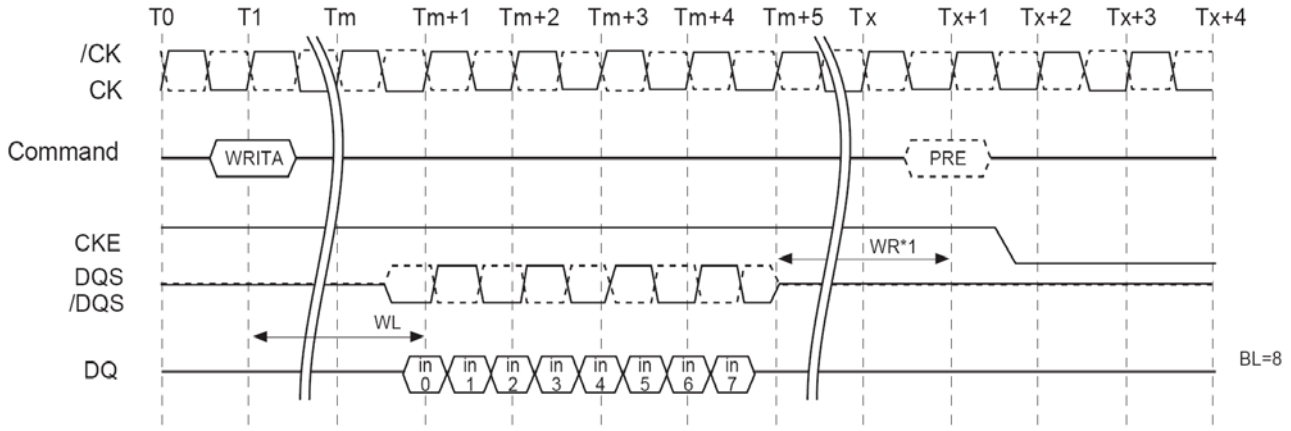
Read with Auto Precharge to Power-Down Entry

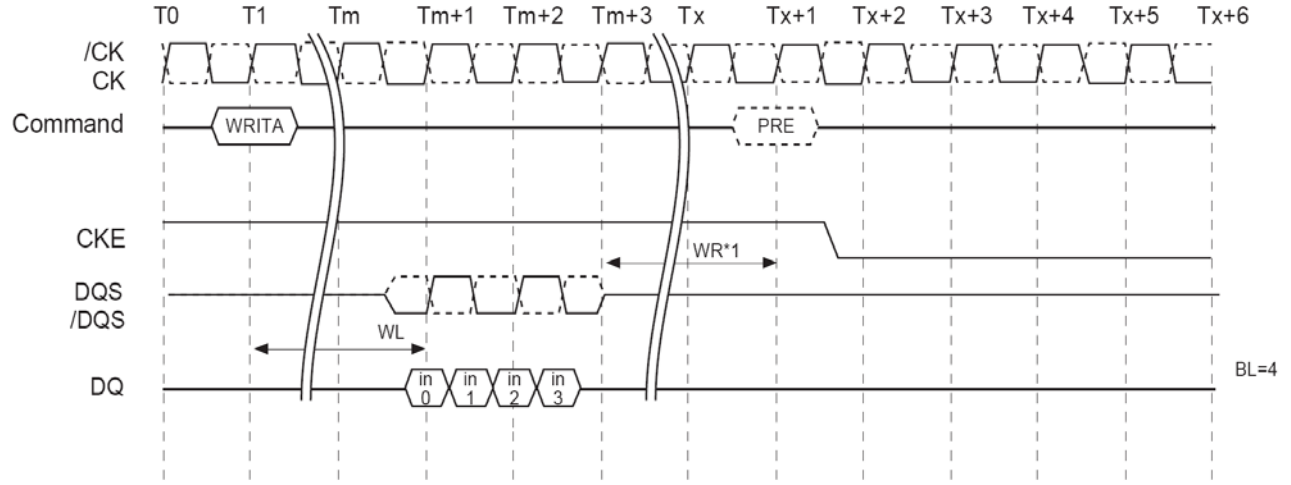


Write to Power-Down Entry



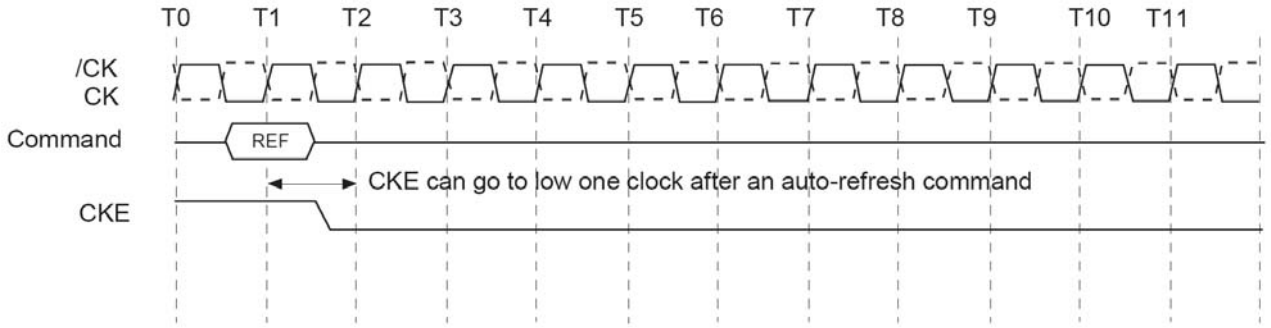
Write with Auto Precharge to Power-Down Entry



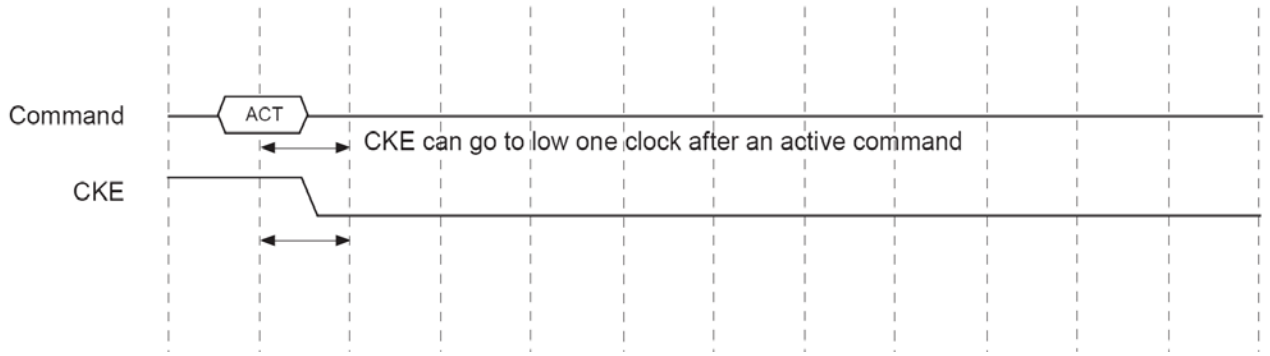


Note: 1. WR is programmed through MRS

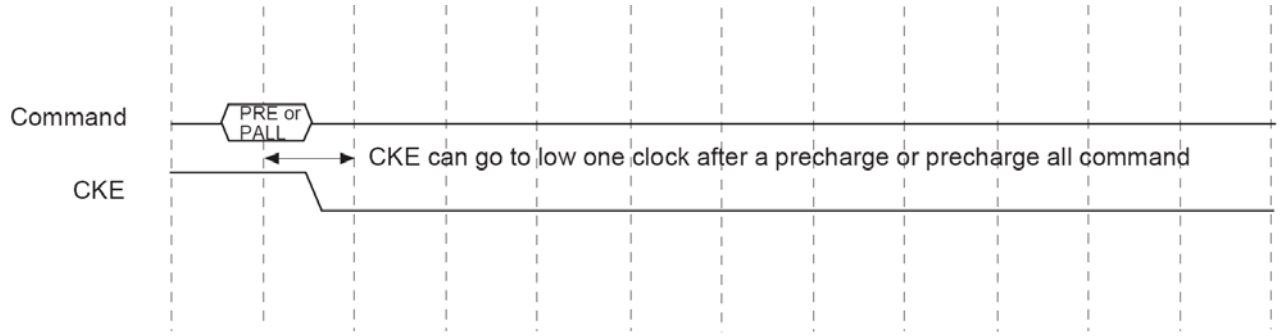
Refresh command to Power-Down Entry



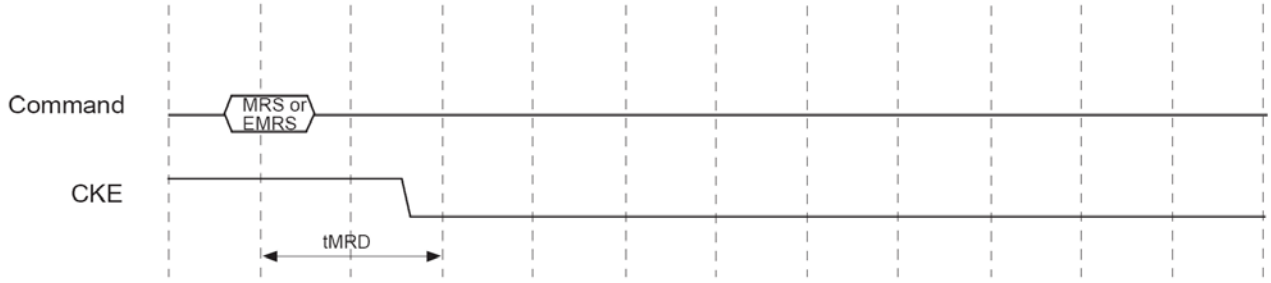
Active command to power down entry



Precharge/Precharge all command to power down entry



MRS/EMRS command to power down entry



No Operation Command

The No Operation Command should be used in cases when the SDRAM is in an idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when /CS is low with /RAS, /CAS, and /WE held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when /CS is brought high, the /RAS, /CAS, and /WE signals become don't care.

Input Clock Frequency Change

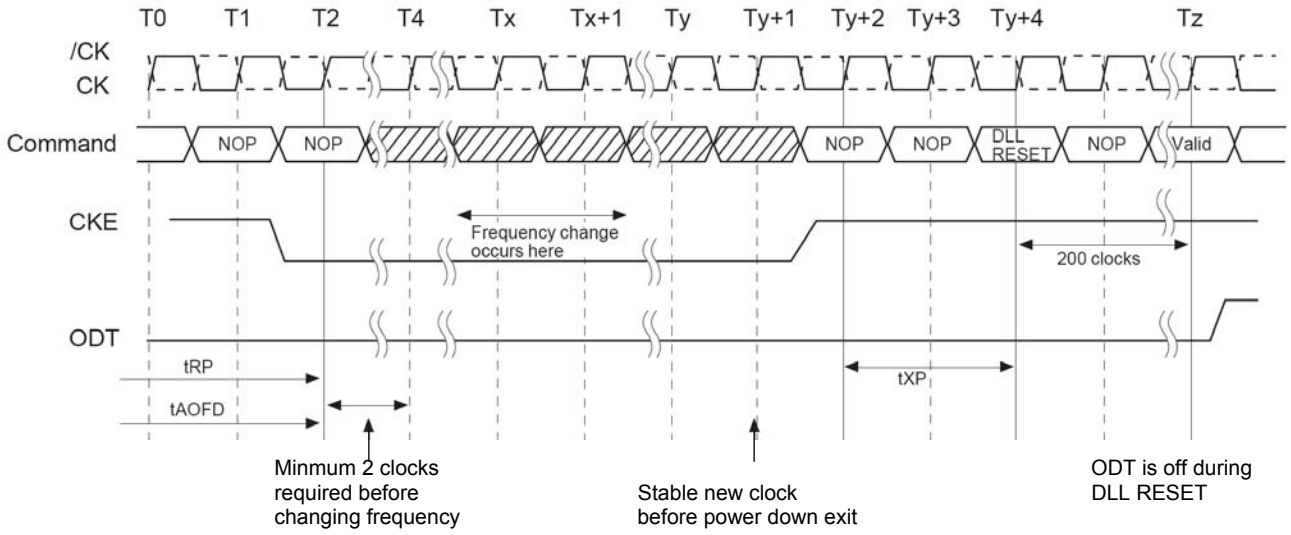
During operation the DRAM input clock frequency can be changed under the following conditions:

a) During Self-Refresh operation

b) DRAM is in Precharge Power-down mode and ODT is completely turned off.

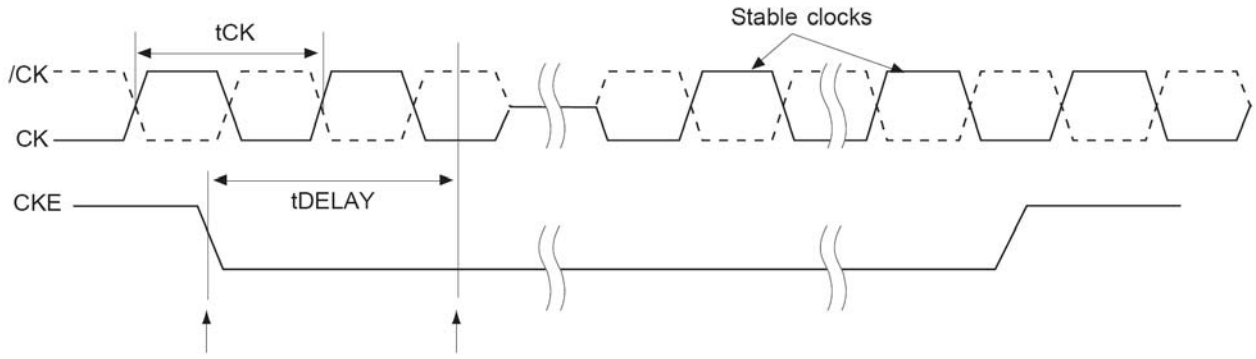
The DDR2-SDRAM has to be in Precharged Power-down mode and idle. ODT must be allready turned off and CKE must be at a logic "low" state. After a minimum of two clock cycles after tRP and tAOFD have been satisfied the input clock frequency can be changed. A stable new clock frequency has to be provided, before CKE can be changed to a "high" logic level again. After tXP has been satisfied a DLL RESET command via EMRS(1) has to be issued. During the following DLL re-lock period of 200 clock cycles, ODT must remain off. After the DLL-re-lock period the DRAM is ready to operate with the new clock frequency.

Clock Frequency Change in Precharge Power Down Mode



Asynchronous CKE Low Event

DRAM requires CKE to be maintained “high” for all valid operations as defined in this data sheet. If CKE asynchronously drops “low” during any valid operation DRAM is not guaranteed to preserve the contents of the memory array. If this event occurs, the memory controller must satisfy a time delay (tdelay) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “high” again. The DRAM must be fully re-initialized as described the the initialization sequence (section 2.2.1, step 4 thru 13). DRAM is ready for normal operation after the initialization sequence. See AC timing parametric table for tDELAY specification.



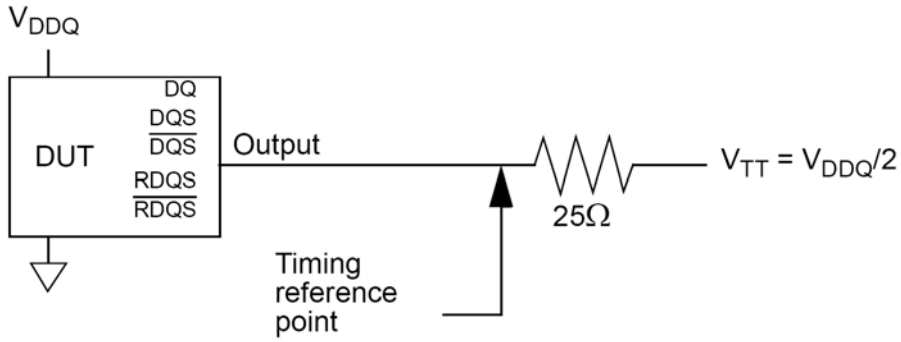
CKE asynchronously drops low

Clocks can be turned off after this point

Reference Loads, Setup & Hold Timing Definition and Slew Rate Derating

Reference Load for Timing Measurements

The figure represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally a coaxial transmission line terminated at the tester electronics. This reference load is also used for output slew rate characterization.



AC Timing Reference Load

The output timing reference voltage level for single ended signals is the cross point with VTT.
The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. /DQS) signal.

Slew rate Measurements

Output Slew rate

With the reference load for timing measurements output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS, /DQS) output slew rate is measured between DQS - /DQS = - 500 mV and DQS - /DQS = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

Input Slew rate - Differential signals

Input slew rate for differential signals (CK, /CK, DQS, /DQS, RDQS, /RDQS) for rising edges are measured from CK - /CK = -250 mV to CK - /CK = + 500 mV and from CK - CK = +250 mV to CK - CK = - 500mV for falling edges.

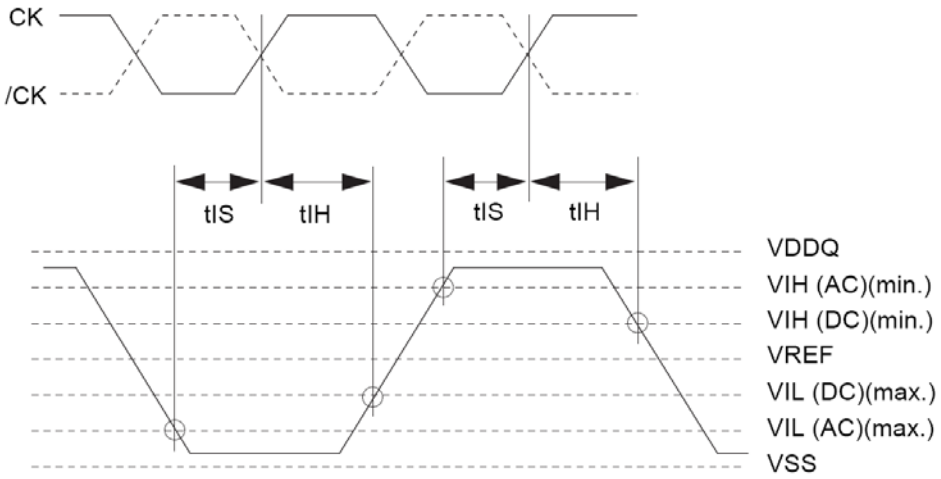
Input Slew rate - Single ended signals

Input slew rate for single ended signals (other than tis, tih, tds and tdh) are measured from dc-level to ac-level: VREF -125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV to VREF - 250 mV for falling edges.

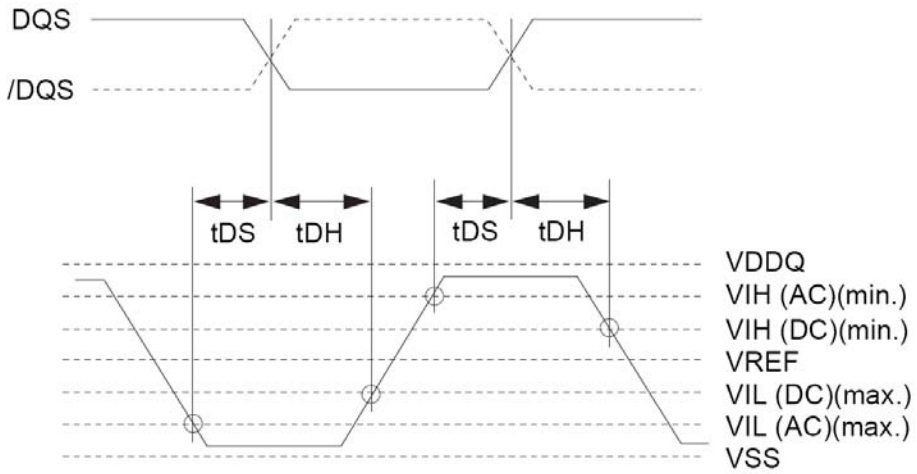
Input and Data Setup and Hold Time

Timing Definition for Input Setup (tIS) and Hold Time (tIH)

Address and control input setup time (tIS) is referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test. Address and control input hold time (tIH) is referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test.



Timing Definition for Data Setup (tDS) and Hold Time (tDH)



1. Data input setup time with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level to differential data strobe crosspoint for a falling signal applied to the device under test. Input waveform timing with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the VIH(ac) level to the data strobe crossing Vref for a rising signal, and from the input signal crossing at the VIL(ac) level to the single-ended data strobe crossing Vref for a falling signal applied to the device under test.

2. Data input hold time with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the VIL(dc) level to the differential data strobe crosspoint for a rising signal and VIH(dc) to the differential data strobe crosspoint for a falling signal applied to the device under test. Input waveform timing with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the VIL(dc) level to the single-ended data strobe crossing Vref for a rising signal and VIH(dc) to the single-ended data strobe crossing Vref for a falling signal applied to the device under test.

Slew Rate Definition for Input and Data Setup and Hold Times

Setup (tIS & tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VIH(ac)min. Setup (tIS & tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VIL(ac)max, (fig. A) If the actual signal is always earlier than the nominal slew rate line between shaded „dc to ac region" , use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded „dc to ac region" , the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.(fig.B)

Hold (tIH & tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of Vref. Hold (tIH & tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of Vref.(fig. A). If the actual signal is always later than the nominal slew rate line between shaded „dc to Vref region" , use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded „dc to Vref region" , the slew rate of a tangent line to the actual signal from the dc level to Vref level is used for derating value.(fig.B)

Single-ended DQS

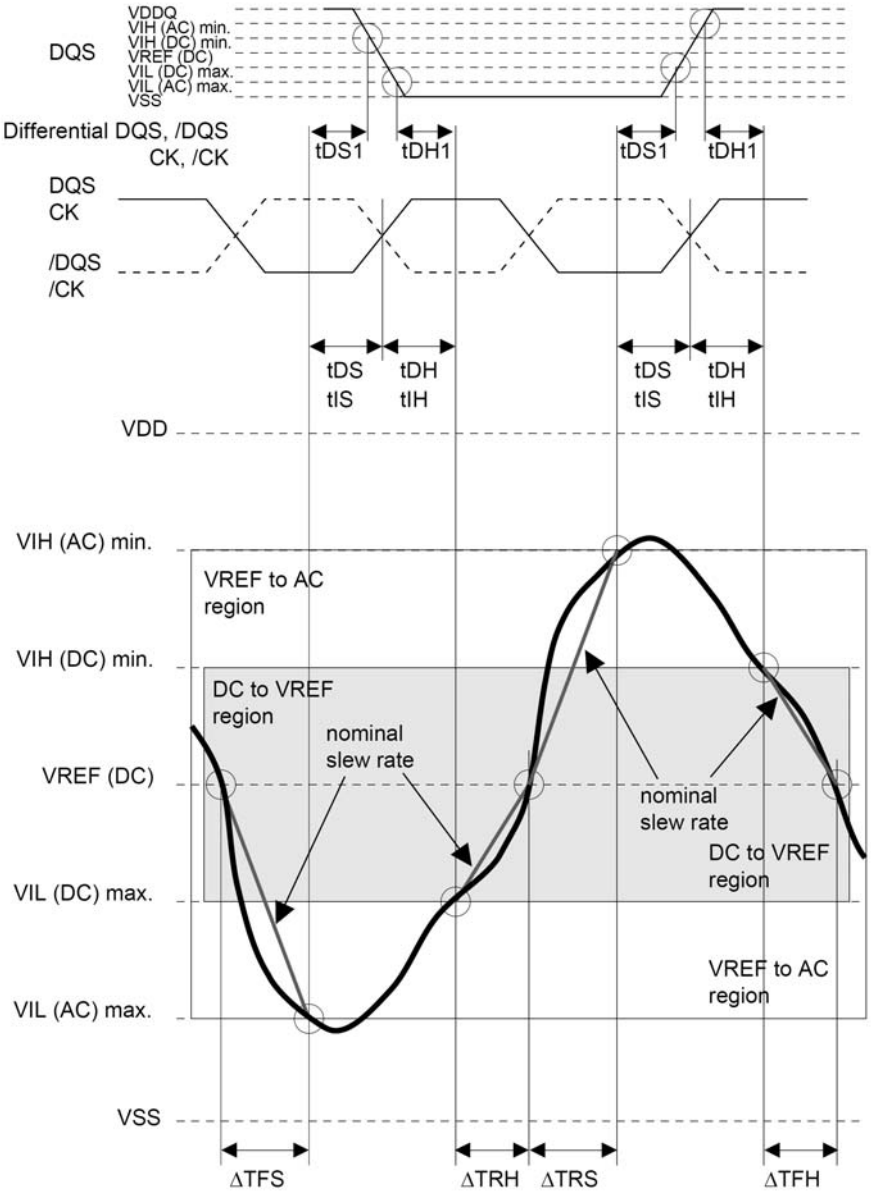


Fig. A Slew Rate Definition Nominal

$$\text{Setup slew rate Falling signal} = \frac{\text{VREF (DC) – VIL (AC) max.}}{\Delta TFS}$$

$$\text{Setup slew rate Rising signal} = \frac{\text{VIH (AC) min. – VREF (DC)}}{\Delta TRS}$$

$$\text{Hold slew rate Rising signal} = \frac{\text{VREF (DC) – VIL (DC) max.}}{\Delta TRH}$$

$$\text{Hold slew rate Falling signal} = \frac{\text{VIH (DC) min. – VREF (DC)}}{\Delta TFH}$$

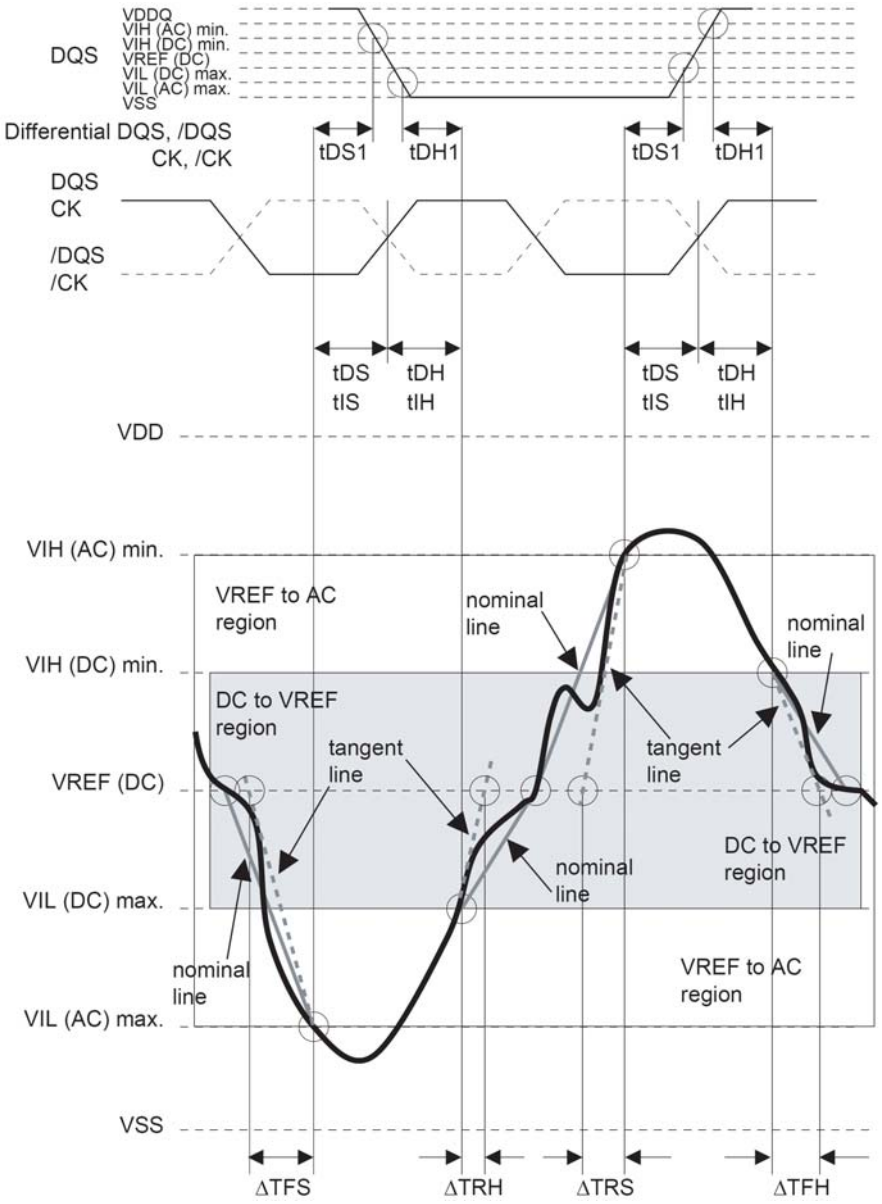


Fig. B Slew Rate Definition Tangent

$$\text{Setup slew rate Falling signal} = \frac{\text{tangent line [VREF (DC) – VIL (AC) max.]}}{\Delta TFS}$$

$$\text{Setup slew rate Rising signal} = \frac{\text{tangent line [VIH (AC) min. – VREF (DC)]}}{\Delta TRS}$$

$$\text{Hold slew rate Rising signal} = \frac{\text{tangent line [VREF (DC) – VIL (DC) max.]}}{\Delta TRH}$$

$$\text{Hold slew rate Falling signal} = \frac{\text{tangent line [VIH (DC) min. – VREF (DC)]}}{\Delta TFH}$$

Input Setup (tIS) and Hold (tIH) Time Derating Table

		CK, /CK Differential Slew Rate						Units
		(-E6 / E7 / G8)						
		2.0 V/ns		1.5 V/ns		1.0 V/ns		
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
Command/Address Slew rate (V/ns)	4.00	150	94	180	124	210	154	ps
	3.50	143	89	173	119	203	149	ps
	3.00	133	83	163	113	193	143	ps
	2.50	120	75	150	105	180	135	ps
	2.00	100	45	130	75	160	105	ps
	1.50	67	21	97	51	127	81	ps
	1.00	0	0	30	30	60	60	ps
	0.90	-5	-14	25	16	55	46	ps
	0.80	-13	-31	17	-1	47	29	ps
	0.70	-22	-54	8	-24	38	6	ps
	0.60	-34	-83	-4	-53	26	-23	ps
	0.50	-60	-125	-30	-95	0	-65	ps
	0.40	-100	-188	-70	-158	-40	-128	ps
	0.30	-168	-292	-138	-262	-108	-232	ps
	0.25	-200	-375	-170	-345	-140	-315	ps
	0.20	-325	-500	-295	-470	-265	-440	ps
	0.15	-517	-708	-487	-678	-457	-648	ps
	0.10	-1000	-1125	-970	-1095	-940	-1065	ps

Data Setup (tDS) and Hold Time (tDH) Derating Table

		DQS, /DQS Differential Slew Rate																	
		(E6, E7, F8/G8)																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ Slew Rate (V/ns)	**2.0**	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

Notes:

1. All units in ps.
2. For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the individual datasheet value to the derating value listed in the previous table.

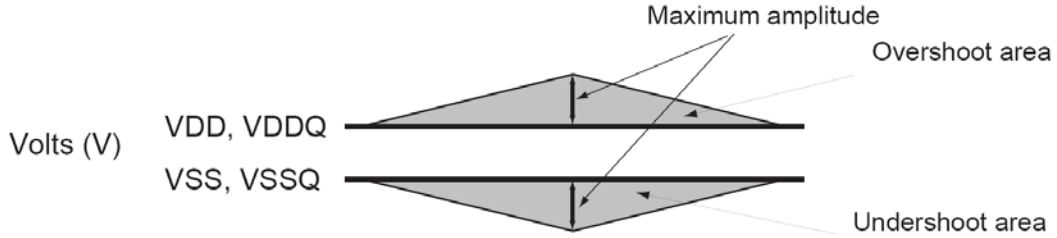
Overshoot and Undershoot Specification

Address and Control Pins

Parameter	E6	E7	F8/G8	Units
Maximum peak amplitude allowed for overshoot area	0.5	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	0.5	V
Maximum overshoot area above VDD	0.8	0.66	0.66	V-ns
Maximum undershoot area below VSS	0.8	0.66	0.66	V-ns

Clock, Data, Strobe and Mask Pins

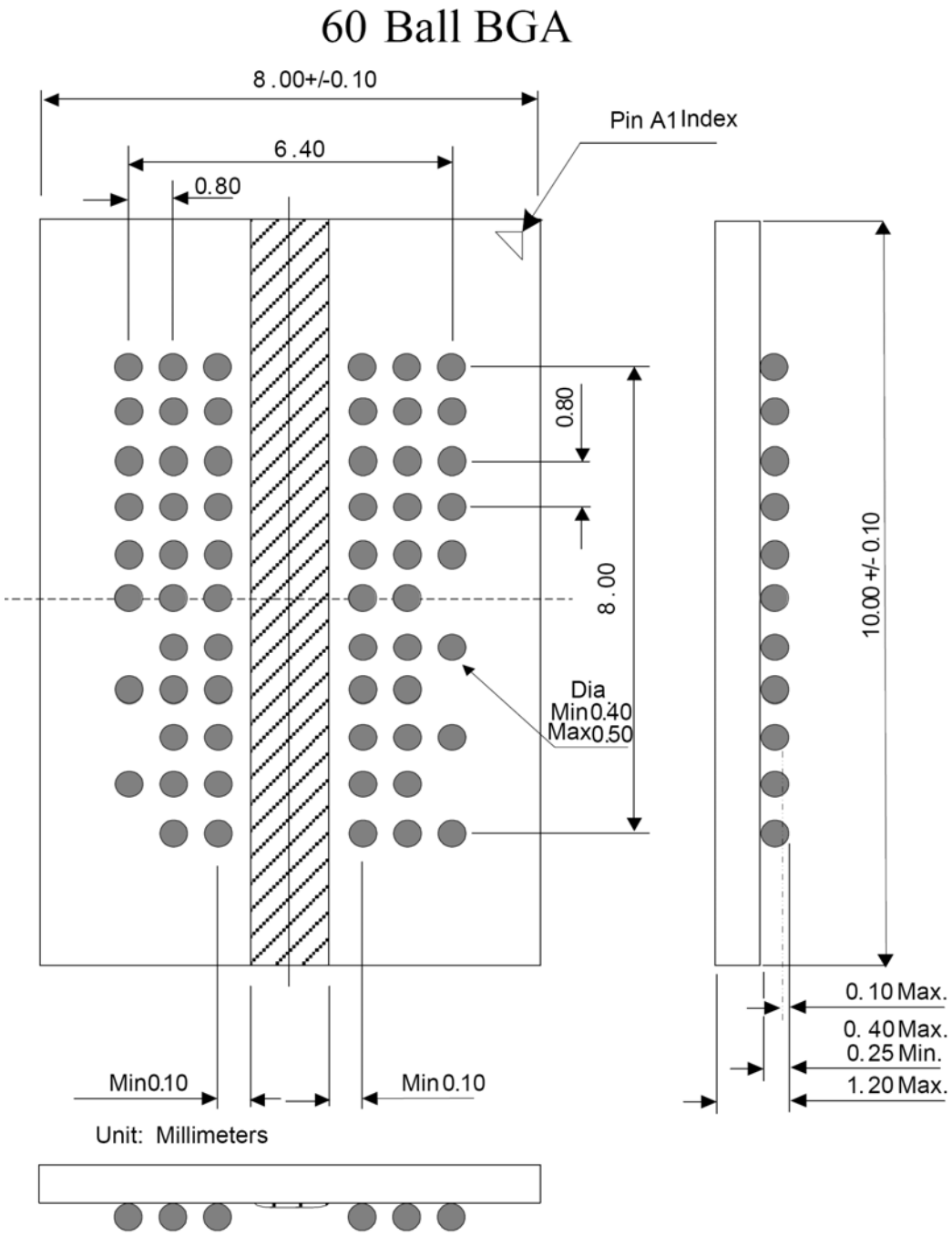
Parameter	E6	E7	F8/G8	Units
Maximum peak amplitude allowed for overshoot area	0.5	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	0.5	V
Maximum overshoot area above VDD	0.23	0.23	0.23	V-ns
Maximum undershoot area below VSS	0.23	0.23	0.23	V-ns



Overshoot/Undershoot Definition

Package Dimensions

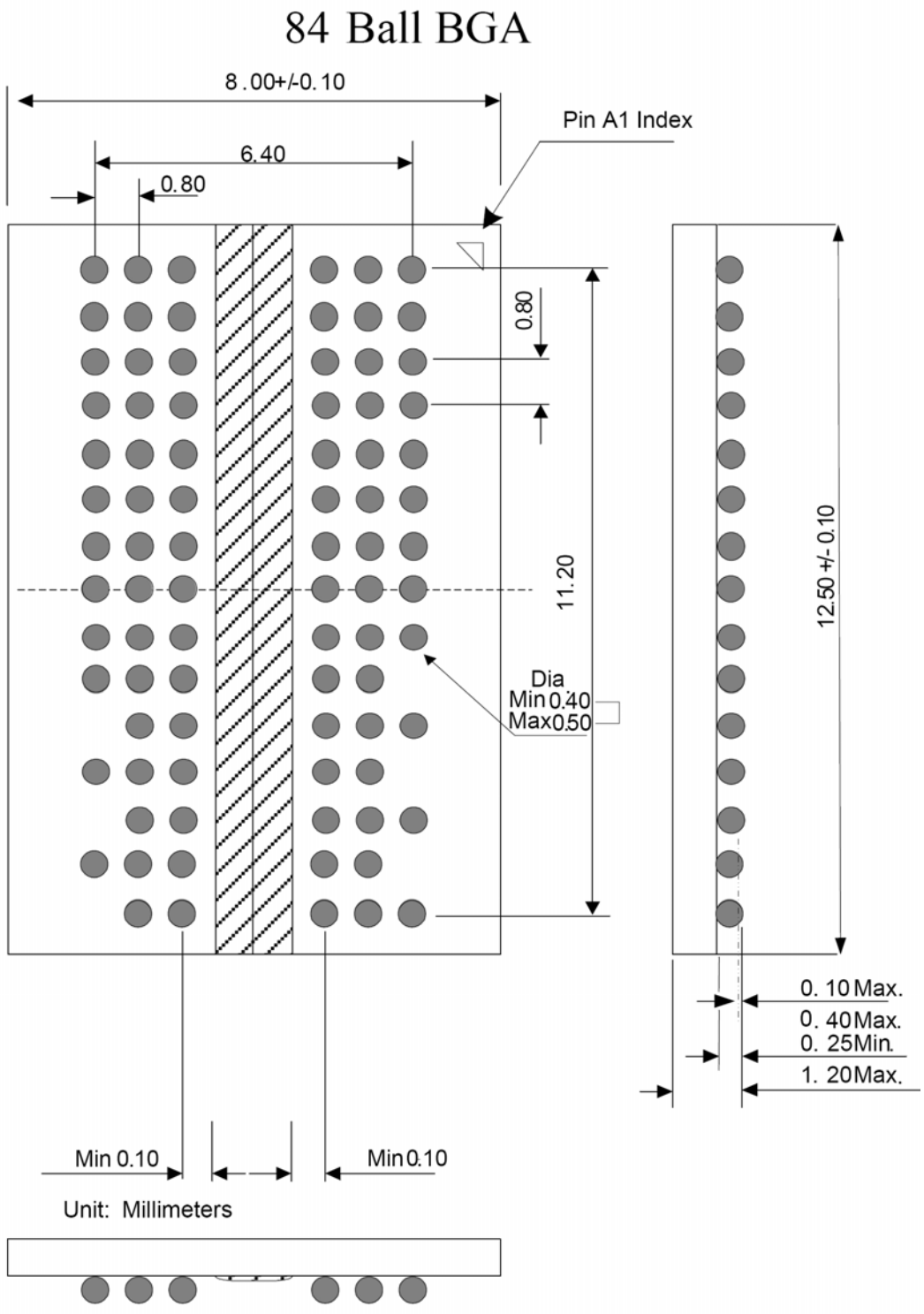
(x8; 60 balls; BGA Package)



Note : All dimensions are typical unless otherwise stated.

Package Dimensions

(X16; 84 balls; BGA Package)



Note : All dimensions are typical unless otherwise stated.